Honeywell

High-Performance Process Manager Service

HP13-500

Total Plant

PM/APM/HPM Service - 1

High-Performance Process Manager Service

HP13-500
Release 500
CE Compliant
3/96

Copyright, Notices, and Trademarks

© Copyright 1995 by Honeywell Inc.

Revision 03 – March 1, 1996

While this information is presented in good faith and believed to be accurate, Honeywell disclaims the implied warranties of merchantability and fitness for a particular purpose and makes no express warranties except as may be stated in its written agreement with and for its customer.

In no event is Honeywell liable to anyone for any indirect, special or consequential damages. The information and specifications in this document are subject to change without notice.

TDC 3000 is a U. S. trademark of Honeywell Inc.

Process Manager is a U. S. trademark of Honeywell Inc.

SMARTLINE is a U. S. trademark of Honeywell Inc.

Other brand or product names are trademarks of their respective owners.

Honeywell
Industrial Automation and Control
Automation College
2820 West Kelton Lane
Phoenix, AZ 85023

(602) 313-5669

About This Publication

This publication provides instructions for use by the High-Performance Process Manager maintenance personnel. It will help you to maintain, test, troubleshoot, and repair the equipment.

This manual supports the Release 500 software. The Universal Station (US) displays shown in this manual are produced by R500 software.

This publication supports CE Compliant equipment. Any equipment designated as "CE Compliant" complies with the European Union EMC and its health and safety directives. All equipment entering the European countries after January 1, 1996 require this type of compliance, denoted by the "CE Mark."

TECHNICAL ASSISTANCE

If you need assistance	If you need technical assistance, contact your local Honeywell Service Organization, as explained in the following paragraphs.
International customers	Outside of the United States, contact your local Honeywell Service Organization. If you are not sure of the location or telephone number, call your Honeywell representative for information.
Customers inside the United States	Within the United States, call the Technical Assistance Center (TAC) at the toll free number 1-800-822-7673.
Arizona customers	Within Arizona, the local number for TAC is 602-313-5558.
Services provided	Calls to TAC are answered by a dispatcher from 7:00 A.M. to 5:00 P.M., Mountain Standard Time (6:00 A.M. to 4:00 P.M. when daylight saving time is in effect). Outside of these hours, emergency calls—those which affect your ability to control or view a process—will be received by an answering service, and returned within one hour. TAC maintains its own TDC 3000^X system, and frequently can duplicate equipment problems.
Time saving tip	It is a good idea to make specific notes about the problem before making the call. This will help to reduce delays and expedite answers.

Standard Symbols

Scope

The standard symbols used in this publication are defined as follows.

ATTENTION

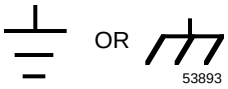
Notes inform the reader about information that is required, but not immediately evident.

CAUTION

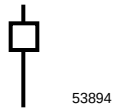
Cautions tell the user that damage may occur to equipment if proper care is not exercised.

WARNING

Warnings tell the reader that potential personal harm or serious economic loss may happen if instructions are not followed.



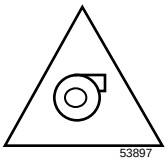
Ground connection to building safety ground.



Ground stake for building safety ground.

Electrical Shock Hazard—can be lethal.

Electrical Shock Hazard—can be lethal.



Rotating Fan—can cause personal injury.

Caution—refer to the appropriate installation document.

Table of Contents

SECTION 1 – INTRODUCTION 1

1.1 Overview 1
1.2 Purpose of this Manual 1

SECTION 2 – EQUIPMENT DESCRIPTION 3

2.1 Overview 3
2.2 Power System Controls 4
2.2.1 Power Supply Module Control 4
2.2.2 HPMM/IOP Card Power Interrupt Switches 5
2.3 HPM Subsystem Overview 6
2.4 HPMM and IOP Card Files 9
2.5 HPMM Card Files 10
2.5.1 HPMM Description 12
2.6 IOP Card Files 18
2.6.1 IOPs 20
2.6.2 Redundant IOPs 21
2.6.3 Low Level Multiplexer IOP (LLMux) 23
2.6.4 Serial Device Interface IOP (SDI) 25
2.6.5 Serial Interface IOP (SI) 29
2.7 I/O Link Extender (Fiber Optic Link) 32
2.8 Field Termination Assembly 38
2.9 FTA Mounting Channels 48
2.10 Power Systems 51
2.10.1 Power Distribution 57
2.10.2 Battery Backup Module 58
2.10.3 CMOS Battery Backup 60
2.10.4 24 Vdc Power Distribution 62
2.10.5 Cabinet Fan Assembly 63
2.10.6 LLAI Line Frequency Clock Voltage 63
2.10.7 24 Vdc Fuse Protection 64
2.10.8 5 Vdc Fuse Protection 81
2.10.9 Card File Power Cabling 82
2.11 I/O Link Interface Cabling 88
2.12 IOP to FTA Cabling 92
2.13 Power Adapter Cabling 94
2.14 UCN Cable System 97
2.15 UCN Node Address Pinning 100
2.16 I/O Link Interface Address Pinning 105
2.17 Firmware/Hardware/Software Correlation 111

Table of Contents

SECTION 3 – UCN STATUS DISPLAYS 113

3.1 Overview 113
3.2 Display Definitions 115
3.2.1 NIM Detail Status Displays 115
3.2.2 HPMM Detail Status Displays 115
3.2.3 IOP Detail Status Displays 116
3.3 Detail Status Display Selection Procedures 116
3.3.1 NIM Detail Status Display 116
3.3.2 HPMM Detail Status Display 119
3.3.3 IOP Detail Status Display 121
3.4 Display Operation 122
3.4.1 UCN Status Displays 122
3.4.1.1 LOAD/SAVE RESTORE Target 127
3.4.1.2 CONTROL STATES Target 129
3.4.1.3 AUTO CHECKPT Target 131
3.4.1.4 UCN CABLE STATUS Target 133
3.4.1.5 RUN STATES Target 140
3.4.1.6 SLOT SUMMARY Target 142
3.4.1.7 DETAIL STATUS Target 143
3.4.2 HPM Status Displays 144
3.4.2.1 LOAD/SAVE RESTORE Target 151
3.4.2.2 CONTROL STATES Target 153
3.4.2.3 AUTO CHECKPT Target 154
3.4.2.4 IOL CABLE COMMANDS Target 155
3.4.2.5 RUN STATES Target 157
3.4.2.6 SLOT SUMMARY Target 159
3.4.2.7 DETAIL STATUS Target 160
3.4.3 NIM Detail Status Displays 161
3.4.4 HPMM Detail Status Displays 166
3.4.4.1 HPMM I/O Link Information Displays 169
3.4.4.2 IOM I/O Link Information Displays 173
3.4.4.3 HPMM Version/Revision Display 175
3.4.4.4 HPMM Control Configuration Display 177
3.4.4.5 HPM Write Lockout Displays 180
3.4.4.6 HPMM Schedule Information Display 183
3.4.4.7 HPMM UCN Statistics Displays 185
3.4.4.8 HPMM Maintenance Support Displays 187
3.4.4.9 HPMM Soft Failure Displays 194
3.4.5 IOP Detail Status Displays 197
3.4.5.1 IOP Box Soft Failures Displays 201
3.4.5.2 IOP Slot Soft Failures Displays 205
3.4.5.3 IOP Slots with Soft Failures Display 208
3.4.5.4 HLAI IOP Detail Status Display 209
3.4.5.5 LLAI IOP Detail Status Display 211
3.4.5.6 AO IOP Detail Status Display 216
3.4.5.7 LLMux IOP Detail Status Display 220
3.4.5.8 DI IOP Detail Status Display 223
3.4.5.9 DO IOP Detail Status Display 224
3.4.5.10 STI/STIM IOP Detail Status Display 226
3.4.5.11 PI IOP Detail Status Display 227
3.4.5.12 SDI IOP Detail Status Display 228
3.4.5.13 SI IOP Detail Status Display 229
3.4.5.14 DISOE IOP Detail Status Display 230

Table of Contents

SECTION 4 – FAULT ISOLATION 231

4.1 Overview 231
4.2 Failure Types 232
4.3 Fault Isolation Concepts 235
4.3.1 Troubleshooting Flow Chart 237
4.3.2 HPMM Corrective Actions (Table 4-1) 243
4.3.3 Comm/Control Hard Failure Codes (Table 4-2) 245
4.3.4 HPMM Soft Failure Codes (Table 4-3) 268
4.3.5 I/O Link Hard Failure Codes (Table 4-4) 273
4.3.6 IOP Hard Failure Codes (Table 4-5) 275
4.3.7 IOP Box Soft Failure Codes (Table 4-6) 277
4.3.8 IOP Slot Soft Failure Codes (Table 4-7) 283
4.4 Smart Transmitter Interface 285
4.5 FTA Redundancy Indicators 286
4.6 Redundant Analog Output IOP Failure Diagnosis 287
4.7 Battery Backup Exhaustion 290
4.8 HPMM Card and Module Indicators 290
4.9 HPMM Alphanumeric Display 294
4.9.1 Alphanumeric Display Format 295
4.9.2 Notification Displays 298
4.9.3 Cold HPMM Startup Display Sequences 299
4.9.4 Load Display Sequence 302
4.9.5 Nonredundant HPM Failure Sequences (After Load) 304
4.9.6 RAM Retention Startup Sequence 306
4.9.7 Redundancy Display Sequences 307
4.9.8 HPMM Alphanumeric Display Blanking 311
4.9.9 Listing of Diagnostic Tests 312
4.10 I/O Card Indicators 320
4.11 FTA Indicators 322
4.12 Power System Indicators 324
4.12.1 Standard Power System 324
4.12.2 AC Only Power System 327
4.13 Power System Voltage Checks 328
4.13.1 Standard Power System 328
4.13.2 AC Only Power System 331

SECTION 5 – UCN EXERCISER 333

5.1 Overview 333
5.2 Applications 334
5.3 Request Data Response (RDR) Test 335
5.4 Triangulation Test 336
5.5 Test Operation 337
5.6 Analyzing Results 344

Table of Contents

SECTION 6 – REMOVAL AND REPLACEMENT 345

6.1 Overview 345
6.2 Electrostatic Discharge Protection 346
6.2.1 ESD Guidelines for HPMM and IOP Cards 347
6.3 HPMM and IOP Cards 348
6.3.1 Removal and Replacement 348
6.3.2 Standby Manual Device Overview 350
6.3.3 AO Standby Manual Device Operation 353
6.3.4 DO Standby Manual Device Operation 359
6.3.5 HPMM or IOP Card Case Replacement 364
6.4 Field Termination Assembly 366
6.4.1 IOP to FTA Cable 366
6.4.2 FTA Replacement 367
6.4.3 FTA Module and Relay Replacement 368
6.5 Card File Replacement 369
6.6 Power System 370
6.6.1 CMOS Battery Replacement 370
6.6.2 48 V Backup Battery Replacement 371
6.6.3 Power Supply Module Replacement 376
6.6.4 CMOS Backup Assembly Replacement 377
6.7 Cabinet 377
6.8 I/O Link Extender Optical Coupler Module Replacement 378

SECTION 7 – IOP CALIBRATION PROCEDURES 379

7.1 Overview 379
7.2 LLAI, HLAI, and AO IOP Calibration 380
7.2.1 Common Calibration Procedures 380
7.2.2 Precision Test Equipment Required 380
7.2.3 LLAI IOP Calibration Procedure 381
7.2.4 Nonredundant HLAI IOP Calibration Procedure 388
7.2.5 Redundant HLAI IOP Calibration Procedure 391
7.2.6 Nonredundant AO IOP Calibration Procedure 393
7.2.7 Redundant AO IOP Calibration Procedure 395
7.2.8 LLMux IOP Calibration Procedure 397
7.3 Thermocouple Input Accuracy Verification 399

SECTION 8 – PERIODIC REDUNDANCY TESTS 401

8.1 Overview 401
8.2 HPMM Redundancy 402
8.3 IOP Redundancy 403
8.3.1 Redundant 8-Channel Analog Output IOPs 405
8.4 Power Cable Redundancy 407
8.5 Power Supply Module Redundancy 408

SECTION 9 – SPARE PARTS 409

9.1 Overview 409
9.2 Periodic Maintenance Parts 410
9.3 Optimum Replaceable Unit (ORU) Parts 413
9.4 UCN Parts 434

Figures

Figure 2-1 Cabinet Layout – HPM with Nonredundant HPMM 8
Figure 2-2 15-Slot HPMM Card File 11
Figure 2-3 HPM UCN Interface Module (Front Panel) 15
Figure 2-4 High-Performance Comm/Control Card (Front Panel) 16
Figure 2-5 High-Performance I/O Link Card (Front Panel) 17
Figure 2-6 15-Slot IOP Card File 19
Figure 2-7 HLAI FTA with Redundant HLAI IOPs 21
Figure 2-8 Analog Output FTA with Redundant Analog Output IOPs 22
Figure 2-9 Low Level Multiplexer Interconnections 23
Figure 2-10 Serial Device Interface Interconnections 26
Figure 2-11 Model MU-TSIM12 Serial Interface FTA Interconnections 30
Figure 2-12 Standard I/O Link Extender Interconnections with Nonredundant HPMM 34
Figure 2-13 Standard I/O Link Extender Interconnections with Redundant HPMMs 35
Figure 2-14 Long Distance I/O Link Extender Interconnections with Nonredundant HPMM 36
Figure 2-15 Long Distance I/O Link Extender Interconnections with Redundant HPMMs 37
Figure 2-16 Field Termination Assembly (FTA) Sizes 41
Figure 2-17 Typical Vertical FTA Mounting Channel Layout 43
Figure 2-18 Typical FTA Compression Terminal Connector 44
Figure 2-19 Typical FTA Fixed Screw Terminal Connector 45
Figure 2-20 Typical FTA Removable Screw Terminal Connector 45
Figure 2-21 Crimp-Type Galvanic Isolation Module Terminal Connector 46
Figure 2-22 Compression-Type Galvanic Isolation Module 47
Figure 2-23 Vertical FTA Mounting Channel Installation – Dual Access Cabinet 49
Figure 2-24 Vertical FTA Mounting Channel Installation – Single Access Cabinet 50
Figure 2-25 Standard Power System 53
Figure 2-26 HPM Standard Power System 54
Figure 2-27 AC Only Power System 56
Figure 2-28 Power Distribution 57
Figure 2-29 Standard Power System Backplane (Early Production) 58
Figure 2-30 HPM Standard Power System Backplane 59
Figure 2-31 CMOS Battery Backup Assembly (Early Production) 60
Figure 2-32 CMOS Battery Backup Assembly 61
Figure 2-33 Typical Cabinet 24 Vdc Power Distribution 62
Figure 2-34 Left 7-Slot HPMM Card File Backplane 24 Vdc Distribution 66
Figure 2-35 Left 7-Slot IOP Card File Backplane 24 Vdc Distribution 67
Figure 2-36 Left 7-Slot Card File Backplane Fuse Locations 68
Figure 2-37 Right 7-Slot HPMM Card File Backplane 24 Vdc 70
Figure 2-38 Right 7-Slot IOP Card File Backplane 24 Vdc Distribution 71
Figure 2-39 Right 7-Slot Card File Backplane Fuse Locations 72
Figure 2-40 15-Slot HPMM Card File Backplane 24 Vdc Distribution 74
Figure 2-41 15-Slot IOP Card File Backplane 24 Vdc Distribution 75
Figure 2-42 15-Slot Card File Backplane Fuse Locations 76
Figure 2-43 IOP Only Card File Backplane 24 Vdc Power Distribution 78
Figure 2-44 IOP Only Card File Backplane Fuse Locations 79
Figure 2-45 HPMM Power Routing and Fuses 81
Figure 2-46 Typical Standard Power System Power Cabling – 15-Slot Card File with Power Distribution Assemblies 83
Figure 2-47 Typical Standard Power System Power Cabling – Two 15-Slot Card File with Power Distribution Assemblies 84
Figure 2-48 Typical Standard Power System Power Cabling – Three 15-Slot Card File 85
Figure 2-49 Typical Standard Power System Power Cabling – Three 15-Slot Card File with Power Distribution Assemblies 86

Figures

Figure 2-50 Typical Early Production Power System Cabling – Three 15-Slot Card Files with Power Distribution Assemblies 87
Figure 2-51 I/O Link Interface Cabling – Three Card Files 89
Figure 2-52 I/O Link Interface Cabling – Four Card Files 90
Figure 2-53 IOP to FTA Cabinet Cabling 93
Figure 2-54 Power Adapter Interconnections – LLMux Application..... 94
Figure 2-55 Power Adapter Interconnections – SDI Application..... 95
Figure 2-56 Power Adapter Interconnections – SI Application..... 96
Figure 2-57 Universal Control Network (UCN) Components..... 97
Figure 2-58 UCN Taps..... 98
Figure 2-59 UCN Drop Cable Connections to a 7-Slot HPMM Card File..... 99
Figure 2-60 Left 7-Slot Card File UCN Node Address Pinning..... 101
Figure 2-61 15-Slot Card File UCN Node Address Pinning..... 102
Figure 2-62 UCN Node Address Pinning Using Plug Jumpers..... 103
Figure 2-63 UCN Node Address Pinning Using Zero-Ohm Resistors 104
Figure 2-64 Left 7-Slot Card File I/O Link Interface Address Pinning 106
Figure 2-65 15-Slot Card File I/O Link Interface Address Pinning..... 107
Figure 2-66 IOP Only Card File I/O Link Interface Address Pinning..... 108
Figure 2-67 Left 7-Slot Card File I/O Link Interface Address Pinning with Plug Jumpers..... 109
Figure 2-68 Left 7-Slot Card File I/O Link Interface Address Pinning with Zero-Ohm Resistors 110
Figure 3-1 System Status Display..... 117
Figure 3-2 UCN Status Display 117
Figure 3-3 NIM Detail Status Display..... 118
Figure 3-4 HPM Status Display..... 119
Figure 3-5 Primary HPMM Detail Status Display..... 120
Figure 3-6 Secondary HPMM Detail Status Display 120
Figure 3-7 IOP Detail Status Display..... 121
Figure 3-8 UCN Status Display 122
Figure 3-9 UCN Status Display – LOAD/SAVE RESTORE Target Selected..... 127
Figure 3-10 UCN Status Display – CONTROL STATES Target Selected..... 129
Figure 3-11 UCN Status Display – AUTO CHECKPT Target Selected 131
Figure 3-12 UCN Status Display – UCN CABLE STATUS..... 133
Figure 3-13 UCN Status Display – NIM Node and UCN CABLE STATUS Targets Selected 134
Figure 3-14 UCN Status Display – HPM Node and UCN CABLE STATUS Targets Selected 135
Figure 3-15 UCN Network Statistics Display..... 138
Figure 3-16 UCN Network Statistics Display – UCN Node Selected..... 138
Figure 3-17 UCN Status Display – RUN STATES Target Selected 140
Figure 3-18 UCN Status Display – SLOT SUMMARY Target Selected..... 142
Figure 3-19 UCN Status Display – REGULATORY CONTROL Target Selected..... 143
Figure 3-20 HPM Status Display..... 144
Figure 3-21 HPM Status Display – LOAD/SAVE RESTORE Target Selected 151
Figure 3-22 HPM Status Display – CONTROL STATES Target Selected..... 153
Figure 3-23 HPM Status Display – AUTO CHECKPT Target Selected..... 154
Figure 3-24 HPM Status Display – IOL CABLE COMMANDS Target Selected 155
Figure 3-25 HPM Status Display – RUN STATES Target Selected..... 157
Figure 3-26 HPM Status Display – SLOT SUMMARY Target Selected..... 159
Figure 3-27 HPM Status Display – REGULATORY CONTROL POINTS Target Selected..... 160
Figure 3-28 NIM Driver Configuration Display..... 161
Figure 3-29 NIM Local UCN Statistics Display – Page 1..... 164
Figure 3-30 NIM Local UCN Statistics Display – Page 2..... 164
Figure 3-31 Primary HPMM Detail Status Display..... 166
Figure 3-32 Secondary HPMM Detail Status Display 167
Figure 3-33 Primary HPMM I/O Link Information Display..... 169

Figures

Figure 3-34 Secondary HPMM I/O Link Information Display 170
Figure 3-35 IOM I/O Link Information Display 173
Figure 3-36 HPMM Version/Revision Display 175
Figure 3-37 HPMM Control Configuration Display 177
Figure 3-38 HPM Write Lockout Control Display 180
Figure 3-39 HPM Write Lockout Control Display – Improper US Keylock Position .. 181
Figure 3-40 HPM Write Lockout Control Help Display 182
Figure 3-41 HPMM Schedule Information Display 183
Figure 3-42 HPMM UCN Statistics Display – Page 1 186
Figure 3-43 HPMM UCN Statistics Display – Page 2 186
Figure 3-44 HPMM Communications Error Block Display 187
Figure 3-45 HPMM Control Block Display 188
Figure 3-46 HPMM Control Patches Display 189
Figure 3-47 HPMM Communications Patches Display 190
Figure 3-48 HPMM Node Status Information Display 191
Figure 3-49 Manufacturing Information Display 193
Figure 3-50 HPMM Soft Failure Display 194
Figure 3-51 HPMM Soft Failure Display – 00-39 195
Figure 3-52 HPMM Soft Failure Display – 40-79 195
Figure 3-53 HPMM Soft Failure Display – 80-95 196
Figure 3-54 HLAI IOP Detail Status Display 197
Figure 3-55 IOP Box Soft Failures Display 201
Figure 3-56 IOP Box Soft Failures Display – Page 1 202
Figure 3-57 IOP Box Soft Failures Display – Page 2 202
Figure 3-58 IOP Box Soft Failures Display – Page 3 203
Figure 3-59 IOP Box Soft Failures Display – Page 4 203
Figure 3-60 IOP Box Soft Failures Display – Page 5 204
Figure 3-61 IOP Slot Soft Failures Display 205
Figure 3-62 IOP Slot Soft Failures Display – Page 1 206
Figure 3-63 IOP Slot Soft Failures Display – Page 2 206
Figure 3-64 IOP Slot Soft Failures Display – Page 3 207
Figure 3-65 IOP Slots with Soft Failures Display 208
Figure 3-66 High Level Analog Input IOP Detail Status Display – ENABLE CALIBRATN Target Selected 209
Figure 3-67 High Level Analog Input IOP Detail Status Display – DISABLE CALIBRATN Target Selected 210
Figure 3-68 Low Level Analog Input IOP Detail Status Display – ENABLE CALIBRATN and ENABLE RJ CALIBR Target 211
Figure 3-69 Low Level Analog Input IOP Detail Status Display – DISABLE CALIBRATN Target Selected 212
Figure 3-70 Low Level Analog Input IOP Detail Status Display – DISABLE RJ CALIBR Target Selected 213
Figure 3-71 Low Level Analog Input IOP Detail Status Display 214
Figure 3-72 8-Channel Analog Output IOP Detail Status Display 216
Figure 3-73 16-Channel Analog Output IOP Detail Status Display 217
Figure 3-74 Analog Output IOP Detail Status Display – ENABLE CALIBRATN Target Selected 218
Figure 3-75 Analog Output IOP Detail Status Display – DISABLE CALIBRATN Target Selected 219
Figure 3-76 LLMux IOP Detail Status Display – ENABLE CAL ON Target Selected 220
Figure 3-77 LLMux IOP Display – DISABLE CALIBRATN Target Selected 221
Figure 3-78 Low Level Multiplexer IOP Detail Status Display 222
Figure 3-79 Digital Input IOP Detail Status Display 223
Figure 3-80 16-Channel Digital Output IOP Detail Status Display 224
Figure 3-81 32-Channel Digital Output IOP Detail Status Display 225
Figure 3-82 Smart Transmitter Interface IOP Detail Status Display 226
Figure 3-83 Pulse Input IOP Detail Status Display 227

Figures

Figure 3-84 Serial Device Interface IOP Detail Status Display 228
Figure 3-85 Serial Interface IOP Detail Status Display 229
Figure 3-86 Digital Input Sequence of Events IOP Detail Status Display 230
Figure 4-1 HPM Fault Isolation Flowchart (Sheet 1 of 6) 237
Figure 4-2 HPM Fault Isolation Flowchart (Sheet 2 of 6) 238
Figure 4-3 HPM Fault Isolation Flowchart (Sheet 3 of 6) 239
Figure 4-4 HPM Fault Isolation Flowchart (Sheet 4 of 6) 240
Figure 4-5 HPM Fault Isolation Flowchart (Sheet 5 of 6) 241
Figure 4-6 HPM Fault Isolation Flowchart (Sheet 6 of 6) 242
Figure 4-7 Standard Power System Indicators 324
Figure 4-8 Standard Power System Annunciator Contact Connections 326
Figure 4-9 Power System Power Output Connector Pin Assignments 329
Figure 4-10 Power Supply Module Test Points and Indicators 329
Figure 4-11 Power System AC Wiring 330
Figure 5-1 RDR Test Configuration 335
Figure 5-2 Triangulation Test 336
Figure 5-3 UCN Exerciser Overview Display – Page 1 338
Figure 5-4 UCN Exerciser Overview Display – Page 2 338
Figure 5-5 UCN Exerciser Help Display 339
Figure 5-6 Connection Test Summary Display – Page 1 340
Figure 5-7 Connect Test Summary Display – Page 2 341
Figure 5-8 Connection Test Detail Display 344
Figure 6-1 Cabinet ESD Wriststrap Connection 346
Figure 6-2 HPM UCN Interface Module Installation 350
Figure 6-3 Digital Output Manual Device Interconnection 351
Figure 6-4 Original Analog Output Standby Manual Device 353
Figure 6-5 Compact Analog Output Standby Manual Device 355
Figure 6-6 Model MU-SMDC02 Portable Digital Output Standby Manual Device . 359
Figure 6-7 Digital Standby Manual Device Panel 361
Figure 6-8 Replacing HPMM or IOP Card Case 365
Figure 7-1 Zero Calibration Circuit – TC and All Linear Zero Circuits 382
Figure 7-2 Zero Calibration Circuit – RTD Zero Cu: 10 Ohm, Pt: 100 Ohm, Ni: 120 Ohm 382
Figure 7-3 LLAI FTA Showing DS1 Status Indicator and Calibration Pads 383
Figure 7-4 Full Scale Calibration Circuit – TC and All Linear Full Scale Circuits 384
Figure 7-5 Full Scale Calibration Circuit – RTD Full Scale Cu: 10 Ohm, Pt: 100 Ohm, Ni: 120 Ohm 385
Figure 7-6 RJ Calibration Circuit – RJ Zero 386
Figure 7-7 RJ Calibration Circuit – RJ Full Scale 386
Figure 7-8 Galvanic Isolation HLAI Calibration Tool (51201450) 389
Figure 7-9 Nonredundant HLAI Calibration Connections 390
Figure 7-10 Redundant HLAI Calibration Connections 392
Figure 7-11 Nonredundant AO Calibration FTA Connections 394
Figure 7-12 Redundant Analog Output Calibration Connections 396
Figure 7-13 LLMux FTA Calibration Connections 398

Tables

Table 2-1 Card File Models 9
Table 2-2 HPMM Card/Module Types 12
Table 2-3 Standard Field Termination Assembly Types 39
Table 2-4 Galvanically Isolated Field Termination Assembly Types 40
Table 2-5 Left 7-Slot Card File Fuse Protection 65
Table 2-6 Right 7-Slot Card File Backplane Fuse Protection 69
Table 2-7 15-Slot Card File Backplane Fuse Protection 73
Table 2-8 IOP Only Card File Fuse Protection 77
Table 2-9 Card File Power Cabling 82
Table 2-10 I/O Link Interface Cabling Card File Connector Assignments 88
Table 3-1 UCN Status Display – UCN/NIM Status 123
Table 3-2 UCN Status Display – Primary HPMM Status 125
Table 3-3 UCN Status Display – Secondary HPMM Status 126
Table 3-4 UCN Status Display – LOAD/SAVE RESTORE Target Selected 128
Table 3-5 UCN Status Display – CONTROL STATES Target Selected 130
Table 3-6 UCN Status Display – AUTO CHECKPT Target Selected 132
Table 3-7 UCN Status Display – UCN CABLE STATUS Target Selected 135
Table 3-8 UCN Network Statistics Display Definitions 139
Table 3-9 UCN Status Display – RUN STATES Target Selected 141
Table 3-10 HPM Status Display – UCN and HPM Status 145
Table 3-11 HPM Status Display – Primary HPMM Status 147
Table 3-12 HPM Status Display Definitions – Secondary HPMM Status 148
Table 3-13 HPM Status Display – IOP A Status 149
Table 3-14 HPM Status Display – IOP B Status 150
Table 3-15 HPM Status Display – LOAD/SAVE RESTORE Target Selected 152
Table 3-16 HPM Status Display – CONTROL STATES Target Selected 153
Table 3-17 HPM Status Display – AUTO CHECKPT Target Selected 154
Table 3-18 HPM Status Display – IOL CABLE COMMANDS Target Selected 156
Table 3-19 HPM Status Display – RUN STATES Target Selected 158
Table 3-20 NIM Driver Configuration Display 162
Table 3-21 HPMM Detail Status Display 168
Table 3-22 HPMM I/O Link Information Display 171
Table 3-23 IOM I/O Link Information Display 174
Table 3-24 HPMM Version/Revision Display 176
Table 3-25 HPMM Control Configuration Display 178
Table 3-26 HPMM Schedule Overrun Counters Statistics 179
Table 3-27 Performance Statistics 185
Table 3-28 HPMM Node Status Information Display 192
Table 3-29 IOP Detail Status Display – IOP Configuration 198
Table 3-30 IOP Detail Status Display – I/O Link Cable Status/Statistics 199
Table 3-31 IOP Detail Status Display – I/O Link Cable Status Messages 199
Table 3-32 Low Level Analog Input IOP Detail Status Display 215
Table 4-1 HPMM Corrective Actions 243
Table 4-2 Communications and Control Processor Hard Failure Codes 245
Table 4-3 Comm/Control Soft Failure Error Codes 269
Table 4-4 I/O Link Hard Failure Error Codes 273
Table 4-5 IOP Hard Failure Error Codes 275
Table 4-6 IOP Box Soft Failure Error Codes 277
Table 4-7 IOP Slot Soft Failure Error Codes 283
Table 4-8 Two-Wire Link/Smart Transmitter Fault Isolation Procedure 285
Table 4-9 Switching Module Replacement Procedure 289
Table 4-10 HPMM Card and Module Indicators 291
Table 4-11 Alphanumeric Display Formats 296
Table 4-12 User Notification Message Formats 298
Table 4-13 Alphanumeric Display for a Normal Startup Sequence 299
Table 4-14 Alphanumeric Display for Startup/Factory Test Mode 300
Table 4-15 Alphanumeric Display for HPMM Cold Startup Failure Sequence 301
Table 4-16 Alphanumeric Display for Load Sequence 302

Tables

Table 4-17	Communications/I/O Link Processor Failure Display Sequence	304
Table 4-18	Control Processor Failure Display Sequence	305
Table 4-19	RAM Retention Startup Display Sequence	306
Table 4-20	Alphanumeric Display for HPMM Swapping Sequence (Detailed Display Mode)	307
Table 4-21	Alphanumeric Display for HPMM Swapping Sequence (Non-Detailed Display Mode)	308
Table 4-22	Alphanumeric Display for Failover HPMM Swapping Sequence (Detailed Display Mode)	309
Table 4-23	Alphanumeric Display for Failover HPMM Swapping Sequence (Non-Detailed Display Mode)	310
Table 4-24	Diagnostic Test Listing	312
Table 4-25	IOP Card Indicators	320
Table 4-26	IOP Multicolor Status Indicator	321
Table 4-27	FTA Indicators	322
Table 4-28	Standard Power System Voltage Test Points	328
Table 4-29	AC Only Power System Voltage Test Points	331
Table 5-1	UCN Exerciser Test Procedure	342
Table 7-1	Typical Precision Test Equipment	380
Table 7-2	Galvanically Isolated HLAI Calibration Connector Pins	388
Table 9-1	HPM Periodic Maintenance Parts	410
Table 9-2	Non-Conformally Coated HPM ORU Parts List	413
Table 9-3	Conformally Coated HPM ORU Parts List	426
Table 9-4	UCN Parts List	434

Acronyms

AC ..... Alternating Current
AO ..... Analog Output
APM ..... Advanced Process Manager
CMOS ..... Complementary Metal-Oxide Semiconductor
CPU ..... Central Processing Unit
dB ..... Decibel
DISOE ..... Digital Input Sequence of Events
DI ..... Digital Input
DMA ..... Direct Memory Access
DO ..... Digital Output
DRAM ..... Dynamic Random Access Memory
EDAC ..... Error Detect And Correct
EEPROM ..... Electrically Erasable Programmable Read-Only Memory
EPROM ..... Electrically Programmable Read-Only Memory
FTA ..... Field Termination Assembly
HLAI ..... High Level Analog Input
HPMM ..... High-Performance Process Manager Module
HPM ..... High-Performance Process Manager
I/O ..... Input/Output
ID ..... Identification
IEEE ..... Institute of Electrical and Electronic Engineering
IOL ..... I/O Link
IOM ..... Input /Output Module
IOP ..... Input/Output Processor
LCN ..... Local Control Network
LED ..... Light Emitting Diode
LLAI ..... Low Level Analog Input
LLC ..... Logical Link Control
LM ..... Logic Manager
MAC ..... Media Access Control
MAP ..... Manufacturing Automation Protocol
Mbps ..... Megabits Per Second
NIM ..... Network Interface Module
ORU ..... Optimum Replaceable Unit
PI ..... Pulse Input
PM ..... Process Manager
PPX ..... Point Processing Execution
PSM ..... Power Supply Module
RTU ..... Remote Terminal Unit
SAP ..... Service Access Point
SBU ..... Startup and Base Utilities
SRAM ..... Static Random Access Memory
STI ..... Smart Transmitter Interface
TBC ..... Token Bus Controller
UCN ..... Universal Control Network
UM51 ..... I/O Link 8031 Processor
US ..... Universal Station
WDT ..... Watch Dog Timer

References

Publication Title	Publication Number	Binder Title	Binder Number
High-Performance Process Manager Specification and Technical Data	HP03-500	System Summary - 2	TDC 3010-2
High-Performance Process Manager Planning	HP02-500	System Site Planning - 2	TDC 3020-2
High-Performance Process Manager Installation	HP20-500	Implementation/ High-Performance Process Manager - 3	TDC 3066-3
High-Performance Process Manager Checkout	HP20-510	Implementation/ High-Performance Process Manager - 3	TDC 3066-3
Process Manager I/O Specification and Technical Data	IO03-500	System Summary - 2	TDC 3010-2
TDC 3000^X System Site Planning	SW02-550	System Site Planning - 1	TDC 3020-1
Universal Control Network Specification and Technical Data	UN03-500	System Summary - 2	TDC 3010-2
Universal Control Network Planning	UN02-501	System Site Planning - 1	TDC 3020-1
Universal Control Network Installation	UN20-500	Installation/Universal Control Network	TDC 3041
Universal Control Network Guidelines	UN12-510	Installation/Universal Control Network	TDC 3041
Local Control Network Planning	SW02-501	System Site Planning - 1	TDC 3020-1
LCN System Installation	SW20-500	LCN Installation	TDC 3025
LCN System Checkout	SW20-510	LCN Installation	TDC 3025
LCN Guidelines - Implementation, Troubleshooting, and Service	LC09-510	LCN Installation	TDC 3025

Section 1 – Introduction

1.1 Overview

Section contents

The topics covered in this section are:

	Topic	See Page
1.1	Overview	1
1.2	Purpose of this Manual	1

Introduction

This section describes the purpose of this manual and lists all available manuals that may be required when servicing the High-Performance Process Manager.

1.2 Purpose of this Manual

Service philosophy

The *High-Performance Process Manager Service* manual provides instructions for servicing the High-Performance Process Manager (HPM). The instructions consist of fault isolation and removal/replacement procedures at the Optimum Replaceable Unit (ORU) parts level. In addition, an ORU parts lists for current production hardware is provided.

Section 2 – Equipment Description

2.1 Overview

Section contents

The topics covered in this section are:

	Topic	See Page
2.1	Overview	3
2.2	Power System Controls	4
2.2.1	Power Supply Module Control	4
2.2.2	HPMM/IOP Card Power Interrupt Switches	5
2.3	HPM Subsystem Overview	6
2.4	HPMM and IOP Card Files	9
2.5	HPMM Card Files	10
2.5.1	HPMM Description	12
2.6	IOP Card Files	18
2.6.1	IOPs	20
2.6.2	Redundant IOPs	21
2.6.3	Low Level Multiplexer IOP (LLMux)	23
2.6.4	Serial Device Interface IOP (SDI)	25
2.6.5	Serial Interface IOP (SI)	29
2.6	I/O Link Extender (Fiber Optic Link)	32
2.7	Field Termination Assembly	38
2.8	FTA Mounting Channels	48
2.9	Power Systems	51
2.9.1	Power Distribution	57
2.9.2	Battery Backup Module	58
2.9.3	CMOS Battery Backup	60
2.9.4	24 Vdc Power Distribution	62
2.9.5	Cabinet Fan Assembly	63
2.9.6	LLAI Line Frequency Clock Voltage	63
2.9.7	24 Vdc Fuse Protection	64
2.9.8	5 Vdc Fuse Protection	81
2.9.9	Card File Power Cabling	82
2.10	I/O Link Interface Cabling	88
2.11	IOP to FTA Cabling	92
2.12	Power Adapter Cabling	94
2.13	UCN Cable System	97
2.14	UCN Node Address Pinning	100
2.15	I/O Link Interface Address Pinning	105
2.16	Firmware/Hardware/Software Correlation	111

Introduction

This section describes the assemblies that comprise the High-Performance Process Manager (HPM) subsystem which is a node on the Universal Control Network (UCN). The UCN interfaces with the Local Control Network (LCN) through a Network Interface Module (NIM). The modules (nodes) on the LCN comprise the TDC 3000^X system.

Component part numbers

The Honeywell part numbers for the items described in this section are listed in Section 9.

2.2 Power System Controls

2.2.1 Power Supply Module Control

Two methods of power controlling power

Control of ac power to the Power Supply Modules is provided by two methods when the High-Performance Process Manager cabinet contains the normal Standard Power System components.

AC power control

All ac power to the cabinet, which includes any Cabinet Fan assemblies, is controlled by a dedicated circuit breaker that is supplied by the user for each Power Supply Module in the Power System. Additional ac Power Supply Module control is provided by a power switch that is mounted at the front of each module.

DC power control

Since the Standard Power System can contain redundant Power Supply Modules, placing a module's power switch in the off position does not necessarily remove power from the card files and FTAs in the cabinet because the second module will continue to supply power unless its Power switch is in the off position.

If the Standard Power System contains a Battery Backup Pack, 24 Vdc power will continue to be supplied to the card files and FTAs unless the **BATTERY** switch is placed in the off position, or the Battery Backup Pack is discharged. All three switches must be in the off position to completely remove power from the card files.

AC Only Power System

In a cabinet that contains an AC Only Power System, no Battery Backup Pack exists to provide 24 Vdc power to the card files and FTAs, so control of dc power to the card files and FTAs is provided exclusively by user supplied ac circuit breakers. When redundant Power Supply Modules exist, each module has its own circuit breaker that is provided by the user. There is no on-off switch at the front of the Power Supply Module.

2.2.2 HPMM/IOP Card Power Interrupt Switches

24 Vdc power interruption

The HPMM High-Performance Comm/Control and High-Performance I/O Link cards, and each IOP card have a 24 Vdc power interrupt switch that is activated by unlocking and lifting the upper card extractor/insertion lever. Activating either HPMM card's interrupt switch removes power from both HPMM cards and the HPM UCN Interface module in the card file, while activating an IOP card power interrupt switch removes power only from that IOP card. Power is removed only while the switch is activated.

WARNING

WARNING—The loss of power to an analog or digital output IOP causes the loss of the IOP's outputs to the field connections. Analog output IOP outputs drop to a nonpowered state (-6.9%), and the digital output IOP outputs are set to their off state.

The nonpowered state of the output IOPs should result in a safe condition for personnel, the plant, and the process under control.

2.3 HPM Subsystem Overview

Major assemblies

The High-Performance Process Manager subsystem (HPM) is comprised of the major assemblies that are described in the following subsections. Figure 2-1 is a view of a single cabinet containing a nonredundant HPMM and identifies some of the High-Performance Process Manager assemblies. The High-Performance Process Manager major assemblies are:

- Left 7-Slot Card File (Slots 1 through 7)
- Right 7-Slot Card File (Slots 9 through 15)
- 15-Slot Card File
- IOP Only Card File (in PM/APM upgraded cabinets)
- Input/Output Processors (IOPs)
- Field Termination Assemblies (FTAs)
- Power Systems

Card file types

Three types of card files can accommodate both High-Performance Process Manager Module (HPMM) and Input/Output Processor (IOP) cards, or may have IOP cards only. The HPMM card set occupies slots 1 and 2 in both the Left 7-Slot and 15-Slot card files. The HPMM card set occupies slots 9 and 10 in the Right 7-Slot card file. All card slots accept IOPs.

An older “IOP Only” card file may exist in a HPM cabinet that was upgraded to an HPM from a PM or APM. This older card file cannot support an HPMM card set. It is restricted to IOP cards and optional I/O Link Extender cards.

Card file designations

When a card file contains an HPMM card set, it is designated an HPMM card file. If the card file contains only IOP cards, the card file is designated 7-Slot or 15-Slot IOP card file. A card file can accommodate only one HPMM card set. A second HPMM card file must be added for HPMM redundancy.

Nonredundant 15-Slot HPMM card file

When configuring an HPM with a nonredundant HPMM by using a 15-Slot card file, the HPMM card file is typically installed in the bottom card file position of the cabinet.

Redundant 15-Slot HPMM card files

If an HPM is configured with redundant HPMMs by using 15-Slot card files, HPMM card files are installed in the bottom two card file positions in the cabinet. A redundancy cable is connected between the HPMM card files.

Continued on next page

Nonredundant 7-Slot HPMM card file

When configuring an HPM with a nonredundant HPMM by using a 7-Slot card file, the HPMM card set are typically installed in a Left 7-Slot card file.

Redundant 7-Slot HPMM card files

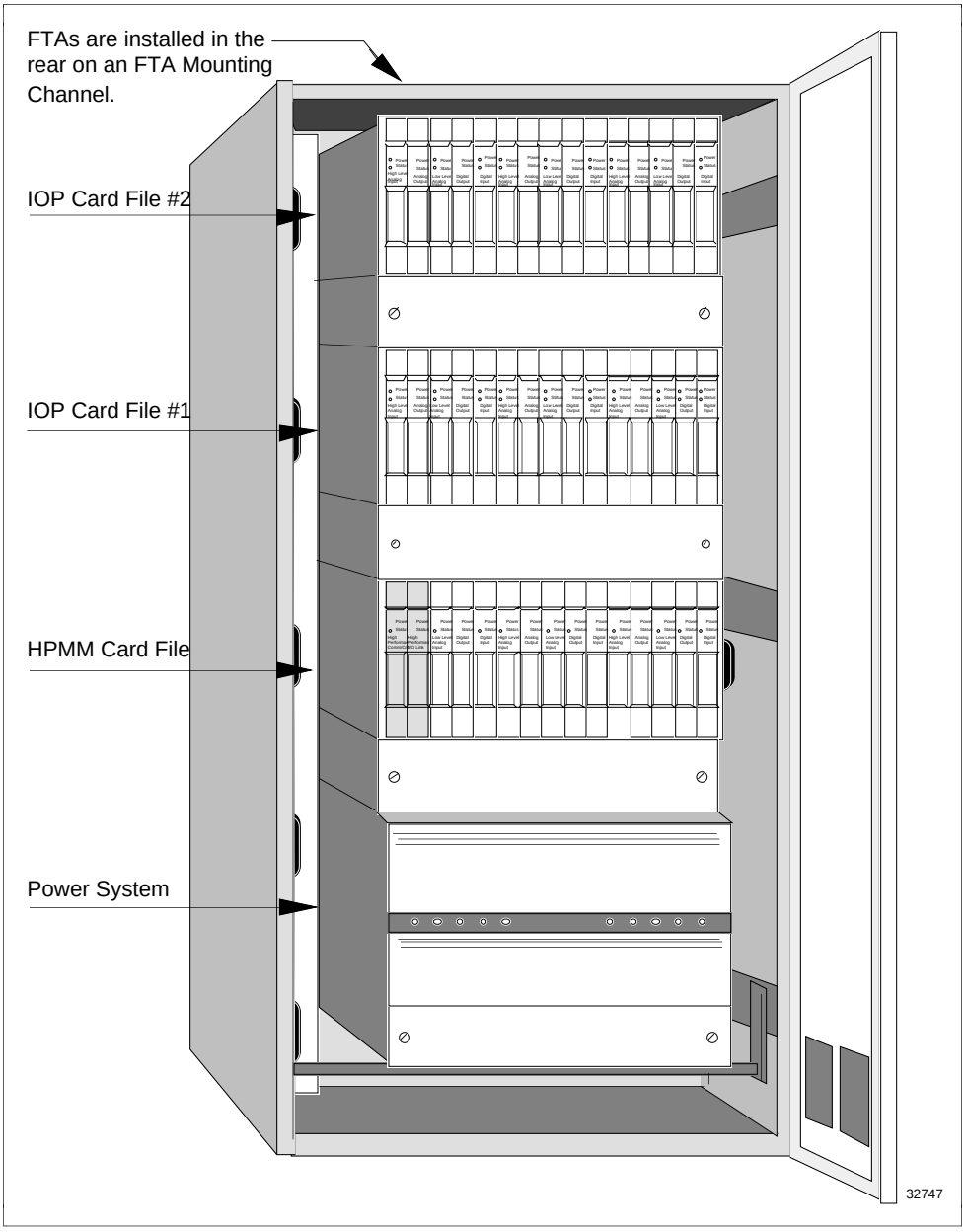
If an HPM is configured with redundant HPMMs using 7-Slot card files, HPMM card sets are installed in both a Left 7-Slot card file and in a Right 7-Slot card file. The card files are normally mounted side-by-side in the bottom card file position of the cabinet. A redundancy cable is connected between the HPMM card files.

Continued on next page

Nonredundant HPMM cabinet layout

Figure 2-1 is an illustration of an HPM cabinet that contains a nonredundant HPMM that is installed in left most card slots of the lower 15-Slot card file. IOPs are installed in the remaining slots of the lower card file and the 15-Slot card files above.

Figure 2-1 Cabinet Layout – HPM with Nonredundant HPMM



2.4 HPMM and IOP Card Files

Introduction

There are nine (9) card file models. Three models are not CE Compliant and six models are CE Compliant. Table 2-1 lists the nine card file models. All models are also available with conformal coating (a model number with a prefix of MC, rather than MU).

Table 2-1 Card File Models

Card File Description	CE Compliant	Non-CE Compliant
Left 7-Slot HPMM or IOP	N/A	MU-HPFH01
Right 7-Slot HPMM or IOP	N/A	MU-HPFH11
15-Slot HPMM or IOP	N/A	MU-HPFX02
Left 7-Slot HPMM	MU-HPFH03	N/A
Right 7-Slot HPMM	MU-HPFH13	N/A
15-Slot HPMM	MU-HPFX03	N/A
Left 7-Slot IOP	MU-HPFI03	N/A
Right 7-Slot IOP	MU-HPFI13	N/A
15-Slot IOP	MU-HPFI23	N/A

HPMM and IOP card file differences

An HPMM card file and IOP card file differ only in the application. Electrically, their backplanes are the same.

Non-CE Compliant card file models

The non-CE Compliant card file models can be designated as an HPMM card file or an IOP card file by either installing an HPMM card set in the the two left-most card slots or installing IOP cards.

CE Compliant card file models

Unlike the non-CE Compliant card file models, the CE Compliant card file models are designated either an HPMM card file or an IOP card file because even though their is no electrical difference in the backplane, they differ mechanically. The addition of a ground plate and filtered IOP connectors in the two left-most slots prohibits the installation of an HPMM card set.

The card file is designated an IOP card file when the ground plate and filtered connectors are present.

The card file is designated an HPMM card file when the ground plate and filtered connectors are absent.

Conversion kit

A CE Compliant HPMM card file can be converted to an IOP card file with a model MU-ZPFI03 upgrade kit. The kit adds 2 filtered IOP adapter connectors to the two left-most card slots and a ground plate extension.

2.5 HPMM Card Files

Introduction

A High-Performance Process Manager (HPMM) card file is a 7-Slot or 15-Slot card file that is populated with an HPMM card set. The HPMM card set consists of following assemblies.

- High-Performance Comm/Control card
- High-Performance I/O Link card
- HPM UCN Interface module

The HPMM assemblies occupy the two left-most slot positions in the card file. The HPM UCN Interface module mounts in the connector beneath the High-Performance Comm/Control card in the first slot.

Three HPMM card file configurations

There are 3 HPMM card file configurations. They are as follows.

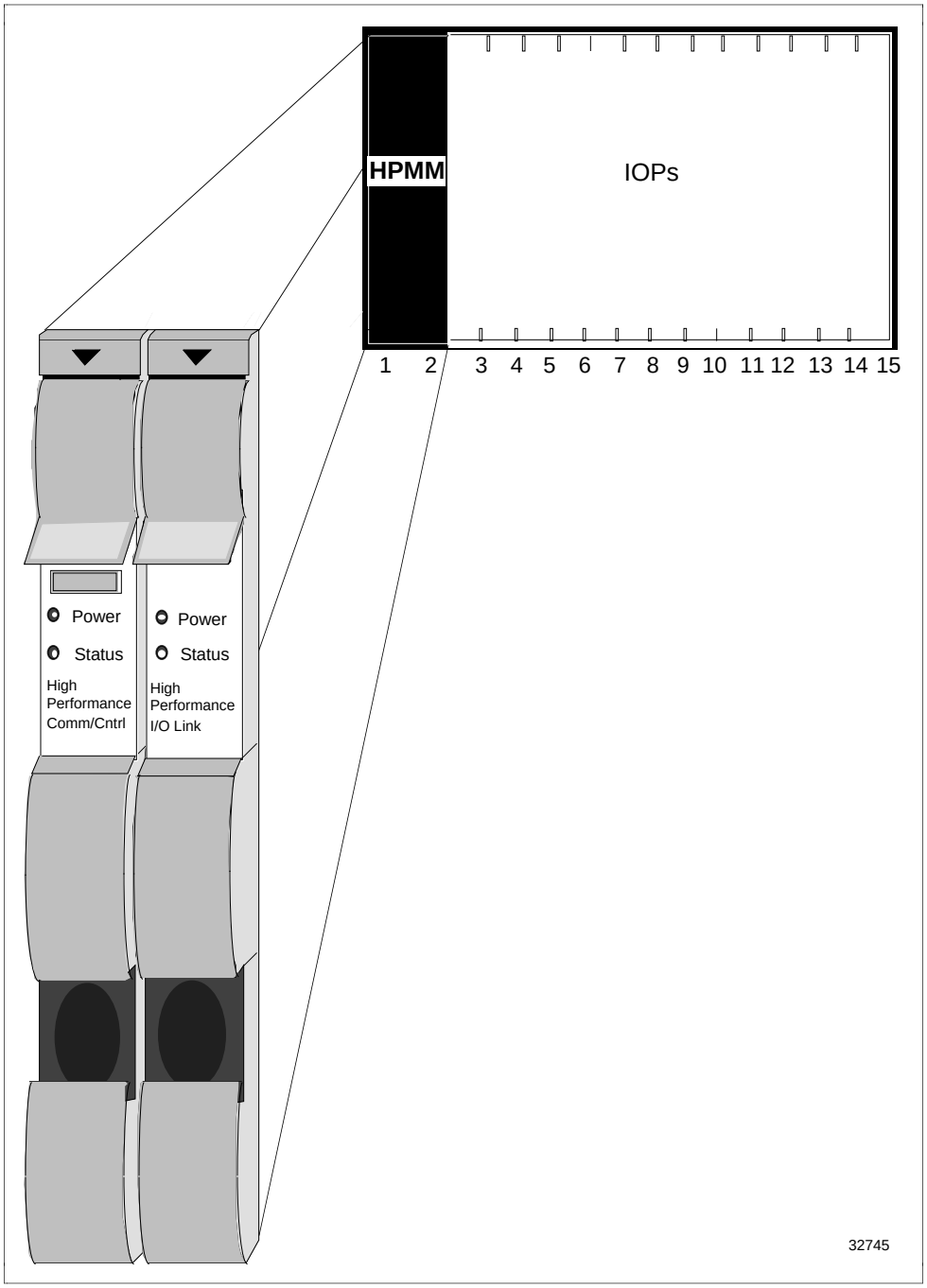
- Left 7-Slot HPMM card file
- Right 7-Slot HPMM card file
- 15-Slot HPMM card file

Continued on next page

15-Slot HPMM card file illustration

Figure 2-2 is an illustration of a 15-Slot HPMM card file.

Figure 2-2 15-Slot HPMM Card File



2.5.1 HPMM Description

HPMM functionality

The High-Performance Process Manager Module (HPMM) provides:

- Communications with the Local Control Network (LCN) Network Interface Module (NIM) through the Universal Control Network (UCN)
- A Communications processor (Motorola 68LC040)
- Communications through the I/O Link Interface with Input/Output Processors (IOPs) and I/O Link Extenders
- A Control processor (Motorola 68040)
- Separate and shared memory for the Communications and Control processors
- An I/O Link processor (Motorola 80C32) with SRAM
- HPMM redundancy control

HPMM card/module types

The HPMM is composed of two card types and a UCN interface module that mounts in the 50-pin connector below the High-Performance Communications/Control card in the first left-most card file slot. The cards and the module are described in Table 2-2.

Table 2-2 HPMM Card/Module Types

Card/Module Type	Function
High-Performance Comm/Control Card	Consists of a Communications (Comm) processor, Control processor (Control), separate and shared RAM for the processors, interface to the HPMM Global bus on the backplane, TBC interface to the HPM UCN Interface module, redundancy interface to another HPMM, and front panel LEDs and a four character alphanumeric diagnostic display.
High-Performance I/O Link Card	Consists of an I/O Link processor, SRAM through which the processor communicates with the Communications/Control card, an I/O Link driver/receiver interface, and a +24 Vdc to +5 Vdc power converter that provides +5 Vdc for both HPMM cards and the HPM UCN Interface module.
HPM UCN Interface Module	Consists of 5 Mbps IEEE 802.4 compatible MAP carrier band modulator/demodulator circuitry that provides the interface with the Universal Control Network (UCN). Logically provides redundant UCN cable selection (transmit on both, receive on the selected cable) through redundant UCN cable driver/receivers.

Continued on next page

CAUTION

CAUTION—It is important that you wear a properly connected Electrostatic Discharge (ESD) wriststrap while touching or handling HPM components.

Card/module illustrations

Figures 2-3 through 2-5 illustrate the two cards and a module that comprise the HPMM. The figures are:

- Figure 2-3 HPM UCN Interface module
- Figure 2-4 High-Performance Comm/Control card
- Figure 2-5 High-Performance I/O Link card

Refer to these figures for the discussion of HPMM indicators, diagnostic switch, and power margin jumper that follows.

Power indicators

When power is applied to the HPMM, the **Power** indicator on each HPMM card and the HPM UCN Interface module lights. The **Power** indicator is illuminated whenever 24 Vdc from the cabinet Power System is present.

Status indicators

The **Status** indicator on the High-Performance Communications/Control card illuminates momentarily after applying power. Internal test routines are executed upon applying power, and the **Status** indicator remains on if the tests are successfully completed. The steady illumination of the **Status** indicator signifies that no test failures were detected.

The High-Performance I/O Link **Status** indicator is not lit when the HPMM is in the Alive state. It will light (not blinking) after the HPMM is loaded with the operating personality software, and enters the OK state.

The UCN cable in use indicators are visible at the front of the HPM UCN Interface module (**Rx-A** and **Rx-B**) as well as under the front cover of the High-Performance Comm/Control card (**UCN A** and **UCN B**).

The Transmit (**Tx**) indicator at the front of the HPM UCN Interface module is an indication of UCN cable transmit activity.

Refer to subsection 4.5 in this manual for additional information on the status indicators.

Diagnostic display

The 4-digit Diagnostic display at the front of the High-Performance Communications/Control card (below the upper extraction lever) provides additional status information as well as error code information if a failure occurs. After power is applied and the internal test routines have completed successfully, it will display a code that indicates the HPMM is in the Alive state, such as **Axxx.**

Continued on next page

Diagnostic display analysis example

A diagnostic code of **AL09** is analyzed as follows:

First character = **A** = The HPMM is in the Alive state.

Possible first characters are:

A = Alive

B = Backup

I = Idle

F = Fail

L = Load

T = Test

Second character = **L** = The card file is a left 7-Slot file.

Possible characters are:

L = Left 7-slot HPMM card file

R = Right 7-slot HPMM card file

1 = First 15-slot HPMM card file

2 = Second 15-slot HPMM card file

Third and Fourth characters = **09** = The pinned UCN node number

Refer to subsection 4.6 in this manual for additional Diagnostic display codes and more detailed information.

Detailed Diagnostic display switch

A pushbutton switch (**Display**) under the front cover of the High-Performance Comm/Control card controls additional detailed diagnostic information displays. The additional diagnostic codes are presented in a fixed sequence.

This detailed diagnostic information becomes extremely useful when troubleshooting.

The switch effects only the behavior of the display and will not effect the operational capability of the High-Performance Comm/Control card.

Refer to subsection 4 in this manual for troubleshooting information, failure code charts including suggested corrective actions, and additional information on detailed diagnostic displays and the sequences of presentation.

Continued on next page

Debug connector

The High-Performance Comm/Control card has a debug connector (**Debug**) under the front cover. The connector is used by Honeywell engineering with specialized equipment and design level knowledge. The factory also uses the connector.

HPMM +5 volt power margins

HPMM +5 volt power margining can be accomplished by using the jumper positions under the front cover of the High-Performance I/O Link card. The possible settings are **Normal**, **High**, and **Low** margins. Power margining is used by manufacturing test and can also be used for troubleshooting intermittent hardware problems as a last resort. Power margining is effective as soon as the jumper is moved.

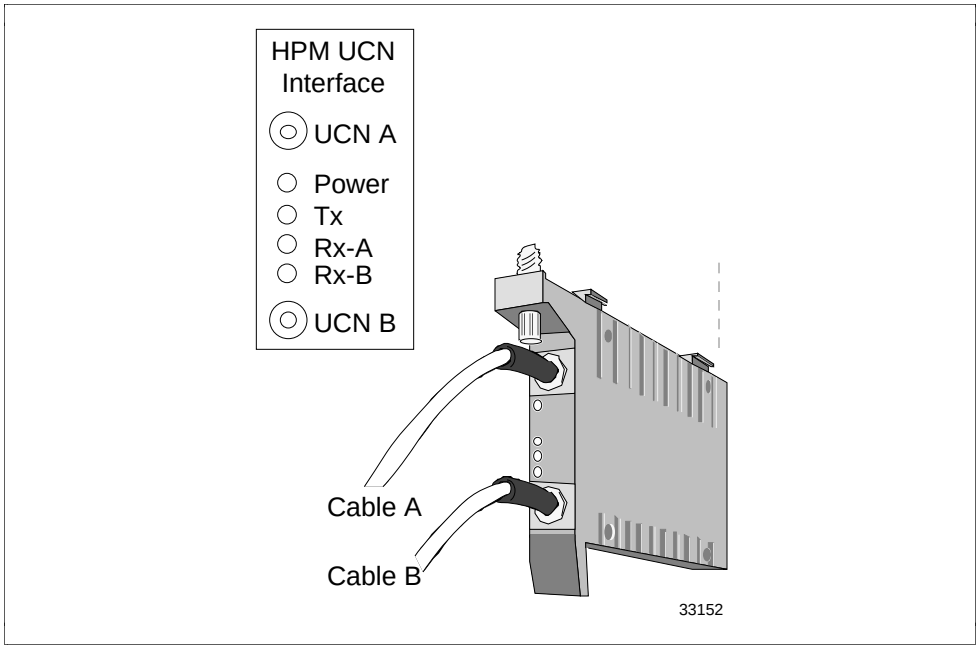
Honeywell does not recommend the use of power margins on any device that is on-process. Figure 2-5 identifies the pinning selections on the High-Performance I/O Link card with a single jumper.

It is important that the jumper be placed in the **Normal** position when a nominal voltage level is required (rather than removing the jumper completely). The jumper in the **Normal** position is required to internally set the correct values for error detection (error trip points) at the nominal voltage level.

HPM UCN Interface module illustration

Figure 2-3 illustrates the front of the HPM UCN Interface module.

Figure 2-3 HPM UCN Interface Module (Front Panel)

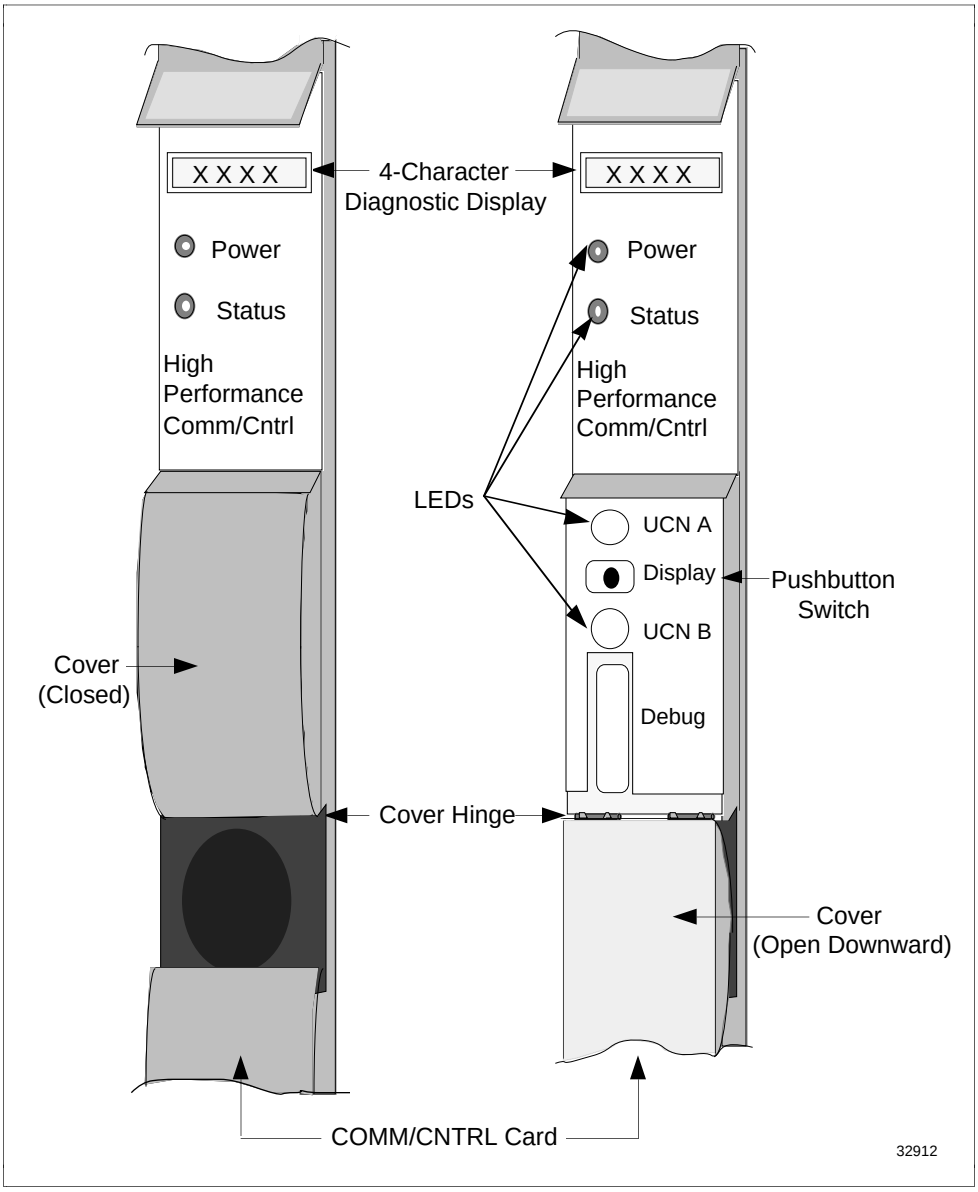


Continued on next page

High-Performance Comm/Control card illustration

Figure 2-4 illustrates the front of the High-Performance Comm/Control card as well as the indicators, Diagnostic display, Detailed Diagnostic switch, and Debug connector that are located under the front cover.

Figure 2-4 High-Performance Comm/Control Card (Front Panel)

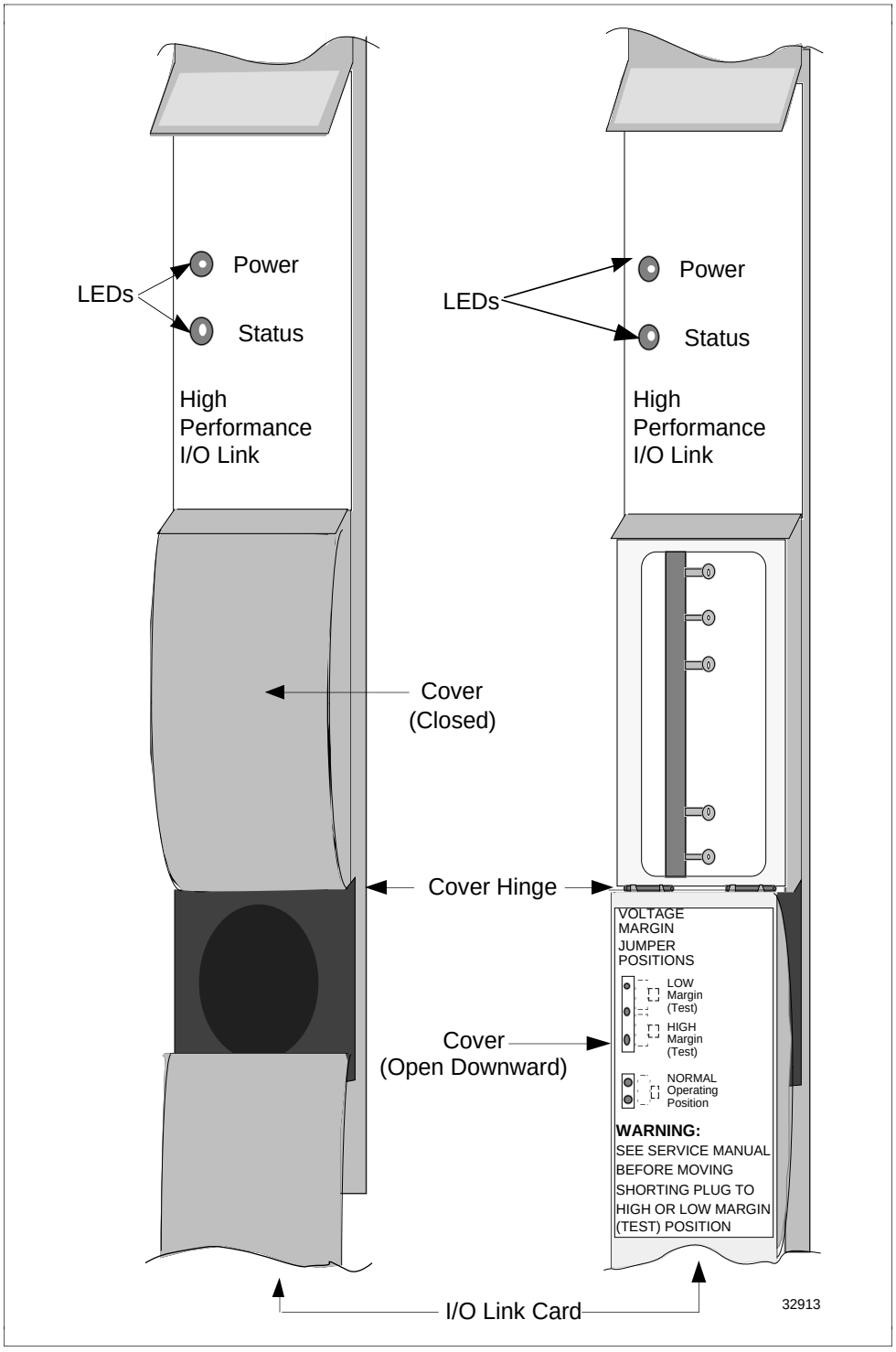


Continued on next page

High-Performance I/O Link card illustration

Figure 2-5 illustrates the front of the High-Performance I/O Link card as well as the voltage margin jumper pins that are located under the front cover.

Figure 2-5 High-Performance I/O Link Card (Front Panel)



2.6 IOP Card Files

Introduction

Additional Input/Output Processor (IOP) card file slots can be added to any High-Performance Process Manager by the addition of one or more 7-Slot (Left or Right) or 15-Slot card files. CE Compliant 7-Slot or 15-Slot card files that accommodate only IOPs are designated IOP card files. The IOP card files are electrically the same card files as the card files that HPMM cards occupy. They have the same backplane but differ mechanically. Each IOP card file accommodates either 7 or 15 IOPs. A 15-Slot IOP card file is illustrated in Figure 2-6.

In cabinets that are upgraded from a PM or APM configuration to an HPM configuration, IOP Only card files may exist. These 15-Slot IOP Only card files are restricted to IOP and optional I/O Link Extender cards.

Total number of card files

The number of card files that can exist in a single High-Performance Process Manager subsystem is dependent upon the mix of 7-Slot and 15-Slot card files. This includes card files that are designated HPMM or IOP card files. Eight I/O Link Interface addresses are available for use in the HPM subsystem. Each card file must be assigned an I/O Link Interface address. Two 7-Slot card files can share the same I/O Link Interface address if one is a Left card file (slots 1-7) and the other a Right card file (slots 9-15). The 15-Slot card file (HPMM or IOP type) cannot share its I/O Link Interface address with another card file. It is conceivable that sixteen 7-Slot card files can exist in a HPM subsystem (eight Left 7-Slot and eight Right 7-Slot card files).

Remote card file installation

IOP card files can be installed at remote locations by the use of I/O Link Extenders as well as locally in the HPM cabinet or cabinet complex.

Total number of IOPs

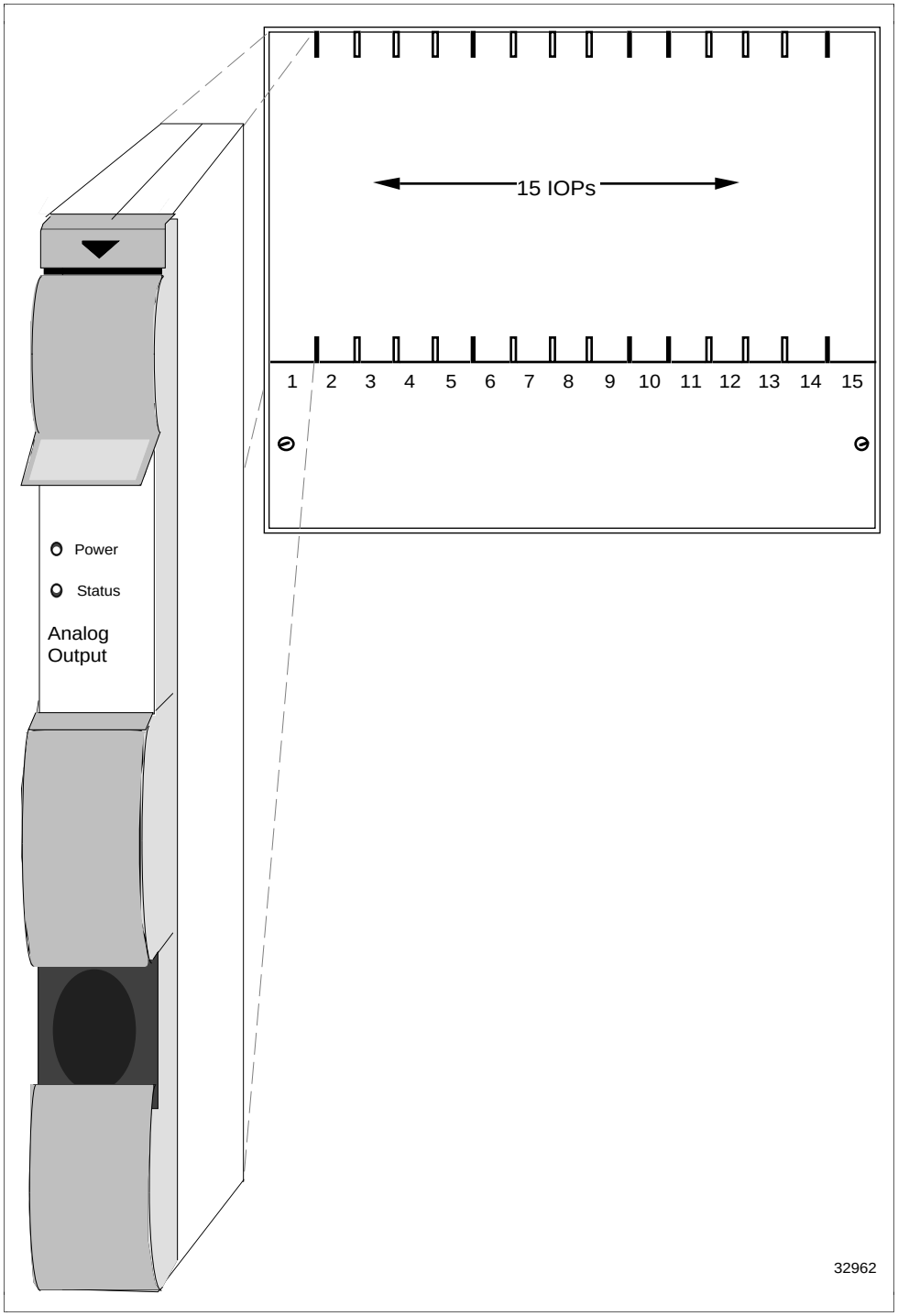
Depending upon the configuration of IOP types, up to 40 primary IOPs, 40 secondary (redundant) IOPs, and 3 I/O Link Extenders (a maximum of 8 I/O Link Extender cards) can exist in a single HPM subsystem.

Continued on next page

15-Slot IOP card file

Figure 2-6 illustrates a 15-slot IOP card file.

Figure 2-6 15-Slot IOP Card File



2.6.1 IOPs

Types of Input/Output Processors (IOPs)

There are eleven types of Input/Output Processor (IOP) card assemblies. Some IOP card types interface with more than one type of Field Termination Assembly (FTA). The functional types of IOPs are:

- High Level Analog Input (HLAI)
- Low Level Analog Input (LLAI)
- Low Level Analog Multiplexer (LLMux)
- Digital Input (DI)
- Analog Output (AO)
- Digital Output (DO)
- Smart Transmitter Interface (STI)
- Pulse Input (PI)
- Digital Input Sequence of Events (DISOE)
- Serial Device Interface (SDI)
- Serial Interface (SI)

AO and DO IOPs

Some of the functional types of IOPs support only certain associated Field Termination Assemblies (FTAs) models because the number of channels (Points) differ. Examples are the Analog Output (8 and 16 channels) and Digital Output (16 and 32 channels) IOPs.

2.6.2 Redundant IOPs

Introduction

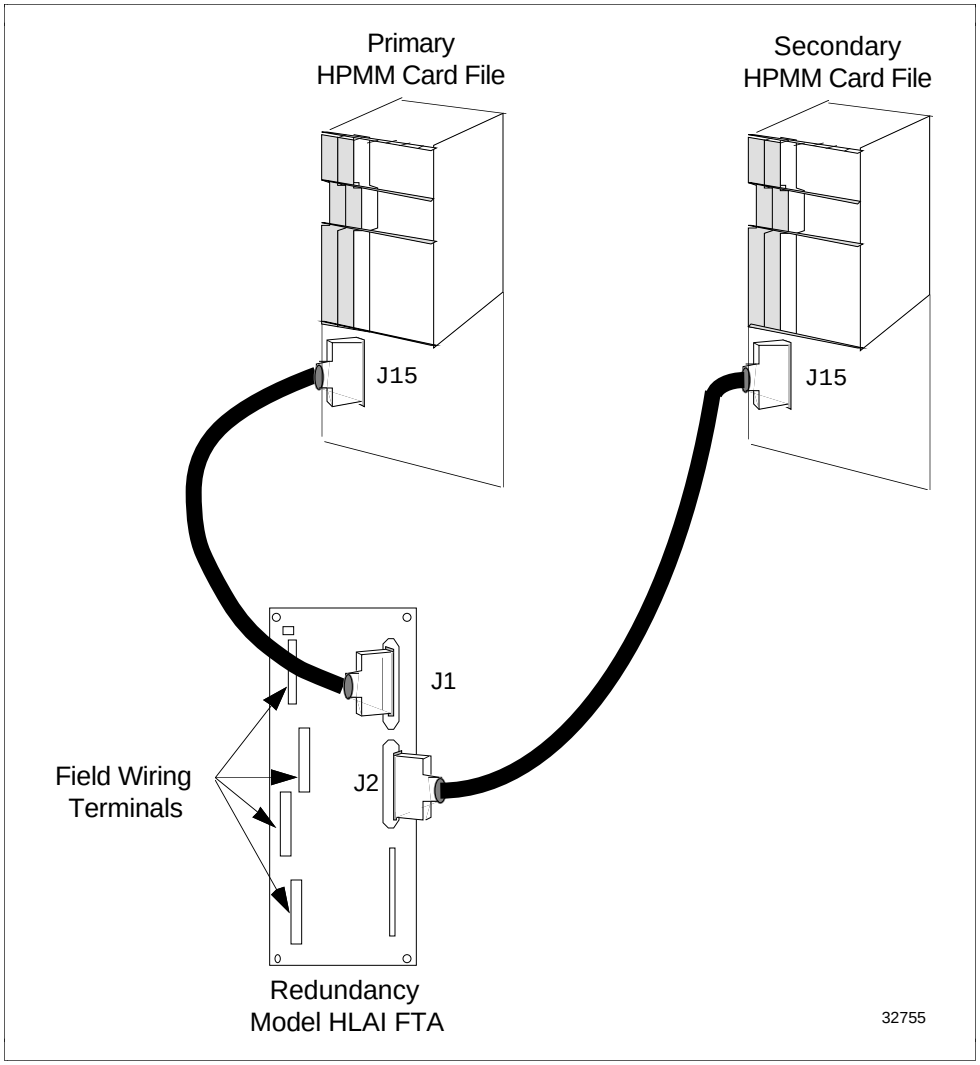
IOPs can be connected in a redundant configuration with both IOPs connected by separate cables to the same FTA. Some models of the following types of IOPs support redundancy.

- Smart Transmitter Interface (STI)
- High Level Analog Input (HLAI)
- Digital Input (DI)
- Digital Output (DO)

Redundant HLAI IOPs

Figure 2-7 illustrates an HLAI FTA that interfaces with a pair of HLAI IOPs that are installed in separate 7-Slot card files.

Figure 2-7 HLAI FTA with Redundant HLAI IOPs

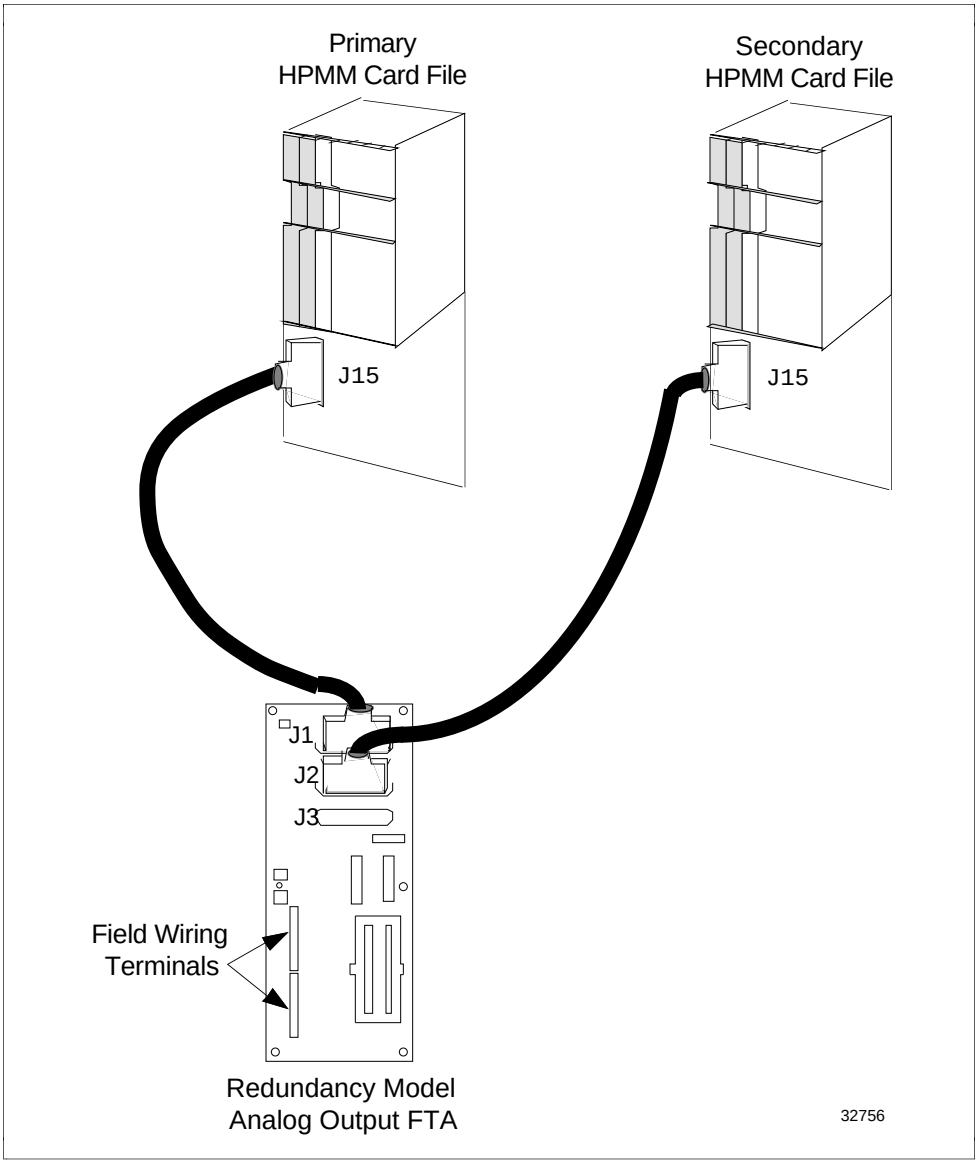


Continued on next page

Redundant AO IOPs

When an Analog Output FTA interfaces with two IOPs through separate cables, and an automatic selector switch on the FTA selects which IOP's output drives the field wiring terminal connectors on the FTA. Figure 2-8 is an illustration of an Analog Output FTA interface with two Analog Output IOPs.

Figure 2-8 Analog Output FTA with Redundant Analog Output IOPs



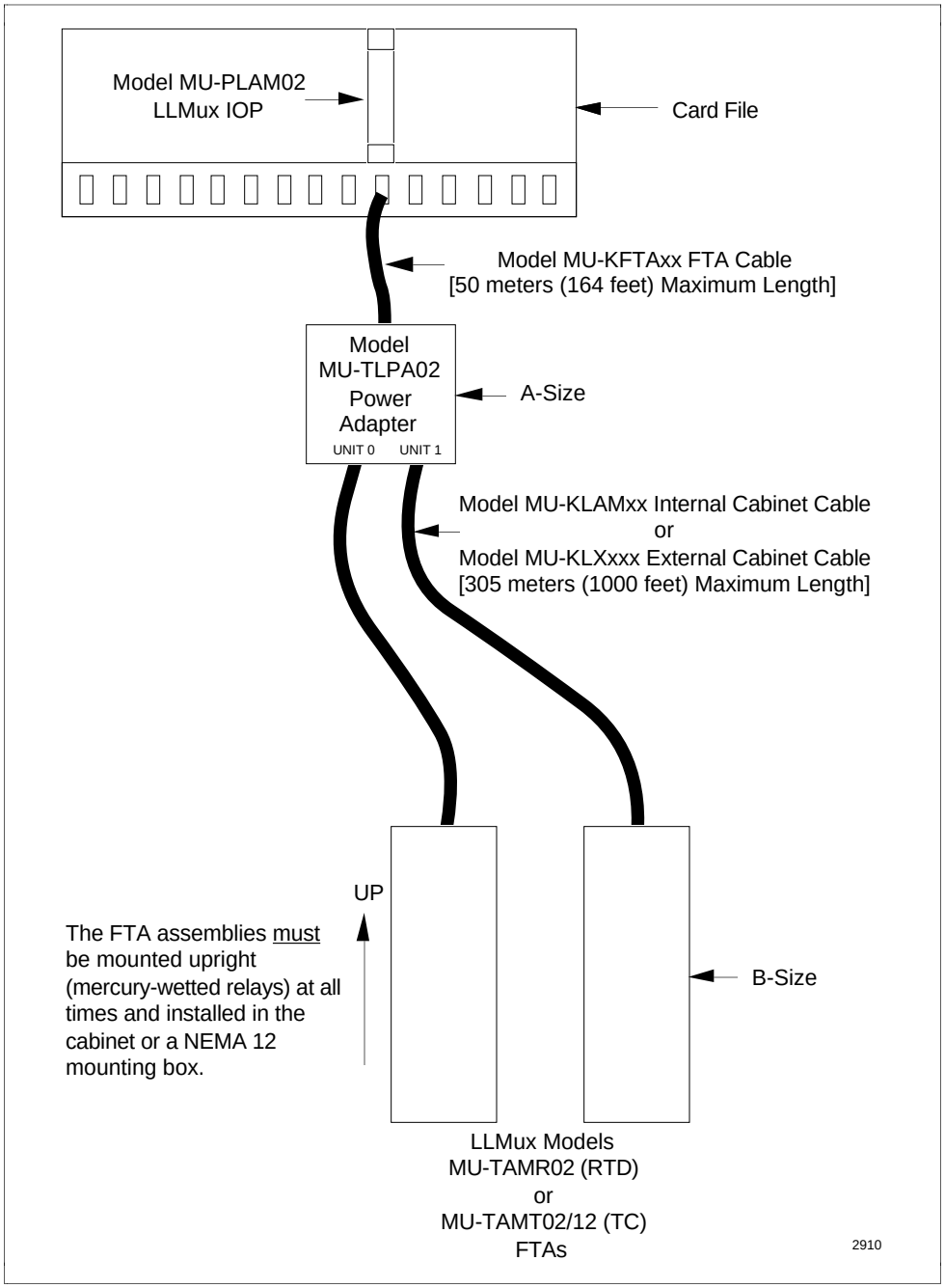
2.6.3 Low Level Multiplexer IOP (LLMux)

Introduction

A Low Level Analog Input Multiplexer (LLMux) IOP processes up to 32 inputs from two 16 input FTAs.

Figure 2-9 illustrates LLMux FTA interconnections for non-CE Compliant FTA models. CE Compliant FTA models are similar. See the *Process Manager I/O Installation* manual for detailed information.

Figure 2-9 Low Level Multiplexer Interconnections



Continued on next page

2.6.3 Low Level Multiplexer IOP (LLMux), Continued

Two types of FTAs

There are two types of FTAs, Thermocouple (TC) and Resistive Temperature Device (RTD), that are connected to the IOP through a Power Adapter assembly. One TC and one RTD FTA, or two of the same type FTAs can be connected to one IOP through the Power Adapter.

Power adapter installation

The Power Adapter provides power to the FTA and can be installed on an FTA Mounting Channel.

IOP to Power Adapter connection

The IOP to Power Adapter connection is made using the standard model MU-KFTAxx (the suffix "xx" represents the length of the cable in meters) IOP to FTA cable. The maximum allowable length is 50 meters (164 feet).

For CE Compliance applications, the model MU-KFTSxx IOP to FTA cable must be used. See the *Process Manager I/O Installation* manual for detailed information.

Power Adapter to FTA connection

The Power Adapter connects to either FTA type with a model MU-KLAMxx (internal cabinet use) or model MU-KLXxxx (external cabinet use) cable (one per FTA). The cable is limited to a maximum length of 305 meters (1000 feet).

The model MU-KLAMxx cable has two individually shielded, twisted pair wires. The shield must be connected to ground at the Power Adapter end of the cable only.

The model MU-KLXxxx external cabinet cable has four wires with a single braided shield. The braided shield must be connected at both the Power Adapter and FTA ends of the cable.

For CE Compliance applications, Belden model 83654 braided shield cable must be used. See the *Process Manager I/O Installation* manual for detailed information.

Power Adapter indicators

The Power Adapter assembly has two LEDs, one for each cable, that indicate a grounded or shorted cable. Each FTA has an LED that indicates the FTA is receiving power.

Cabling information

For more detailed information on cable selection, see the *Process Manager I/O Installation* manual or the *High-Performance Process Manager Planning* manual.

2.6.4 Serial Device Interface IOP (SDI)

Introduction

Figure 2-10 illustrates a typical Serial Device Interface configuration. One or two Serial Device Interface FTAs can be connected to a single Serial Device Interface IOP through the Power Adapter.

The FTA is assigned a unique FTA model number identified by the FTA's assembly tab number on the FTA. The firmware resident in the FTA plug-in module, M1, has been preprogrammed at the factory to accommodate the associated IOP and the selected serial communications interface type (EIA-232 or EIA-422/485).

The Serial Device Interface FTA has both EIA-232 (RS-232) and EIA-422/485 (RS-422/485) asynchronous serial communications interfaces, one of which is active, using either a DB-25 or a 5-terminal compression connector, respectively.

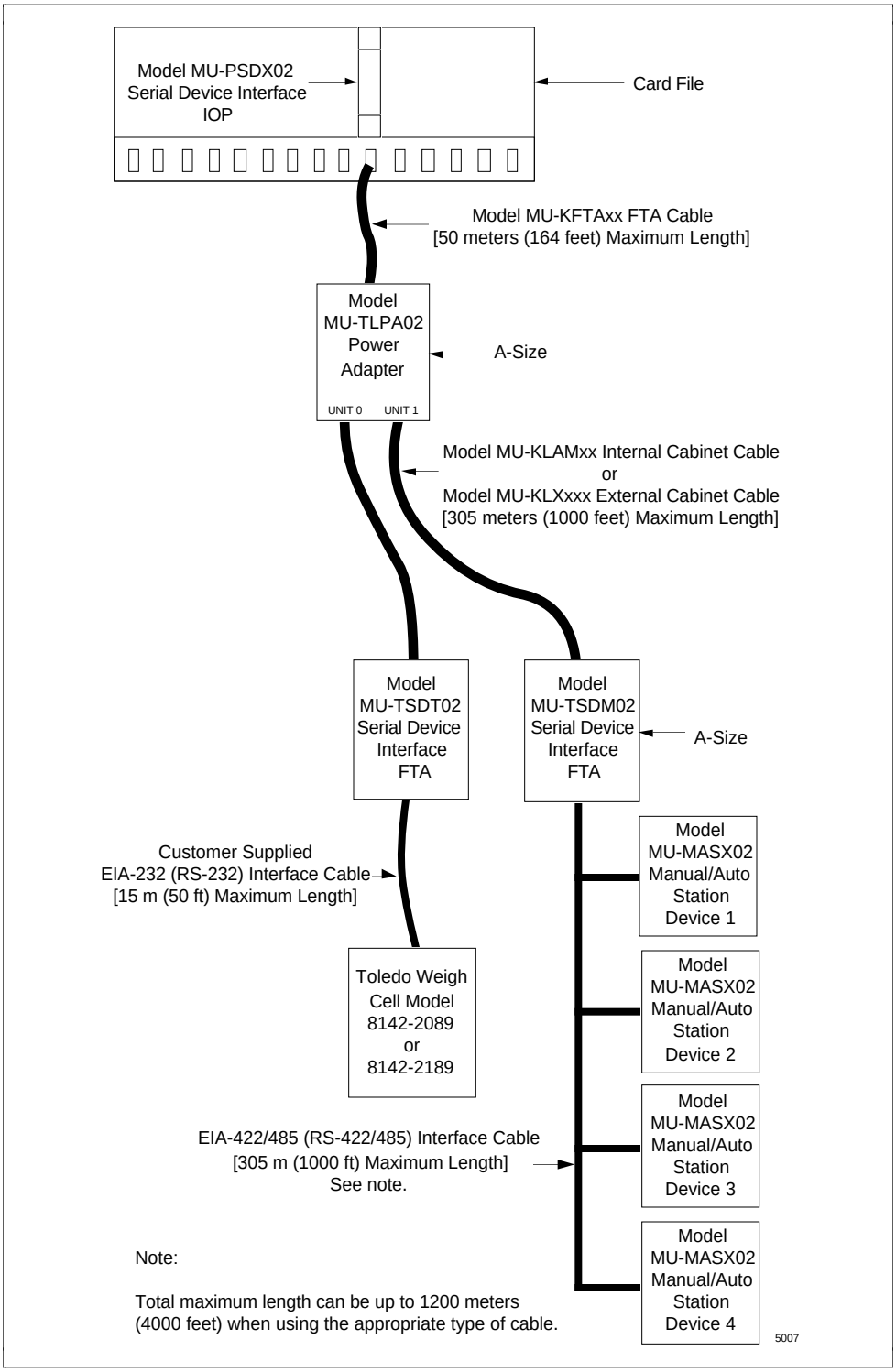
Continued on next page

2.6.4 Serial Device Interface IOP (SDI), Continued

SDI interface configuration

Figure 2-10 illustrates a typical Serial Device Interface configuration.

Figure 2-10 Serial Device Interface Interconnections



Continued on next page

2.6.4 Serial Device Interface IOP (SDI), Continued

EIA-232 and EIA--422/485 interfaces	The EIA-232 interface is a point-to-point interface to which only one serial device can be connected. The EIA-422/485 interface can be configured as a multidrop interface to which several serial devices can be connected.
EIA-232 interface cable length	The EIA-232 cable is limited to a distance of 15 meters (50 feet). The cable must be supplied by the user and terminate in a DB-25 connector.
EIA-422/485 cable length limitation	EIA-422/485 cable is limited to a distance of 305 meters (1000 feet). However, the total length can be 1200 meters (4000 feet) with the appropriate interface cable.
Power Adapter installation	The Power Adapter can be installed on any available FTA Mounting Channel that is within the 50-meter (164-foot) maximum cable length requirement between the IOP and the Power Adapter. The Power Adapter has the same dimensions as an A size (6 inches) FTA. Model MU-KFTAxx interface cable is used.
SDI FTA installation	The Serial Device Interface FTA can be installed in the same cabinet as the Serial Device Interface IOP, or externally, up to 305 meters (1000 feet) from the Power Adapter. The FTA is an A-size (6 inches) FTA and installs on a standard FTA Mounting Channel.
FTA to Power Adapter interface	The Serial Device Interface FTA to Power Adapter connection is made using either model MU-KLAMxx cable for internal cabinet installation or model MU-KLXxxx cable for external cabinet installation. The suffix “xx” or “xxx” represents the length of the cable in meters. The model MU-KLAMxx cable has two individually shielded, twisted pair wires. The shield must be connected to ground at the Power Adapter end of the cable only. The model MU-KLXxxx external cabinet cable has four wires with a single braided shield. The braided shield must be connected at both the Power Adapter and FTA ends of the cable.

Continued on next page

2.6.4 Serial Device Interface IOP (SDI), Continued

Model MU-TSDT02 FTA	The model MU-TSDT02 Serial Device Interface FTA accommodates the model 8142-2084 or 8142-2184 Toledo Weigh Cell device, manufactured by Toledo Scale Inc., through its EIA-232 (RS-232) interface.
Model MU-TSDM02 FTA	The model MU-TSDM02, assembly number 51303932-202, Serial Device Interface FTA accommodates up to four model MU-MASX02 Manual/Auto Station devices, manufactured by Honeywell Inc., through its EIA-422/485 (RS-422/485) interface.
Model MU-TSDU02 FTA	The model MU-TSDU02 Serial Device Interface FTA accommodates up to four model MU-MASX02 UDC 6000 devices, manufactured by Honeywell Inc., through its EIA-422/485 (RS-422/485) interface.
Cabling information	For more detailed information on cable selection, see the *Process Manager I/O Installation* manual or the *High-Performance Process Manager Planning* manual.

2.6.5 Serial Interface IOP (SI)

Introduction

Figure 2-11 illustrates typical Serial Interface interconnections. One or two model MU-TSIM12 or MU-TSIA12 Serial Interface FTAs interface to a model MU-PSIM02 Serial Interface IOP through the model MU-TLPA02 Power Adapter. Figure 2-11 illustrates the model MU-TSIM12 FTA interconnections.

The FTA is assigned a unique FTA model number that is identified by the FTA's assembly tab number on the FTA. The firmware resident in the FTA plug-in module, M1, is preprogrammed at the factory to accommodate the associated IOP and the configured serial communications interface types (EIA-232 and EIA-422/485).

EIA-232 and EIA-422/485 interfaces

The Serial Interface FTA has both EIA-232 (RS-232) and EIA-422/485 (RS-422/485) asynchronous serial communications interfaces, one of which is active, using either a DB-25 or a 5-terminal compression connector, respectively.

Point-to-point or multidrop interfaces

The EIA-232 interface is a point-to-point interface to which only one serial device can be connected. The EIA-422/485 interface can be configured as a multidrop interface to which several serial devices can be connected. System performance is dependent upon the number of devices, their baud rate, the number of transactions, and the FTA Device Driver firmware.

EIA interface limitations

The EIA-232 interface is limited to a distance of 15 meters (50 feet) maximum, and the EIA-422/485 interface is limited to a distance of 305 meters (1000 feet). However, the total length of the EIA-422/485 interface can be 1200 meters (4000 feet) with the appropriate interface cable.

Power Adapter installation

The Power Adapter can be installed on any available FTA Mounting Channel that is within the 50-meter (164-foot) maximum cable length requirement using a model MU-KFTAxx cable (the suffix "xx" represents the length of the cable in meters).

For CE Compliant installations, if the Power Adapter is remotely mounted in a cabinet that is separate from the cabinet in which its associated IOP is mounted, it is mandatory that a model MU-KFTSxx shielded IOP to FTA cable be used between the assemblies.

Power Adapter size

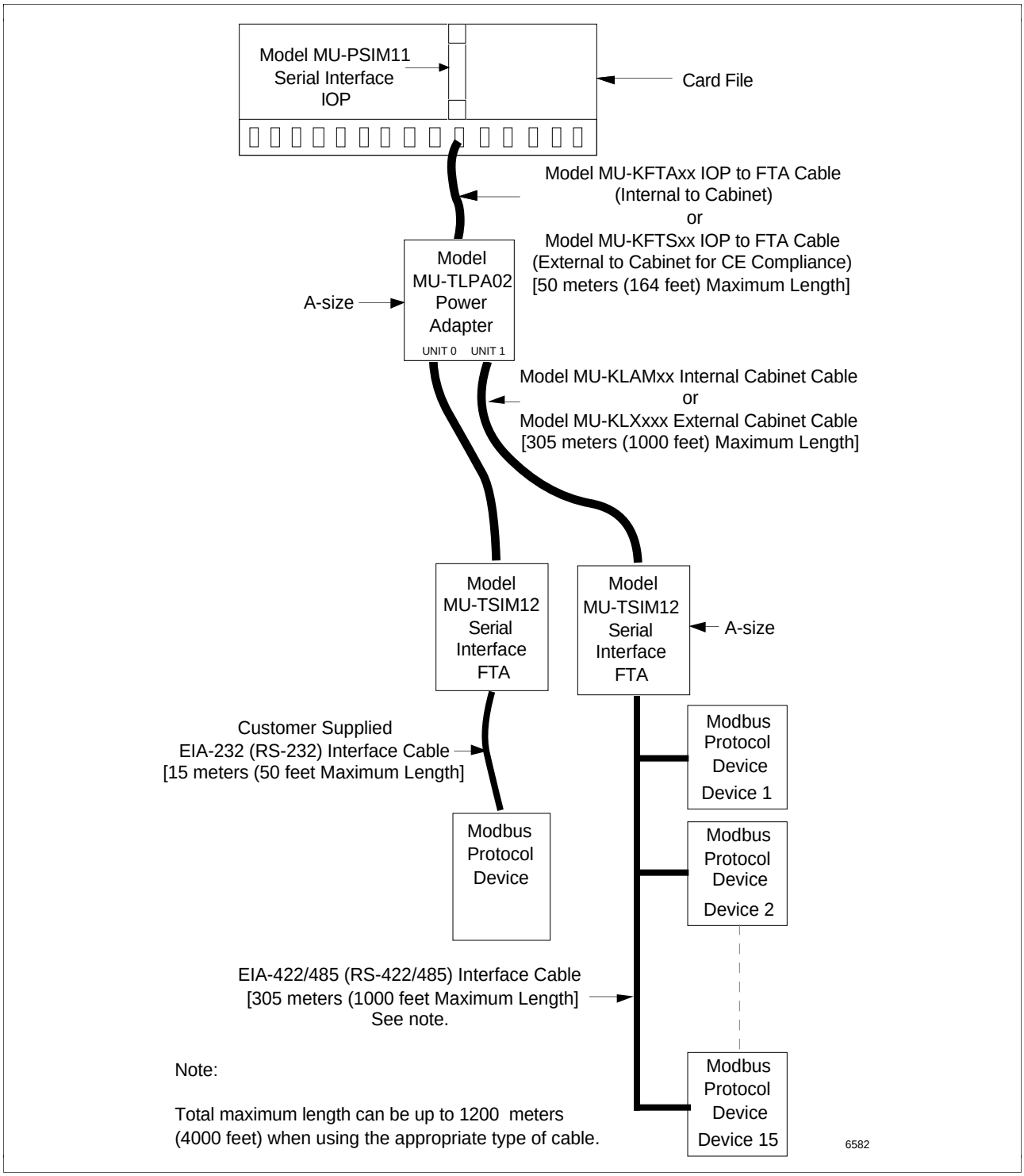
The Power Adapter has the same dimensions as an A-size (6 inches) FTA.

Continued on next page

Model MU-TSIM12 interconnections

Figure 2-11 illustrates a Serial Interface configuration incorporating the model MU-TSIM12 Serial Interface FTA.

Figure 2-11 Model MU-TSIM12 Serial Interface FTA Interconnections



Continued on next page

2.6.5 Serial Interface IOP (SI), Continued

SI FTA installation

The Serial Interface FTA can be installed in the same cabinet as the Serial Interface IOP using model MU-KLAMxx cable (the suffix "xx" designates the length of the cable in meters), or remotely, up to 305 meters (1000 feet) from the Power Adapter. The FTA is an A-size (6 inches) FTA and installs on a standard FTA Mounting Channel.

FTA to Power Adapter interface

The Serial Interface FTA to Power Adapter connection is made using either model MU-KLAMxx cable for internal cabinet installation or model MU-KLXxxx cable for external cabinet installation. The suffix "xx" or "xxx" represents the length of the cable in meters.

The model MU-KLAMxx cable has two individually shielded, twisted pair wires. The shield must be connected to ground at the Power Adapter end of the cable only.

The model MU-KLXxxx external cabinet cable has four wires with a single braided shield. The braided shield must be connected at both the Power Adapter and FTA ends of the cable.

Cabling information

For more detailed information on cable selection, see the *Process Manager I/O Installation* manual or the *High-Performance Process Manager Planning* manual.

Model MU-TSIA12 EIA-232 interface

The model MU-TSIA12 Serial Interface FTA, in combination with the model MU-PSIM11 IOP and the model MU-TLPA02 Power Adapter, provides an EIA-232 (RS-232) communications interface for the Allen-Bradley PLC-2, PLC-3, or PLC-5 devices with its EIA-232 interface.

Model MU-TSIM12 EIA-232 interface

The model MU-TSIM12 Serial Interface FTA, in combination with the model MU-PSIM11 IOP and the model MU-TLPA02 Power Adapter, provides a Modbus RTU EIA-232 (RS-232) communications interface for a peripheral with its EIA-232 interface.

Model MU-TSIM22 EIA-422/485 interface

The model MU-TSIM22 Serial Interface FTA, in combination with the model MU-PSIM11 IOP and the Power Adapter, provides an EIA-422/485 (RS-422/485) communications interface for peripherals that have an EIA-422/485 interface.

2.7 I/O Link Extender (Fiber Optic Link)

Introduction

The I/O Link Extender provides the ability to locate 7-Slot and 15-Slot IOP card files and associated FTAs up to 8 kilometers (5 miles) from the HPMM(s). Two types of I/O Link Extenders and their associated fiber Optical Coupler Modules are available, the "Standard" I/O Link Extender which provides up to a 1.3 kilometers (4000 feet) link, and the "Long Distance" I/O Link Extender which provides up to an 8 kilometers (5 miles) link. The connection is made using a pair of fiber optic transmission cables, driven and terminated by a fiber Optical Coupler Module that mates with the connector located directly below the card file slot in which the I/O Link Extender card is installed.

Features and guidelines

As illustrated in Figures 2-12 through 2-15:

- Each I/O Link Extender consists of two I/O Link Extender cards, one for Link A and one for Link B, which occupy two slots in the HPMM or IOP card file.
- Each Standard I/O Link Extender card has an associated fiber Optical Coupler Module that can drive up to three pair of fiber optic cables. Each cable pair is terminated by a fiber Optical Coupler Module that terminates one fiber optic pair.
- Each Long Distance I/O Link Extender card has an associated Fiber Coupler that drives a single pair of fiber optic cables. Each cable pair is terminated by a fiber Optical Coupler Module that terminates one fiber optic pair.
- Every remote card file, or complex of IOP card files, requires two I/O Link Extender cards and two fiber Optical Coupler Modules, one for Link A and one for Link B. The Standard I/O Link Extender card will drive and terminate Link A or Link B, depending upon the card file's I/O Link Interface address and slot number's I/O Link Interface address. If the card file and slot number I/O Link Interface address are both odd or both even, the card will drive Link A. If the card file and slot number I/O Link Interface address are not both odd or both even, the card will drive Link B. The Link A or Link B selection for the Long Distance I/O Link Extender is determined by a jumper on the card.
- Two Standard I/O Link Extender cards, connecting up to six remote card files, can be installed in a HPMM card file, but the maximum number of other primary IOPs is still 40 (plus 40 redundant IOPs).
- The maximum fiber optic cable length is dependent upon the number of splices and quality of the cable (dB loss per meter of cable). This maximum can be between 0.98 and 1.3 kilometers for the Standard I/O Link Extender and 8 kilometers for the Long Distance I/O Link Extender. See the *High-Performance Process Manager Planning* manual for the Loss Budget calculation.

Continued on next page

2.7 I/O Link Extender (Fiber Optic Link), Continued

Front panel indicators

Two visual front panel indicators are provided on the I/O Link Extender card that are consistent with the display of IOP card indicators. The upper indicator is illuminated if the fused +24 Vdc is present on the card (the input voltage is acceptable). The lower indicator denotes status.

Status indicator operation

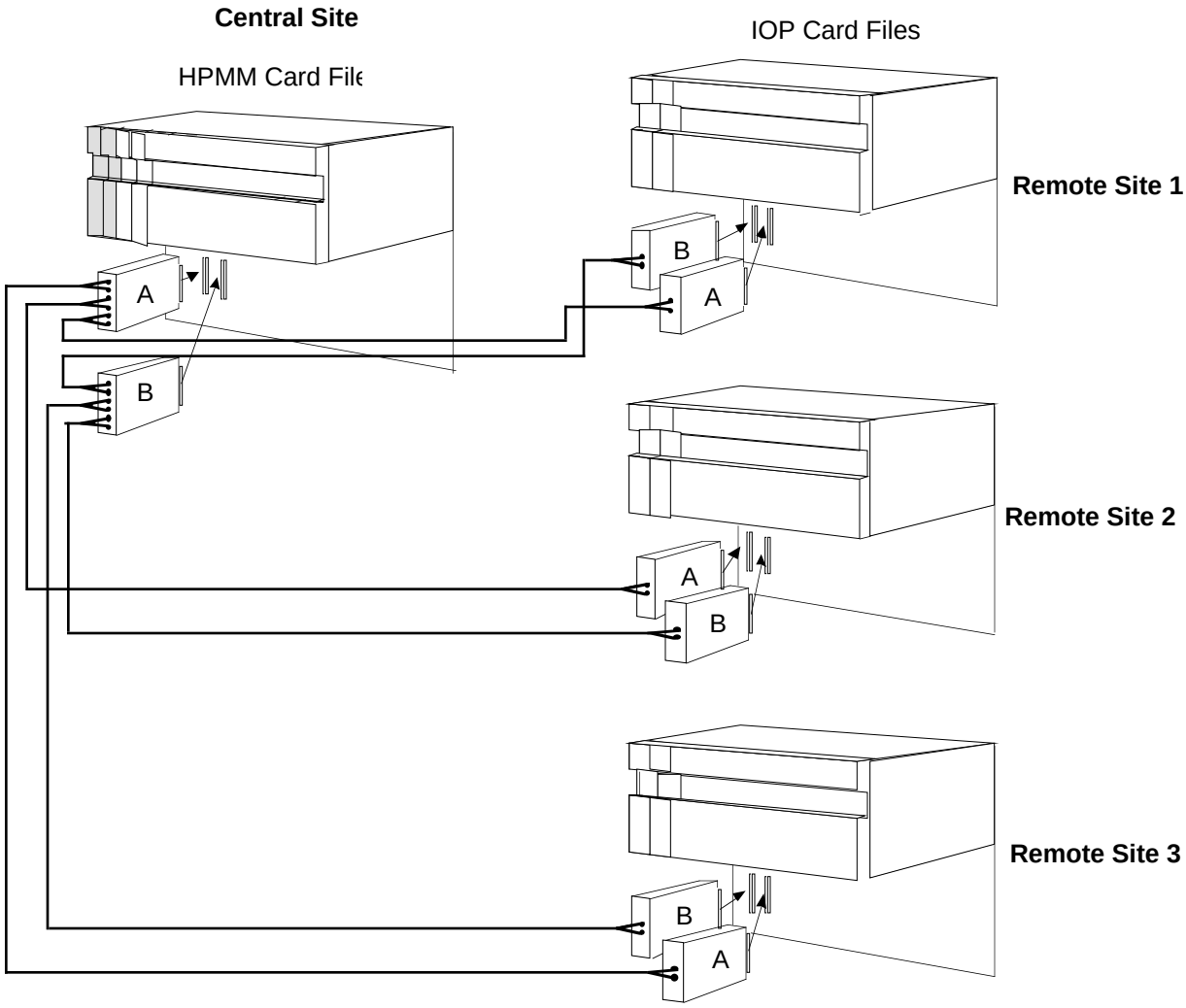
In normal operation, the lower indicator is illuminated when messages are being transmitted from the fiber optic cable. The indicator should be fully lit or slightly flickering, depending on system loading. Abnormal operation will result in the anti-jabber circuit locking up the transmitter circuit when the transmission period has been too long. The indicator will then be extinguished. If the fiber Optical Coupler Module is improperly installed, the indicator will blink at a 50% duty cycle. The anti-jabber circuit can be reset by cycling the upper extractor/insertion lever power switch on the I/O Link Extender card. For the Long Distance I/O Link Extender, cycling power resets both ends of the link. The Standard I/O Link Extender must be manually reset at both ends of the link. The Long Distance I/O Link Extender can be reset by cycling power at one end of the link.

Continued on next page

Standard I/O Link Extender connections nonredundant HPMM

Figure 2-12 illustrates the interconnections for a Standard I/O Link Extender in an High-Performance Process Manager that contains a nonredundant HPMM.

Figure 2-12 Standard I/O Link Extender Interconnections with Nonredundant HPMM

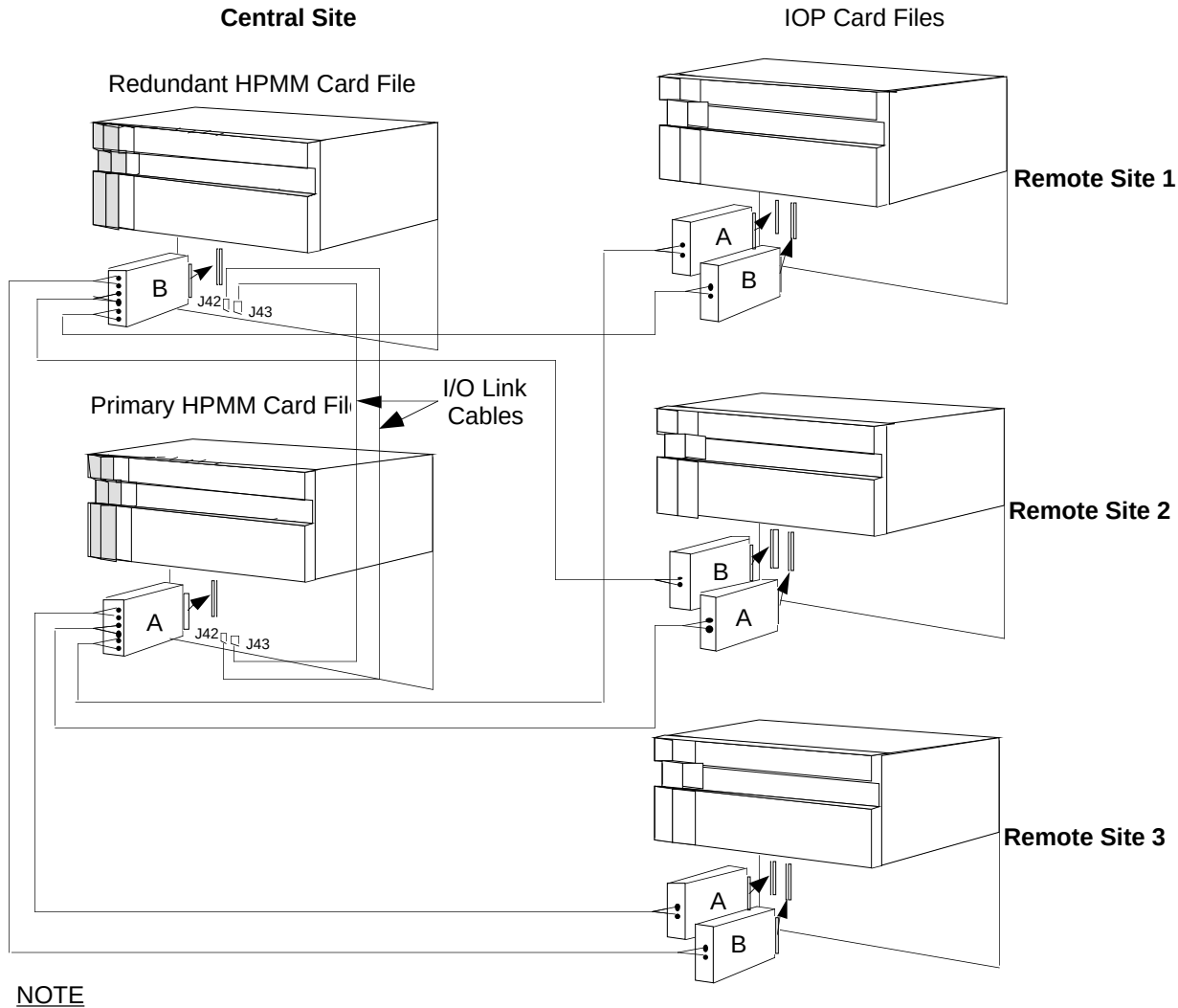


Continued on next page

Standard I/O Link Extender connections redundant HPMMs

Figure 2-13 illustrates the interconnections for a Standard I/O Link Extender in an High-Performance Process Manager that contains redundant HPMMs.

Figure 2-13 Standard I/O Link Extender Interconnections with Redundant HPMMs



NOTE

The following High-Performance Process Manager subsystem configuration is assumed.

1. The lower HPMM card file is configured as card file #1 (I/O Link Address of 0).
2. The upper HPMM card file is configured as card file #2 (I/O Link Address of 1).
3. Remote Site #1's IOP card file is configured as card file #3 (I/O Link Address of 2).
4. Remote Site #2's IOP card file is configured as card file #4 (I/O Link Address of 3).
5. Remote Site #3's IOP card file is configured as card file #5 (I/O Link Address of 4).

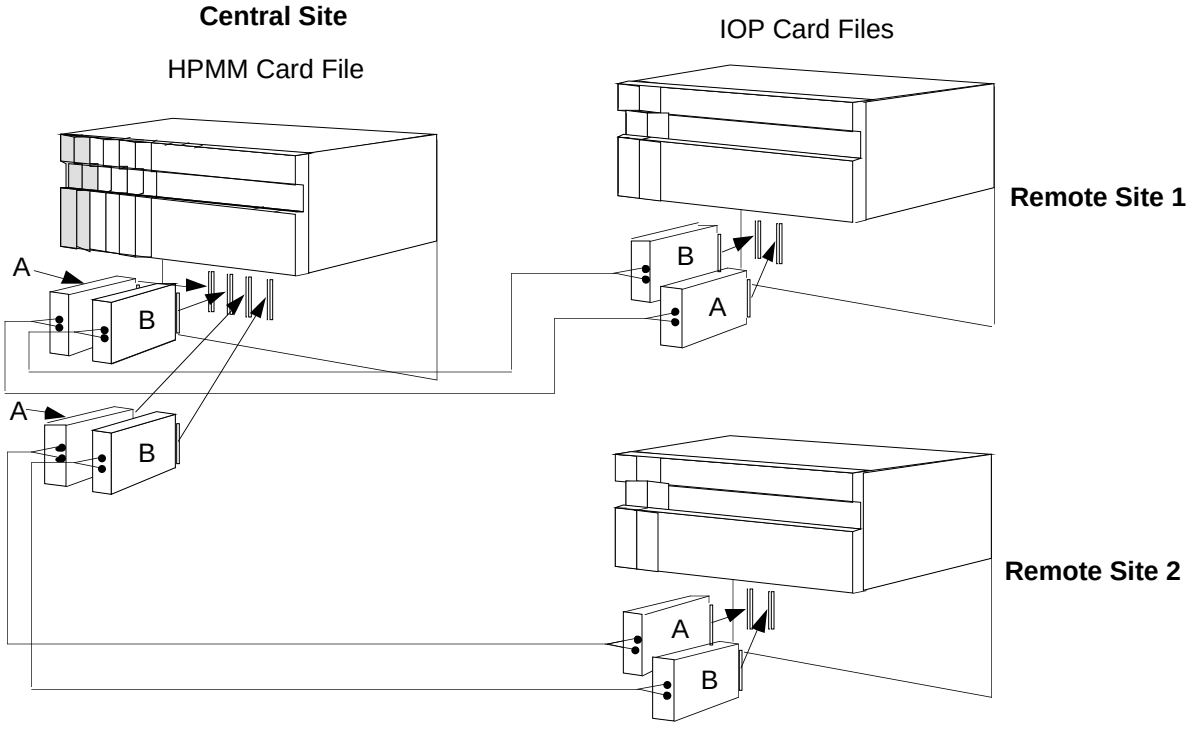
32778

Continued on next page

Long Distance I/O Link Extender connections nonredundant HPMM

Figure 2-14 illustrates the interconnections for a in an High-Performance Process Manager that has a nonredundant HPMM.

Figure 2-14 Long Distance I/O Link Extender Interconnections with Nonredundant HPMM



NOTE

The following High-Performance Process Manager subsystem is assumed.

1. The HPMM card file is configured as card file #1 (I/O Link Address of 0).
2. Remote Site #1's IOP card file is configured as card file #2 (I/O Link Address of 1).
3. Remote Site #2's IOP card file is configured as card file #3 (I/O Link Address of 2).

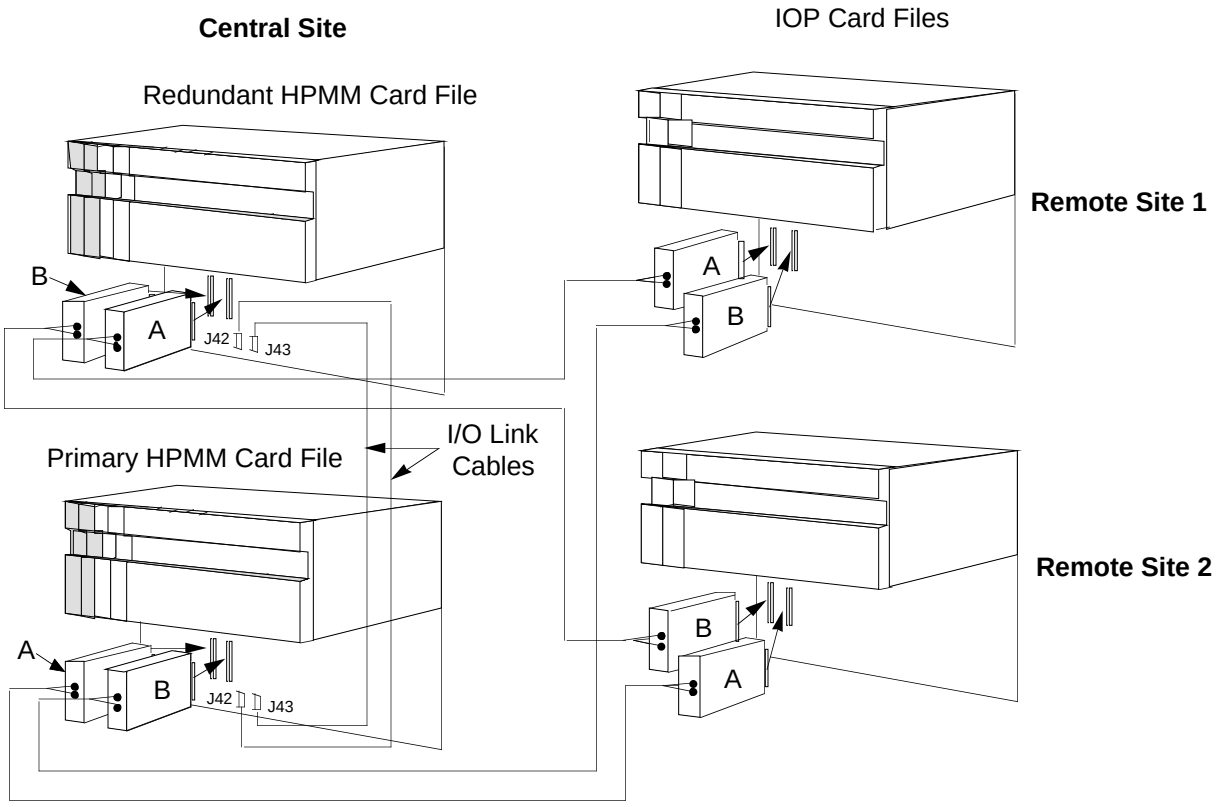
32779

Continued on next page

Long Distance I/O Link Extender connections redundant HPMMs

Figure 2-15 illustrates the interconnections for a Long Distance I/O Link Extender in an High-Performance Process Manager that has redundant HPMMs.

Figure 2-15 Long Distance I/O Link Extender Interconnections with Redundant HPMMs



NOTE

The following High-Performance Process Manager subsystem configuration is assumed.

1. The lower HPMM card file is configured as card file #1)I/O Link address of 0).
2. The upper HPMM card file is configured as card file #2 (I/O Link address of 1).
3. Remote Site #1's IOP card file is configured as card file #3 (I/O Link address of 2).
4. Remote Site #2's IOP card file is configured as card file #4 (I/O Link address of 3).

32780

2.8 Field Termination Assembly

Description

Terminal connectors on the (FTA) provide the connection points for the process control wiring to sense, condition, or operate the connected device. Depending upon the type of FTA, fuses, relays, and resistors protect the FTA circuitry. The FTA communicates with an associated IOP, which in turn communicates with the HPMM(s).

FTAs types

Standard types of FTAs, as described in Table 2-3, interface the field wiring and provide communication with an associated IOP. They are categorized as “standard” because types of Galvanically Isolated FTAs are also available as described in Table 2-4.

Model and part numbers

The model and part numbers for available individual FTAs of each type can be found in Section 9.

Detailed descriptions

Refer to the Process Manager I/O Installation manual for a detailed description of each FTA.

Continued on next page

2.8 Field Termination Assembly, Continued

Standard FTAs Standard type FTAs are listed in Table 2-3.

Table 2-3 Standard Field Termination Assembly Types

FTA Type	Description
High Level Analog Input/ Smart Transmitter Interfac (HLAI/STI)	Accepts high level analog inputs. The inputs are configurable as single-ended or differential in relation to logic common. This FTA is also used to interface a Smart Transmitter device.
High Level Analog Inp (HLAI)	Accepts high level analog inputs. The inputs are configurable as single-ended or differential in relation to logic common.
Smart Transmitter I (STI)	Interfaces with Smart Transmitter devices. The interface is referenced to logic ground. The Smart Transmitter provides field isolation.
Low Level Anal (LLAI)	Can be configured to accept low-level or high-level analog inputs. Low-level analog inputs include Thermocouples (TC), Resistance Temperature Detectors (RTDs), or millivolt sources. High-level inputs such as voltage sources (0-5 V) and 4-20 milliamp current loop devices are acceptable.The inputs are isolated from each other and the HPM, but share a common bus for field wire shields.
Low Le Multip	The FTA accepts one set of low-level analog inputs, such as thermocouples (TC) or Resistance Temperature Detectors (RTDs). The set of inputs must be either thermocouples or RTDs. The inputs are sequentially multiplexed. One or two FTAs of either type can be connected to one Power Adapter assembly and its IOP.
	Provides 4-20 mA analog outputs to proportioning loads such as valves.
	Accepts ac digital inputs. All inputs are isolated from each other. Two versions of the FTA are available, with and without pluggable input modules.
	Similar to the 120 Vac DI FTA, except it has a higher operating voltage and a lower sense current. The inputs are in four groups of eight circuits with a common return for each group. Groups are isolated from each other.
	Accepts contacts grouped with an isolated common return. Two versions of the FTA are available, with and without pluggable input modules.
olid-State igital Output (DO)	Provides solid-state ac digital outputs that are isolated from each other and the HPM.
3-30 Vdc Solid-State Digital Statput (DO)P	r o v i d e s HPM.

Standard FTAs, continued

Table 2-3 Standard Field Termination Assembly Types, Continued

FTA Type	Description
120 Vac/125 Vdc Relay Digital Output (DO)	Provides independent electromechanical relays for ac or dc digital outputs.
240 Vac/125 Vdc Relay Digital Output (DO)	Provides independent electromechanical relays for ac or dc digital outputs.
Pulse Input (PI)	Accepts eight inputs, each with a 32-bit counter, and have a frequency range of dc to 20 kHz. The inputs are referenced to logic ground.
Serial Device Interface (SDI Toledo)	The SDI FTA provides an EIA-232 (RS-232) asynchronous serial communications interface for a model 8142-2084 or 8142-2184 Toledo Weigh Cell peripheral manufactured by Toledo Scale Inc.
Serial Device interface (SDI M/A Station)	The SDI FTA provides an EIA-422/485 (RS-422/485) asynchronous serial communications interface for up to four model MU-MASX02 Manual/Auto Station peripherals manufactured by Honeywell Inc.
Serial Device interface (SDI UDC 6000)	The SDI FTA provides an EIA-422/485 (RS-422/485) asynchronous serial communications interface for up to four UDC 6000 Modbus peripherals manufactured by Honeywell Inc.
Serial Interface (SI Modbus RTU)	The SI FTA provides either an EIA-232 (RS-232) asynchronous serial communications interface for one Modbus compatible device or an EIA-422/485 (RS-422/485) asynchronous serial communications interface for up to 15 Modbus RTU compatible devices.
Serial Interface (Allen-Bradley)	The SI FTA accommodates a single EIA-232 compatible Allen-Bradley device through its EIA-232 interface.

Galvanically isolated FTAs

Galvanically Isolated type FTAs are listed in Table 2-4.

Table 2-4 Galvanically Isolated Field Termination Assembly Types

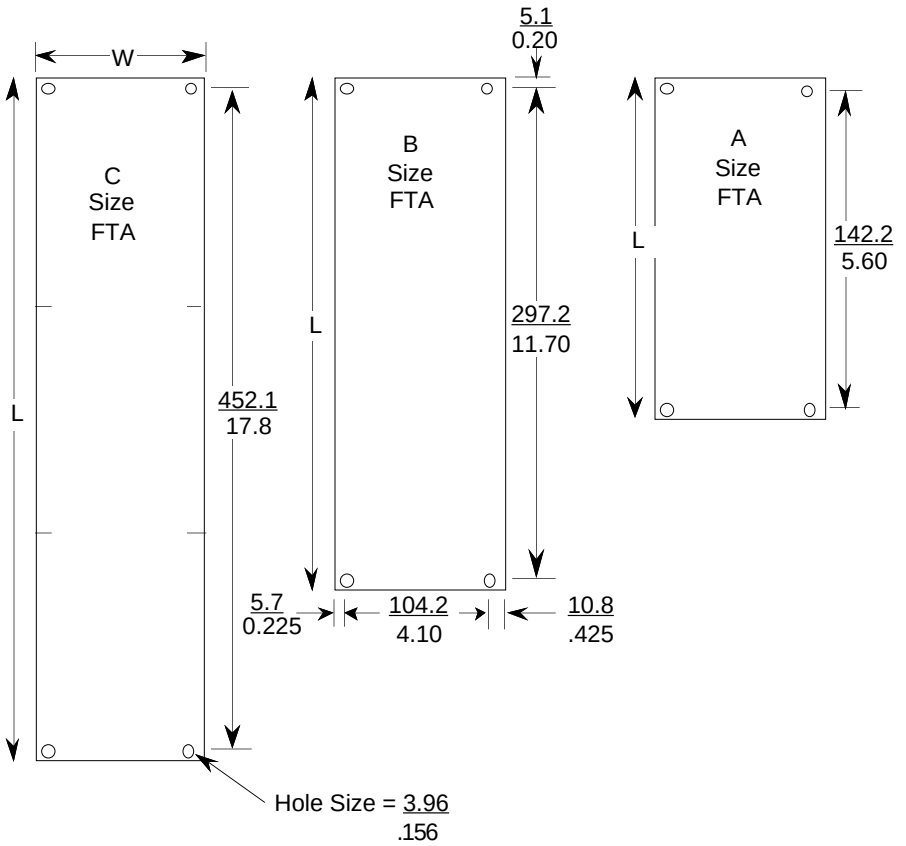
FTA Type	Description
High Level Analog Input (HLAI/STI)	The HLAI/STI FTA accepts high level analog inputs. Some FTA models also interface with Smart Transmitter devices. All inputs are isolated from ground and each other.
24 Vdc Digital Input (DI)	The 24 Vdc DI FTA accepts contact inputs. All inputs are isolated from each other.
Analog Output (AO)	The AO FTA provides isolated 4-20 mA outputs to proportioning loads such as valves.
24 Vdc Digital Output (DO)	The 24 Vdc DO FTA provides isolated digital outputs to loads such as solenoid valves or lamps.

Continued on next page

Three physical sizes

The standard FTAs have three physical sizes as illustrated in Figure 2-16. The Galvanically Isolated FTAs are one size only, B-size.

Figure 2-16 Field Termination Assembly (FTA) Sizes



Size	Length L	Width W
A	152.4/6.00	120.7/4.75
B	307.3/12.10	120.7/4.75
C	462.3/18.20	120.7/4.75

All measurements are in: millimeters / inches

Note:

The center of the mounting holes is a constant distance from the edge of the assembly board for all three FTA sizes as shown for size B.

Sizes B and C, depending on the type of FTA, can have additional mounting holes along the length (sides) of the FTA. The additional mounting holes all fall on a grid established for mounting adjacent A-size FTAs.

2770

Continued on next page

2.8 Field Termination Assembly, Continued

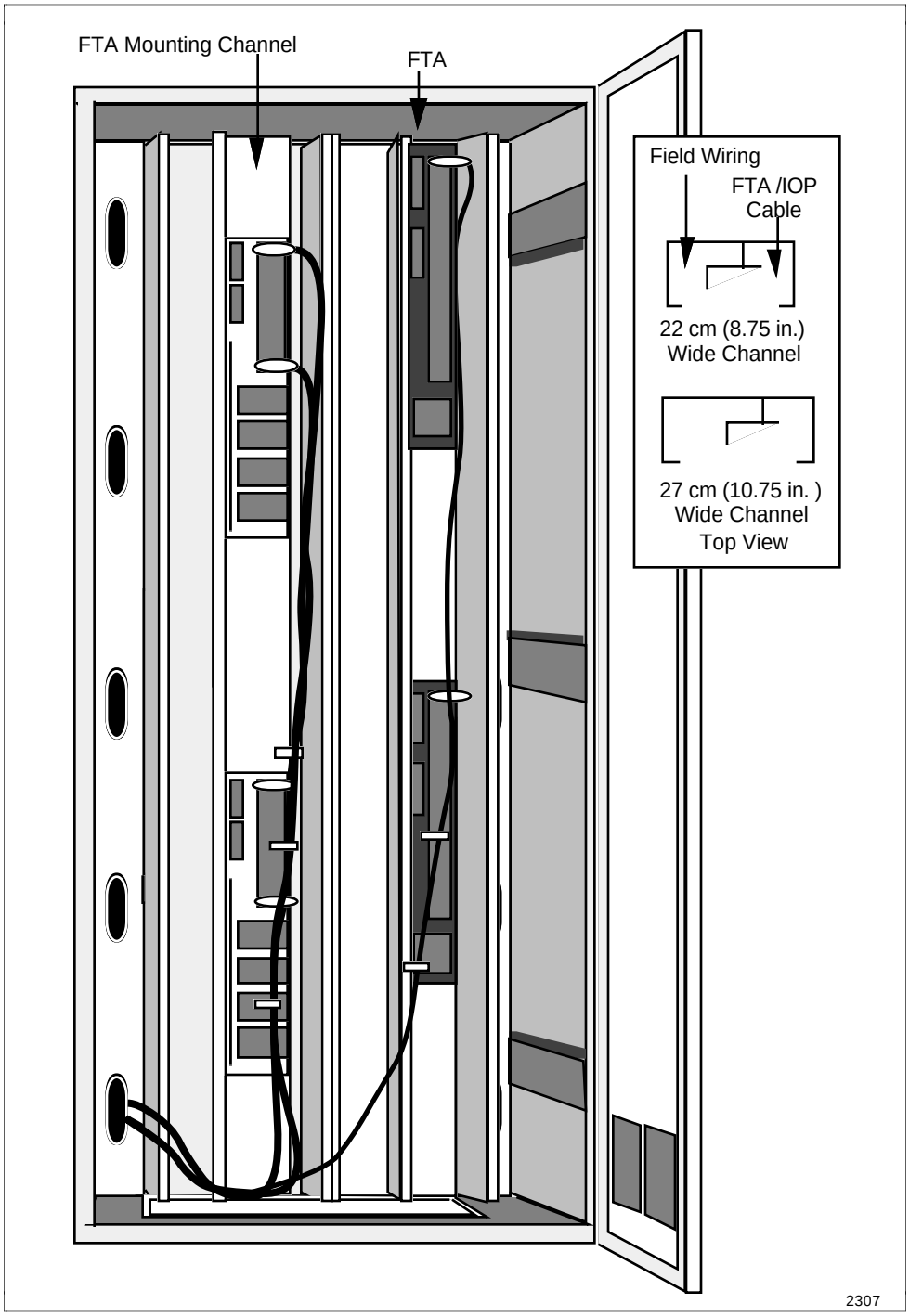
FTA Mounting Channels	The FTAs are installed at the rear or front of a dual access cabinet on one or more FTA Mounting Channels. In a single access cabinet, the FTAs are mounted on FTA Mounting Channels at the front of the cabinet. The FTA Mounting Channels also function as cable and wiring channels, or troughs. The standard and Galvanically Isolated FTAs must not be mounted on the same FTA Mounting Channel. Mounting both types of FTAs on the same FTA Mounting Channel is an intrinsic safety violation.
Vertical orientation	All FTAs except Galvanically Isolated FTAs are mounted on vertically oriented 3-foot long FTA Mounting Channel segments.
Horizontal orientation	Galvanically Isolated FTAs are mounted on horizontally oriented 2-foot long FTA Mounting Channels.

Continued on next page

Typical cabinet layout

A typical cabinet layout of FTA Mounting Channels that demonstrates the installation of standard FTAs in a dual access High-Performance Process Manager cabinet is shown in Figure 2-17.

Figure 2-17 Typical Vertical FTA Mounting Channel Layout



Continued on next page

Compression or screw terminals available

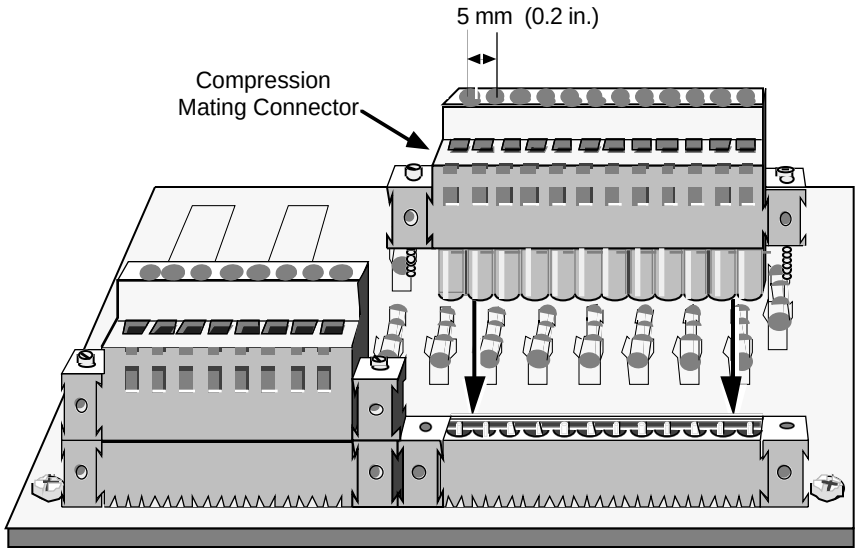
Most standard FTA types are available with either compression-type or screw-type terminal connectors. Some exceptions are the 6-inch Analog Output (AO), 6-inch High Level Analog Input (HLAI), 6-inch Low Level Analog Input Multiplexer (LLMux), and the 6-inch Digital Input Power Distribution Assembly, which are available with compression-type terminal connectors only. The number of terminals for both the compression-type and screw-type terminal connector can vary, depending on the type of standard FTA.

All Galvanically Isolated FTAs are available with both crimp pin-type and compression-type terminal connectors. The Marshalling Panel and Combiner Panel are available only with screw-type terminals.

FTA compression-type terminal connector

Figure 2-18 is an illustration of a typical compression-type terminal connector connection to a standard FTA.

Figure 2-18 Typical FTA Compression Terminal Connector



Compression Mating Connector

Number of Connections	Honeywell Part Number
8 11 12	511190694 - 108, - 208, - 408 - 111, - 411 - 112, - 412

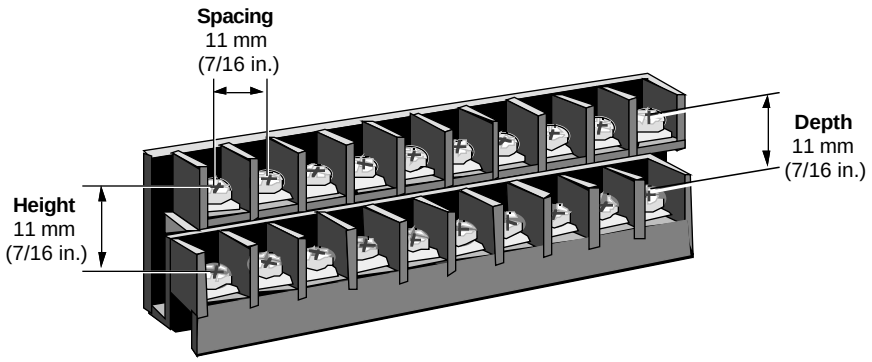
4401

Continued on next page

FTA fixed screw terminal connector

Figure 2-19 illustrates a typical fixed screw-type terminal connector as it would appear on a standard FTA.

Figure 2-19 Typical FTA Fixed Screw Terminal Connector



Screw Terminal Strip Sizes

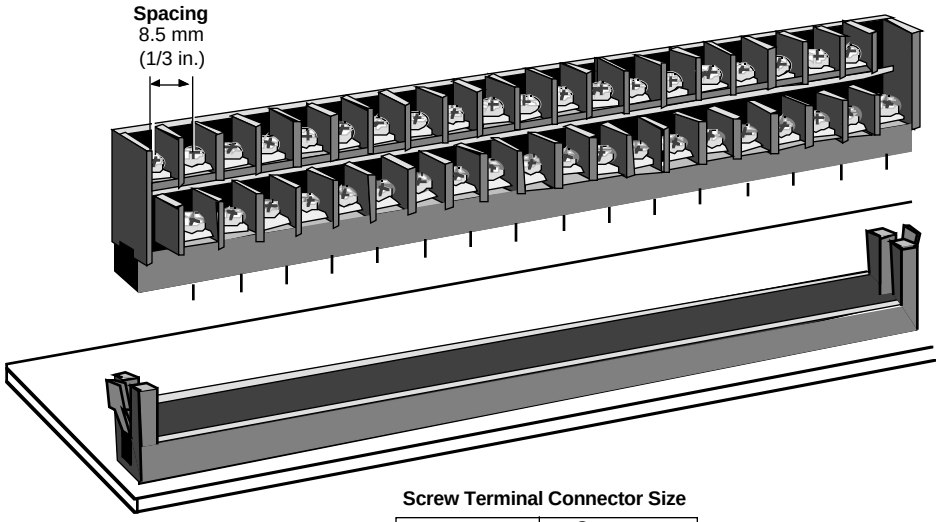
Number of Terminals	Connector Length
8	52 mm (2.0 in.)
12	74 mm (2.9 in.)
24	140 mm (5.5 in.)

4400

FTA removable screw-type connector

Figure 2-20 illustrates a typical removable screw-type terminal connector.

Figure 2-20 Typical FTA Removable Screw Terminal Connector



Screw Terminal Connector Size

Number of Terminals	Connector Length
40	176 mm (6.9 in.)

6170

Continued on next page

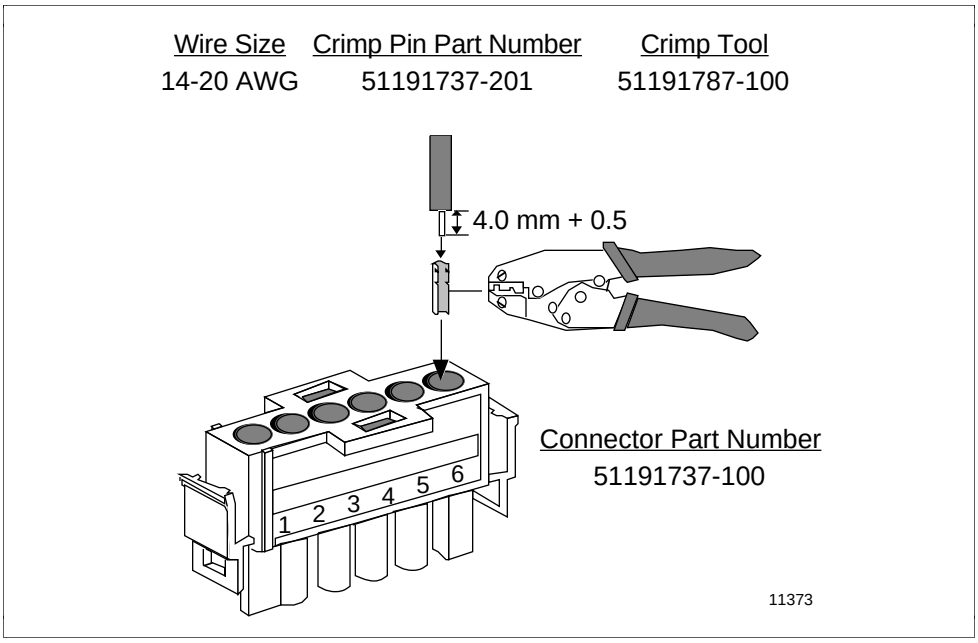
Galvanic Isolation Module connectors

Figures 2-21 and 2-22 illustrate the crimp pin-type and compression-type terminal connectors for the Galvanically Isolated FTAs, respectively. Galvanically isolated FTA terminal connectors on the Galvanic Isolation Modules have six terminals. Depending on the type of terminal connector, the terminals accept size 0.3 to 3.5 mm^2 (12 to 22 AWG) wiring.

Crimp pin-type terminal connector

Figure 2-21 illustrates the crimp pin-type Galvanic Isolation Module terminal connector.

Figure 2-21 Crimp-Type Galvanic Isolation Module Terminal Connector

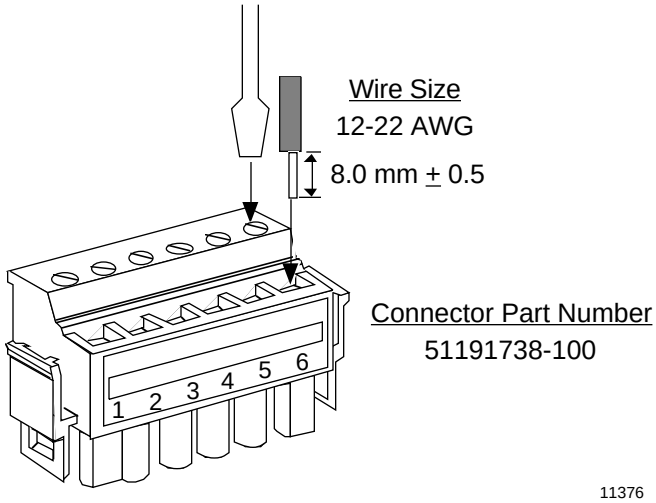


Continued on next page

Compression-type terminal connector

Figure 2-22 illustrates the compression-type Galvanic Isolation Module terminal connector.

Figure 2-22 Compression-Type Galvanic Isolation Module Terminal Connector



2.9 FTA Mounting Channels

Introduction

FTA Mounting Channels are used to support the Field Termination Assemblies (FTAs) and to organize and separate the field wiring and IOP to FTA cables.

Location

The FTAs are installed on FTA Mounting Channels that are located in the front of a single access High-Performance Process Manager cabinet, and in the rear or front of a dual access cabinet.

Number of FTA Mounting Channels

The number of FTA Mounting Channels accommodated in an High-Performance Process Manager cabinet is dependent upon whether the cabinet is single access or dual access, and whether standard or wide vertically orientated FTA Mounting Channels are installed. Horizontally orientated FTA Mounting Channels are installed when Galvanically Isolated FTAs are mounted in the cabinet.

Vertical FTA Mounting Channels

Vertical FTA Mounting Channels are available in two sizes, standard and wide, to better accommodate the amount of process control wiring that connects to the FTAs. The FTA Mounting Channels provide both a mounting surface for the FTAs and dual channels (troughs) to route the IOP to FTA cabling, and the process control wiring.

The IOP to FTA or Power Distribution Assembly cabling is routed in the right channel, and the process control wiring is routed in the left channel.

Horizontal FTA Mounting Channels

Horizontal FTA Mounting Channels are installed when Galvanically Isolated FTAs are mounted in the cabinet. Only Galvanically Isolated FTAs are to be mounted on the horizontal FTA Mounting Channels. They are approximately 61 centimeters (24 inches) long and up to eight horizontal FTA Mounting Channels can be accommodated on one side of the cabinet.

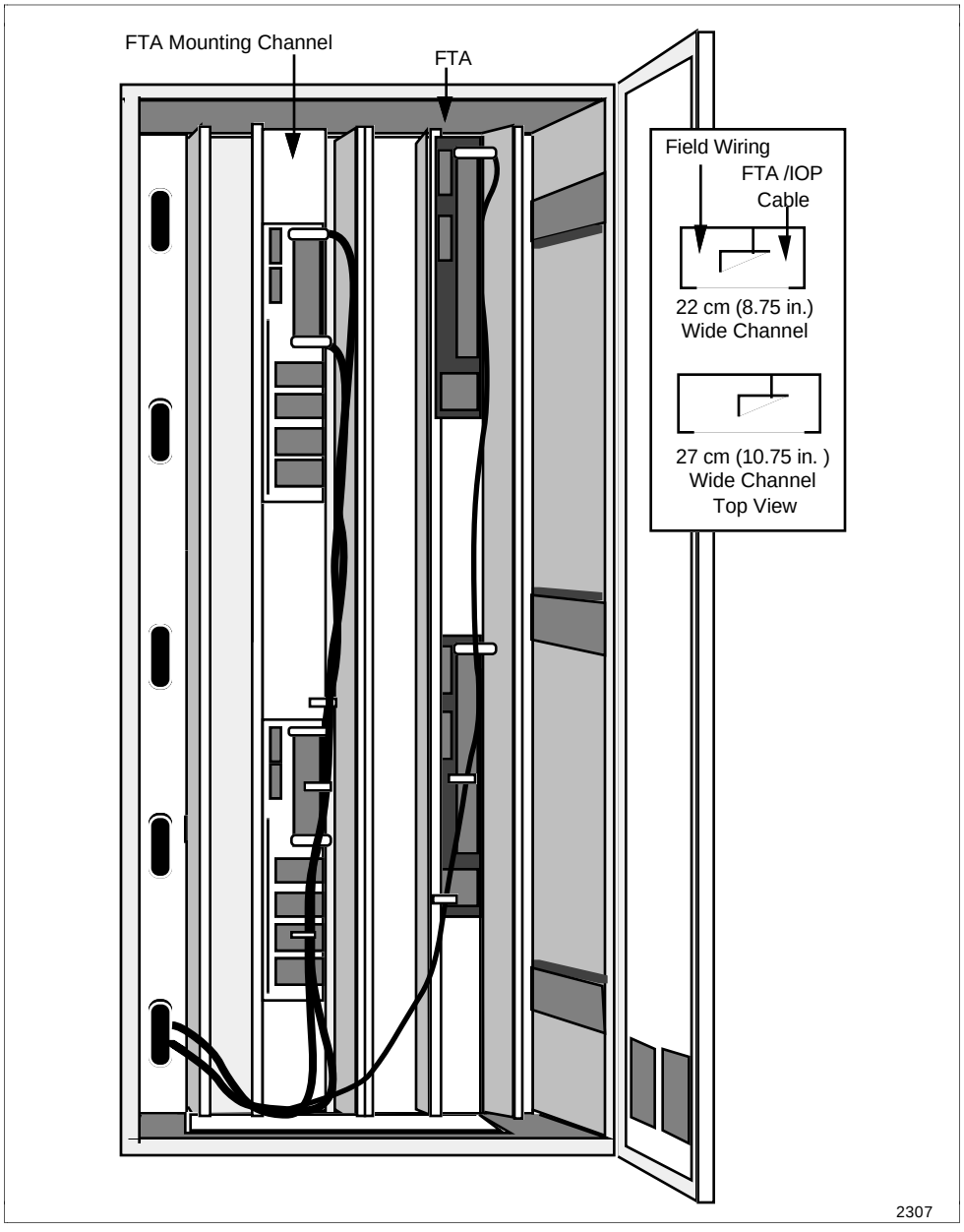
The IOP to FTA, Power Distribution Assembly, or Marshalling Panel cabling is routed in the upper channel to the left side of the cabinet, and the process control wiring is routed in the lower channel to the right side of the cabinet.

Continued on next page

Dual access cabinet installation

Figure 2-23 illustrates the installation of Vertical FTA Mounting Channels in the rear of a dual access cabinet.

Figure 2-23 Vertical FTA Mounting Channel Installation – Dual Access Cabinet

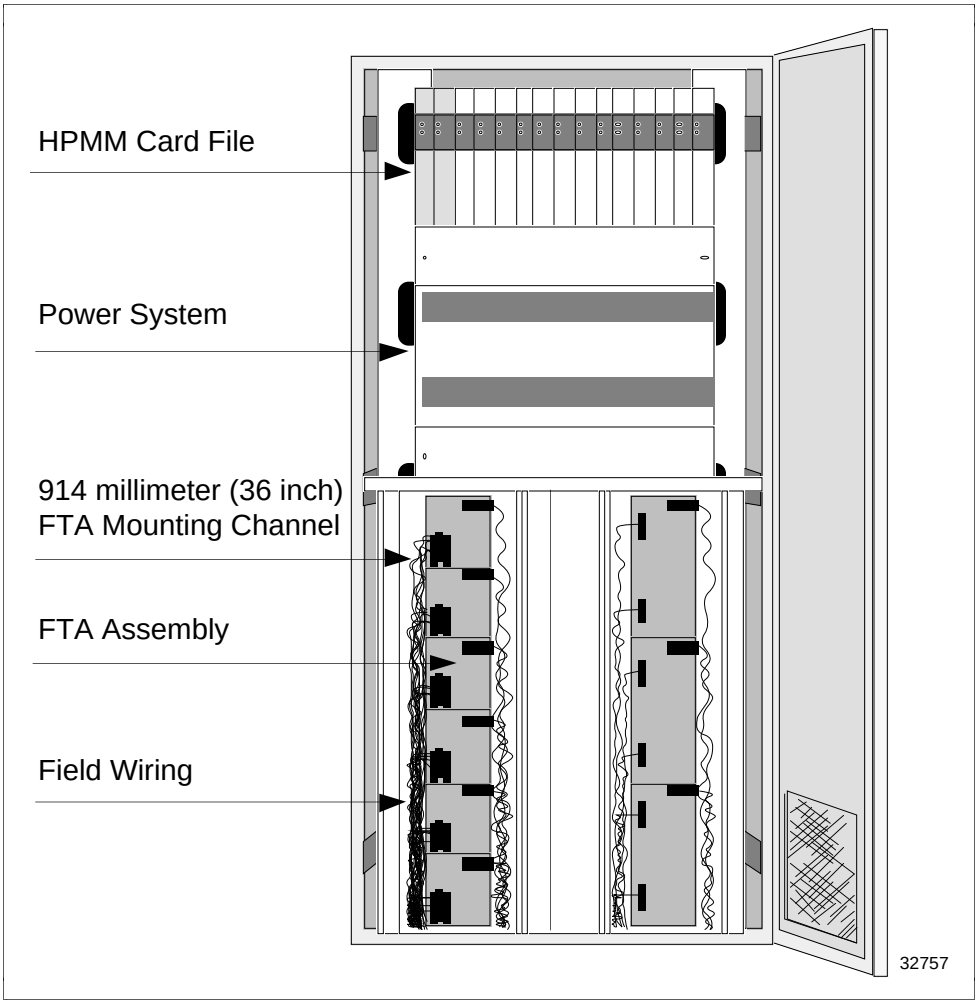


Continued on next page

Single access cabinet installation

Single Vertical FTA Mounting Channels, mounted adjacently, can be used to accept FTAs installed in the front lower area of a single access cabinet below an HPMM card file and Power System as shown in Figure 2-24.

Figure 2-24 Vertical FTA Mounting Channel Installation – Single Access Cabinet



2.10 Power Systems

Power System features

The High-Performance Process Manager Power System provides 24 Vdc power for operation of all HPMM cards, IOP cards, FTAs, a nominal 3.6 Vdc battery output for backup of the HPMM and IOP memory circuits, and a nominal 0.25 ampere, 6 Vac output for operation of a LLAI line frequency noise cancellation clock circuit. There are three types of Power Systems. They are listed below.

Power System Type	Description
Early production Standard Power System (Model MU/MC-PSSX03) (Model MU/MC-PSRX03) (Model MU/MC-PSRB03)	This power system appears in early production HPM cabinets as well as HPM cabinets that were upgraded from PM or APM configurations.
HPM Standard Power System (Model MU/MC-PSSX04) (Model MU/MC-PSRX04) (Model MU/MC-PSRB04)	An enhanced version of power system that will be incorporated some time after initial HPM cabinets are shipped. An upgrade kit for upgrading PM and APM Power Systems will be available.
AC Only Power System (optional)	This Power System is intended for use with an uninterruptible ac power source. It does **not** provide a battery backup option for continuous operation in the event of a primary power loss.

Standard Power System

The Standard Power System has many versatile attributes that include:

- An optional redundant Power Supply Module (model MU-PSRX04)
- Either 120 Vac or 240 Vac input power. A single or dual source of input power can be connected when the optional redundant Power Supply Module option is implemented
- Single and redundant Power Supply Module failure detection
- CMOS memory NiCad battery backup (3.6 Vdc) with failure detection
- An optional 48 Vdc Battery Backup Module (model MU-PSRB04) with a disconnect connector that provides continuous equipment in the event of a primary power loss
- Provides fused ac power for 4 cabinet fan assemblies

48 volt battery backup time duration

The 48 volt battery backup time duration for a redundant HPM cabinet containing redundant HPMMs and a total of 40 IOPs (40 nonredundant or 20 redundant pairs) is approximately 20 minutes for a fully charged battery.

Continued on next page

CMOS backup time duration

The following CMOS backup durations are defined for a HPM cabinet containing redundant HPMMs and a total of 40 IOPs (40 nonredundant or 20 redundant pairs). The time duration depends on which type of power system exists in the specific HPM cabinet.

- Early production Standard Power System versions = 12 hours (uses three AA size NiCad batteries) This version of power system also exists in the currently installed PM/APM cabinets.

- Enhanced HPM Standard Power System = 45 hours (uses three C size NiCad batteries)

Nearly all of the CMOS backup power is consumed by the HPMMs. A cabinet with a nonredundant HPMM will have a battery backup time of approximately double the values listed above. Adding/deleting IOPs does not affect the times to any great extent. The current draw of each IOP is almost negligible.

Honeywell does not specify that upgrading an existent PM/APM cabinet to HPM functionality must include a new power system. The user must decide if the current power system in their upgrade PM/APM cabinet provides sufficient CMOS backup time. The newer enhanced Standard Power System provides a longer CMOS backup time.

PSM redundancy requirements

Configuration rules specify that an HPM cabinet containing redundant HPMMs must have a power system with redundant Power Supply Modules.

Continued on next page

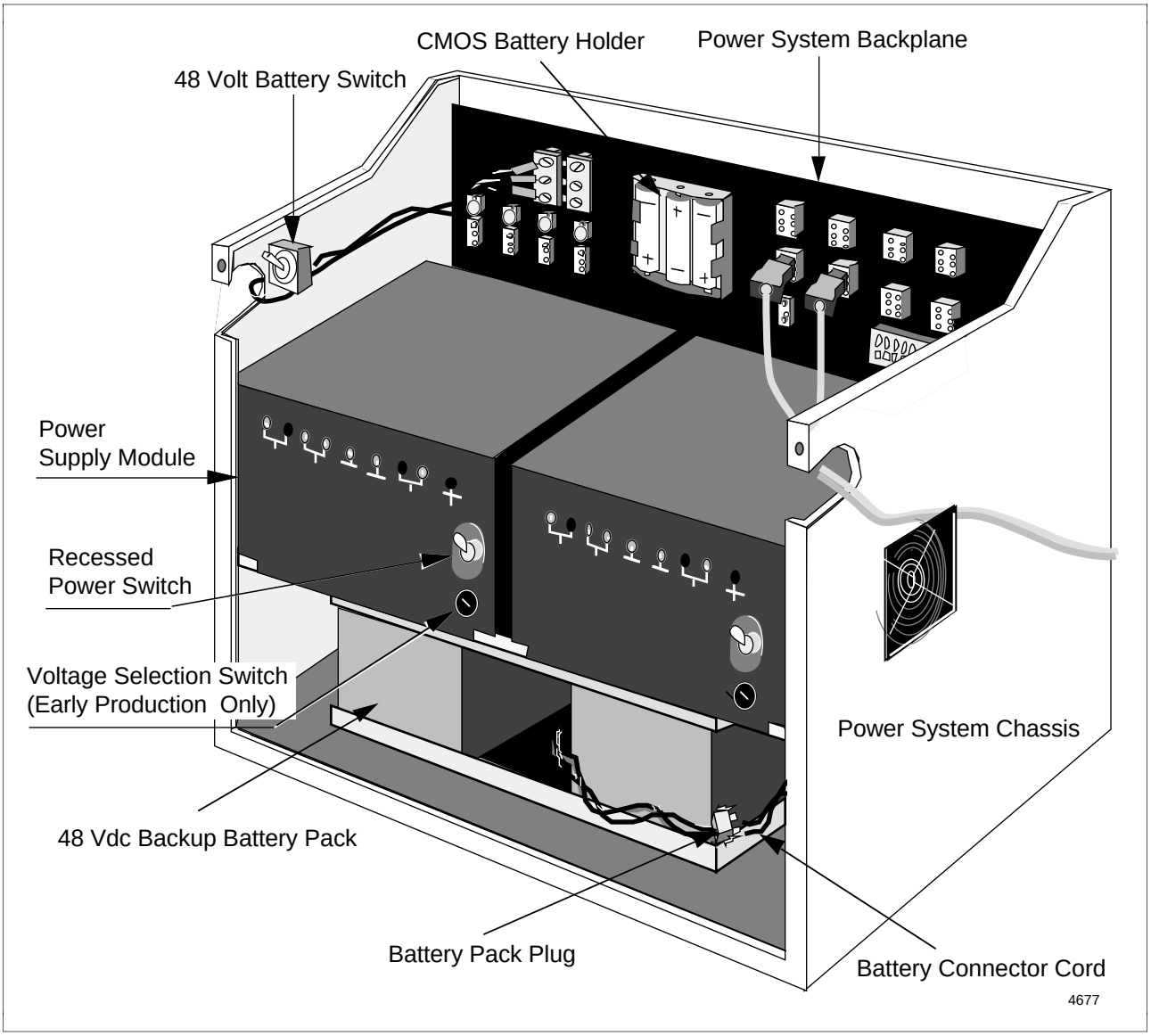
Early production Standard Power System

Figure 2-25 is an illustration of the early production Standard Power System. The Power System's connectors, terminal strips, battery and fuse holders are an integral part of the Power System backplane.

There are eight 24 Vdc power distribution output connectors, four Cabinet Fan Assembly power connectors with associated fuse holders, and a NiCad battery holder on the backplane. Sets of terminals provide alarm signals for each Power Supply Module and the CMOS Battery Backup.

The Power Supply Module in the later production Power System adjusts automatically to the input ac voltage.

Figure 2-25 Standard Power System



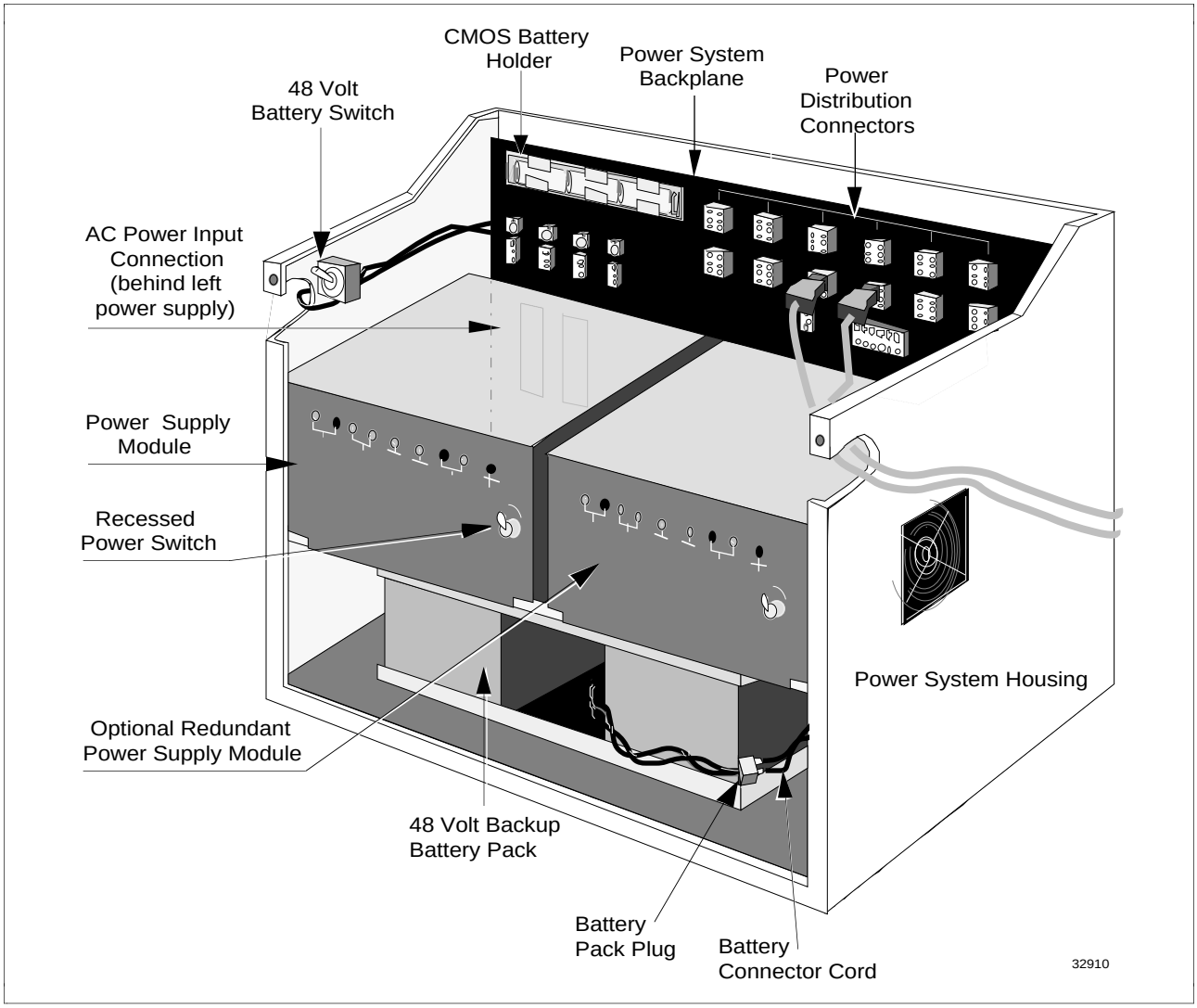
Continued on next page

HPM Standard Power System illustration

Figure 2-26 is a illustration of the enhanced HPM Standard Power System configuration that will be shipped with all new HPM cabinets in the near future. Initial HPM shipments will have an early production Standard Power System instead. The Power System's connectors, terminal strips, battery and fuse holders are an integral part of the Power System backplane.

There are twelve 24 Vdc power distribution output connectors, four Cabinet Fan Assembly power connectors with associated fuse holders, and a NiCad battery holder on the backplane. Sets of terminals provide alarm signals (for external alarm mechanisms) from each Power Supply Module and the CMOS Battery Backup. The alarm signals are normally wired in series to a 24 Vdc Digital Input FTA to notify the system when a Power Supply Module fails.

Figure 2-26 HPM Standard Power System



Continued on next page

AC Only Power System

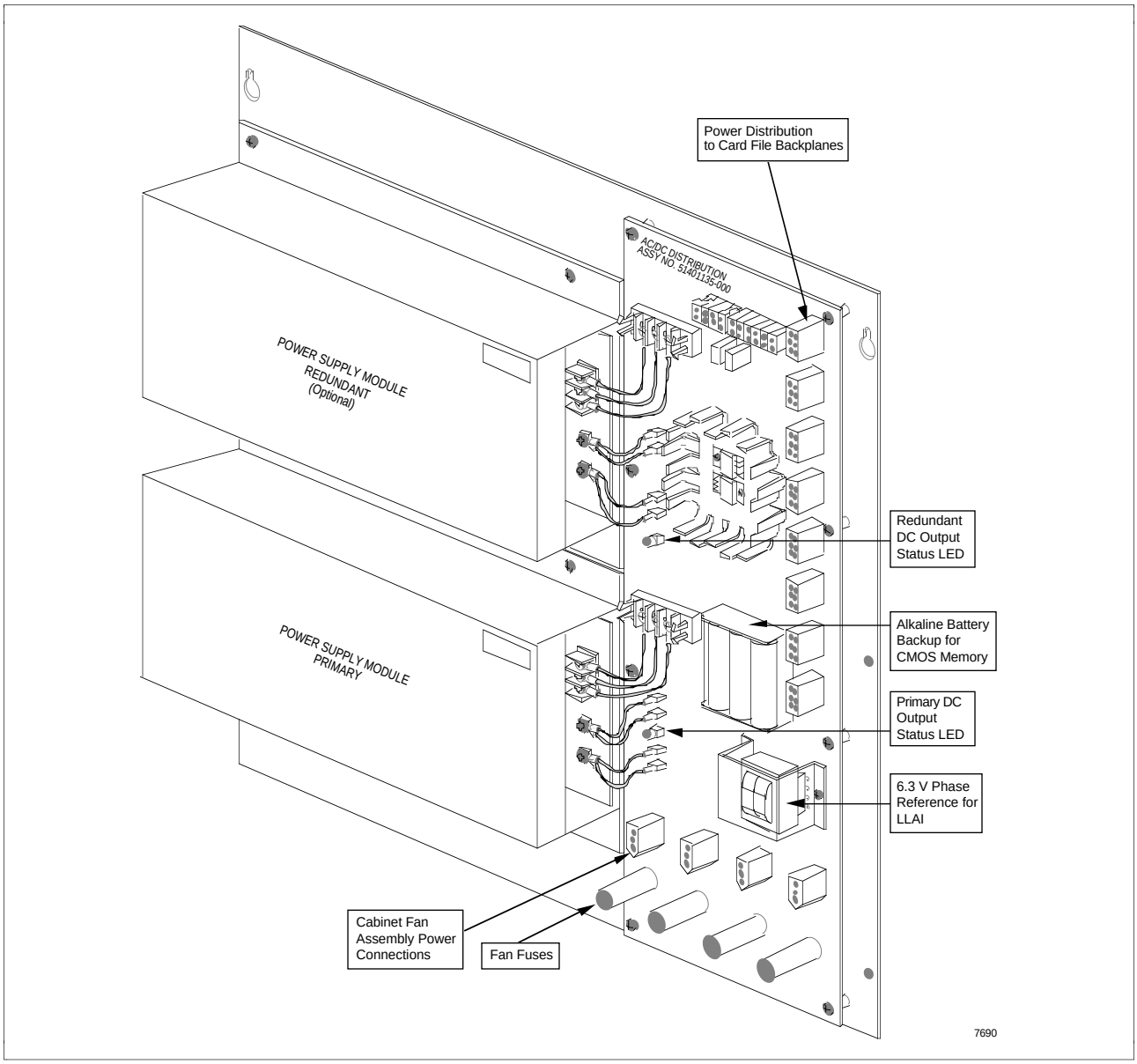
The AC Only Power System offers optional 8- or 16-ampere redundant Power Supply Modules, but does not offer the optional 48 Vdc Battery Backup module feature and rechargeable NiCad CMOS memory backup power. Nonrechargeable alkaline battery CMOS memory backup power is provided instead.

Continued on next page

AC Only Power System illustration

Figure 2-27 is an illustration of the AC Only Power System. Like the early production Standard Power System, the AC Only Power System has eight power distribution output connectors and four fused Cabinet Fan Assembly power connectors. There are two sets of normally open alarm contacts, each set operated by a relay, that signal a Power Supply Module failure. The alarm signals are normally wired in series to a 24 Vdc Digital Input FTA to notify the system when a Power Supply Module fails. Two LED indicators, mounted on the AC Only AC/DC Distribution Assembly, offer a visual indication of a Power Supply Module failure when the LED is extinguished.

Figure 2-27 AC Only Power System



2.10.1 Power Distribution

Standard Power System ac power

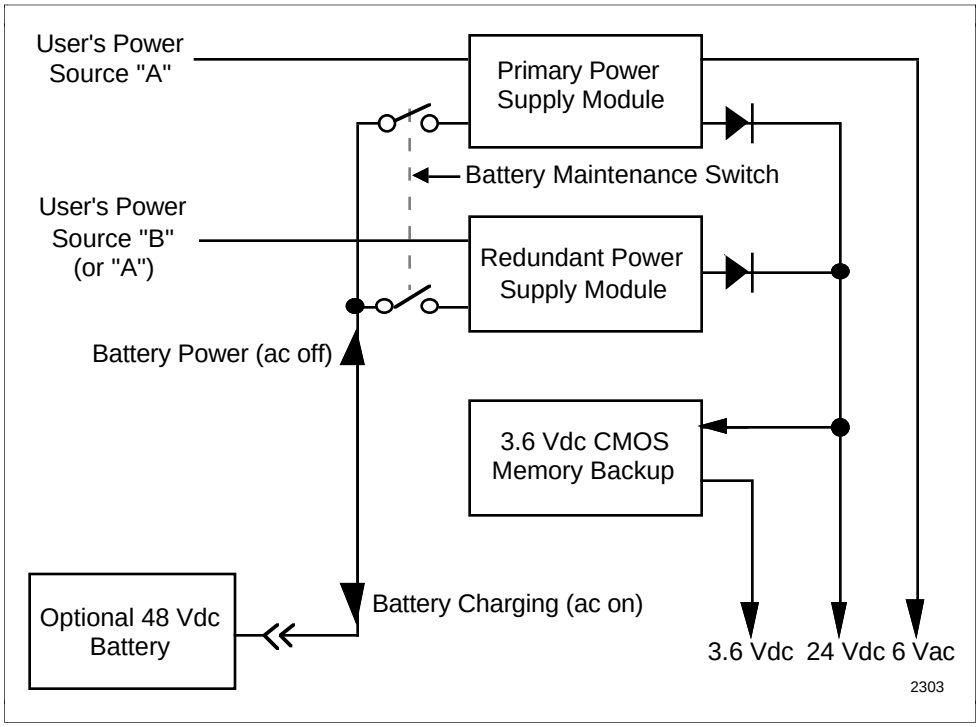
AC input power connections are made to the two AC Input terminal strips at the upper left side of the backplane in the early production Standard Power System.

The connections are located on the lower left side of the backplane, behind the left Power Supply Module, in the HPM Standard Power System.

Primary and redundant terminals can be wired in parallel from a single power line source, or wired separately from two power line sources. See Figure 2-29 or Figure 2-30.

Power distribution is illustrated in Figure 2-28.

Figure 2-28 Power Distribution



AC Only Power System ac power

AC input power connections to the AC Only Power System are made to the AC Input terminal strips at the left side of the AC/DC Distribution board as shown in Figure 2-27. The upper AC Input terminal strip powers the optional redundant Power Supply Module, and the lower AC Input terminal strip powers the primary Power Supply Module. Like the Standard Power System, the primary and redundant terminals can be wired in parallel from a single power line source, or wired separately from two power line sources.

2.10.2 Battery Backup Module

Introduction

The Battery Backup Module used to power the 24 Vdc Power Supply Modules is a 48 Vdc lead acid battery that provides backup power for approximately 25 minutes with a full charge. The charging circuit is active in both Power Supply Modules whenever ac power is available to the Power Supply Module(s). At least one Power Supply Module must be present to allow the battery to supply power to the card files.

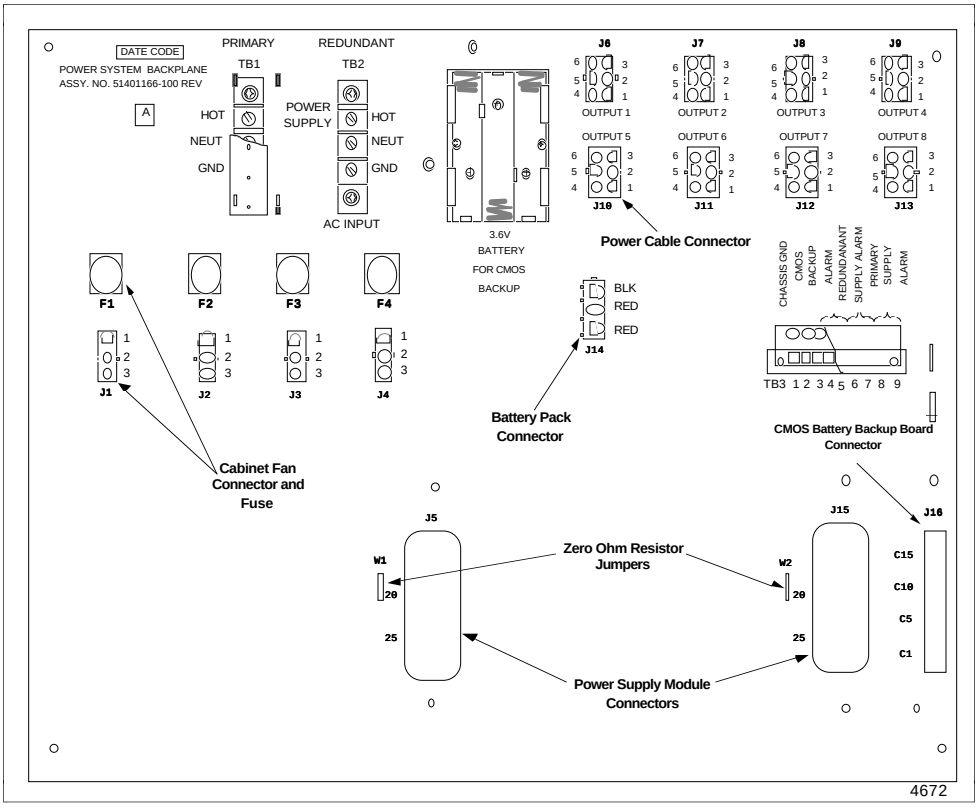
48 Volt Battery switch

A 48 Volt Battery switch that is located at the left side of the Standard Power System chassis provides a means of preventing the Power Supply Modules from discharging the Battery Backup Module when ac power is removed from one or both Power Supply Modules. Placing the switch in the off position disconnects the battery to Power Supply Module paths.

No battery backup (early production Standard Power System)

When there is no battery backup, a battery backup failure is reported unless the zero-ohm resistor jumpers, W1 and W2, located next to the Power Supply Module connectors, are cut. This is done at the factory before shipping. If a battery backup is later installed, the connections must be restored. Figure 2-29 is a view of the Standard Power System backplane.

Figure 2-29 Standard Power System Backplane (Early Production)

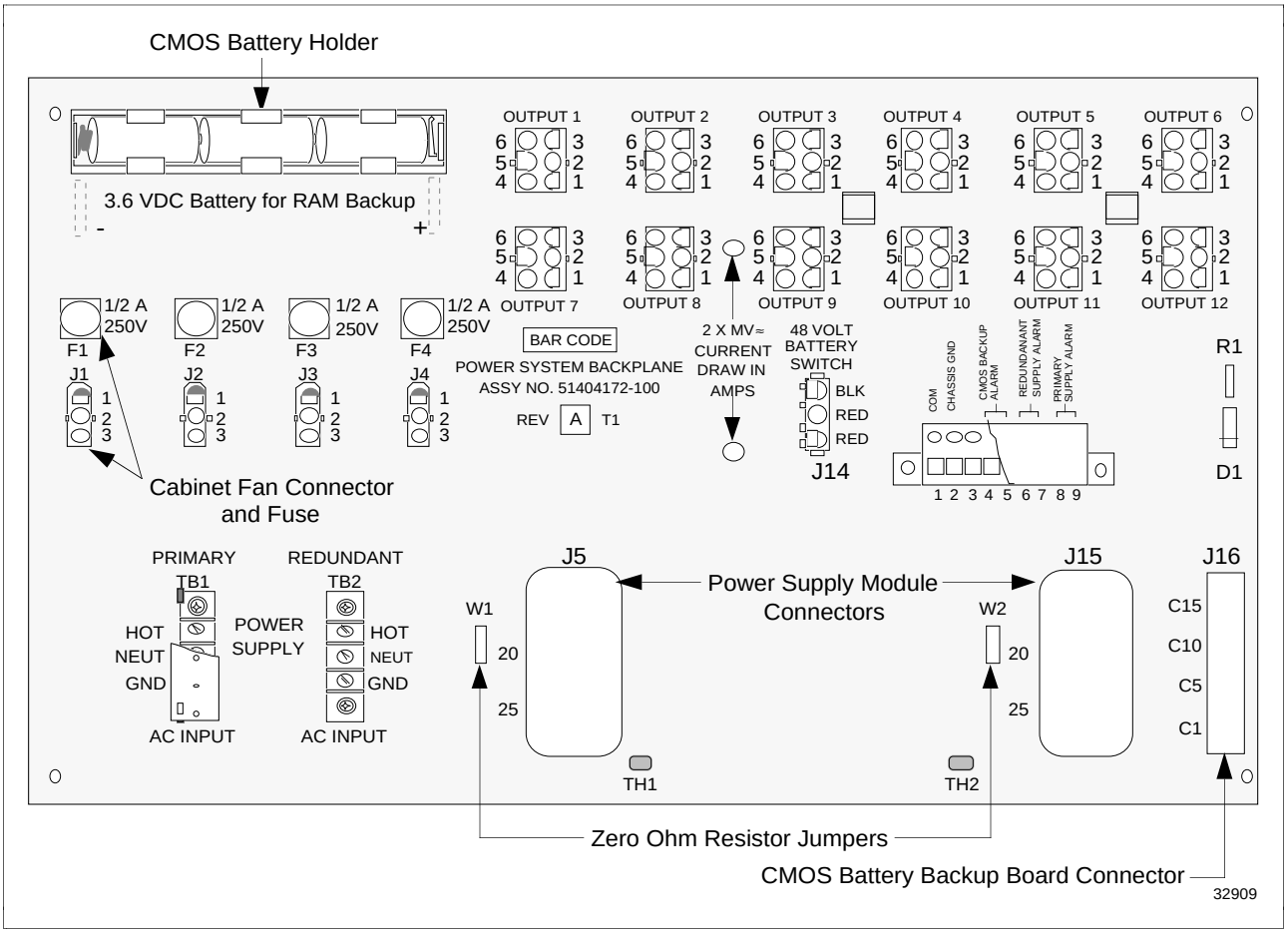


Continued on next page

No battery backup (HPM Standard Power System)

When there is no battery backup, a battery backup failure is reported unless the zero-ohm resistor jumpers, W1 and W2, located next to the Power Supply Module connectors, are cut. This is done at the factory before shipping. If a battery backup is later installed, the connections must be restored. Figure 2-30 is a view of the HPM Standard Power System backplane.

Figure 2-30 HPM Standard Power System Backplane



2.10.3 CMOS Battery Backup

Introduction

Depending on the Power System configuration, three rechargeable NiCad or three nonrechargeable alkaline batteries provide a nominal 3.6 Vdc for CMOS memory backup power. The batteries support all the memory circuits in the HPMM(s) and IOPs. NiCad batteries are long-lived, and they are automatically tested periodically. Every 8 seconds the batteries' output voltage is tested for the proper level, and every 2 hours a load is applied to the batteries and the voltage level is again tested.

The early production Standard Power System uses 3 “AA” size NiCad batteries which provide approximately 12 hours of backup. The enhanced Standard HPM Power System uses 3 “C” size NiCad batteries which provide approximately 45 hours of backup.

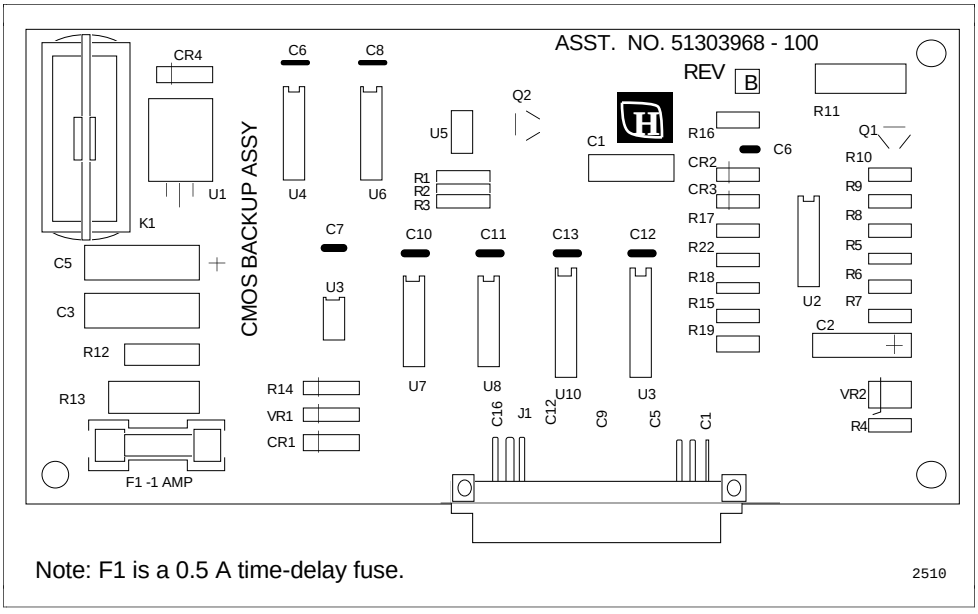
Standard Power System (early production)

Refer to Figure 2-29 for the location of the CMOS Battery Backup Assembly mating connector on the backplane.

The early production Standard Power System has NiCad batteries located at the upper center of the Power System chassis backplane, and the supporting CMOS Battery Backup Assembly is inserted into a connector at the lower right-hand side of the backplane. The right Power Supply Module must be removed to view the assembly. The assembly provides both charging circuitry and a monitoring circuitry for failure alarm reporting.

See Figure 2-31 for an illustration of the CMOS Battery Backup Assembly.

Figure 2-31 CMOS Battery Backup Assembly (Early Production)



Continued on next page

2.10.3 CMOS Battery Backup, Continued

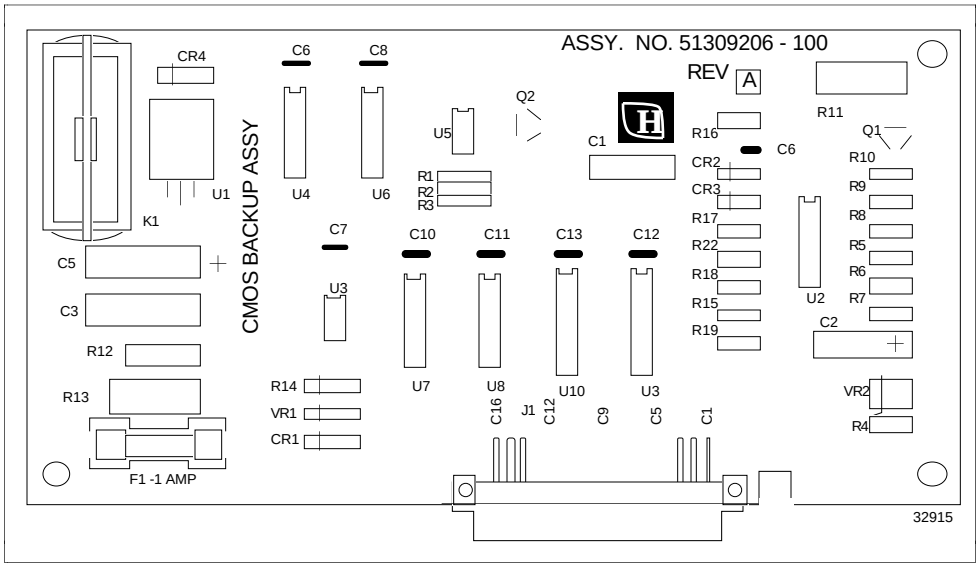
HPM Standard Power System

Refer to Figure 2-30 for the location of the CMOS Battery Backup Assembly mating connector on the backplane.

The Standard Power System configuration has NiCad batteries located at the upper left of the Power System chassis backplane, and the supporting CMOS Battery Backup Assembly is inserted into a connector at the lower right-hand side of the backplane. The right Power Supply Module must be removed to view the assembly. The assembly provides both charging circuitry and a monitoring circuitry for failure alarm reporting. The new version (CMOS Battery Backup Assembly) is backward compatible with the early production version. The older version is not forward compatible.

See Figure 2-32 for an illustration of the latest version of CMOS Battery Backup Assembly.

Figure 2-32 CMOS Battery Backup Assembly (HPM Standard Power System)



ATTENTION

ATTENTION—A bad batteries alarm occurs when the CMOS batteries are discharged or when a High-Performance Comm/Control card is not present in an HPMM card file with or without power applied to the card file. Both the High-Performance Comm/Control and the High-Performance I/O Link cards must either be present or absent in order to charge the batteries.

AC Only Power System

The AC Only Power System uses alkaline batteries which must be replaced frequently. The three alkaline batteries are located at the center of the AC/DC Distribution Assembly as shown in Figure 2-27. No charging circuitry or monitoring circuitry for failure alarm reporting exists.

A new set of batteries will provide approximately 55 hours of backup time.

2.10.4 24 Vdc Power Distribution

Dual power distribution cables

To improve reliability, 24 Vdc distribution to the card files is always provided by two power distribution cables.

Standard Power System

The early production Standard Power System provides eight 6-pin connectors located on its backplane. Three card files and a Digital Input Power Distribution Assembly or Galvanic Isolation Power Distribution Assembly can be redundantly powered.

The enhanced HPM Standard Power System provides twelve 6-pin connectors located on its backplane. This allows a greater flexibility in providing power to card files and Power Distribution assemblies.

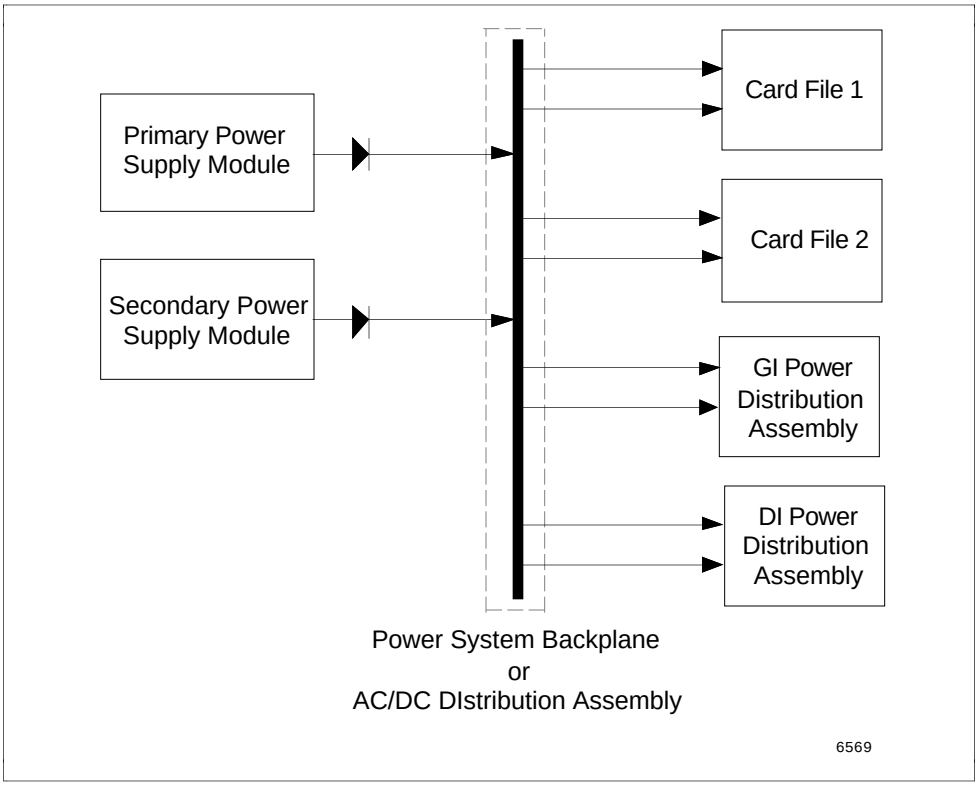
AC Only Power System

The AC Only Power System also provides eight 6-pin connectors located on the AC/DC Distribution Assembly that will redundantly power three card files and a Digital Input Power Distribution Assembly or Galvanic Isolation Power Distribution Assembly.

Typical cabinet power distribution

Figure 2-33 illustrates the typical 24 Vdc cabinet power distribution to the card files, Digital Input Power Distribution Assembly, and Galvanic Isolation Power Distribution Assembly for the various Power System configurations.

Figure 2-33 Typical Cabinet 24 Vdc Power Distribution



2.10.5 Cabinet Fan Assembly

Introduction

Fused 0.5 A 120 Vac or 240 Vac power is provided by the Power System for Cabinet Fan assembly operation.

Up to four Cabinet Fan assemblies

Up to four Cabinet Fan assemblies can be powered by the 120 Vac or 240 Vac provided by the four 3-pin connectors of the Standard or AC Only Power System configurations. The connectors and fuses are located at the left side of the Standard Power System backplane and at the bottom of the AC Only Power System AC/DC Distribution assembly. See Figure 2-25, 2-26, or 27, respectively.

Optional Cabinet Fan assembly

An optional Cabinet Fan assembly has an LED indicator that indicates normal operation of both fans, and an alarm signal, represented by normally open contacts, is available at a terminal strip, TB1. The contacts are closed when the Cabinet Fan assembly is operating normally. The operation of the Cabinet Fan assembly can be monitored by a 24 Vdc Digital Input FTA, by providing the alarm 24 Vdc signal source from the FTA and returning it to the FTA through the alarm contacts.

2.10.6 LLAI Line Frequency Clock Voltage

Introduction

The Power System provides a nominal 6 Vac half-wave rectified phase reference signal to the High-Performance Process Manager card file assemblies through the Power Distribution cable. A pluggable solid-state optical coupler module, U1, on each type of card file backplane generates this line frequency phase reference signal. It is located at the bottom right of a 7-slot card file backplane and in a similar position on the 15 slot card file. Its 6 Vac output is routed to the Low Level Analog Input (LLAI) IOPs through Power Distribution cables and card file backplanes. The signal is used by the IOPs to improve the common and normal mode noise rejection ratio.

Standard Power System

In the Standard Power System configuration, the Power Supply Module located at the left side of the assembly is the source of the line frequency phase reference signal. If the left Power Supply Module is removed, the LLAI IOPs in the same cabinet will report a Soft failure and continue to operate, but at lesser degree of accuracy.

AC Only Power System

The line frequency phase reference signal in the AC Only Power System configuration is not dependent upon the presence of the left or right side Power Supply Modules, since a constant voltage is supplied by the AC/DC Distribution Assembly.

2.10.7 24 Vdc Fuse Protection

Card file fusing

Fuse protection is provided for the four types of card files. The following protection philosophy applies for both the 7-Slot, 15-Slot, and IOP Only card files.

- The individual IOP card and an associated standard FTA are protected by a common fast-action fuse that is located on the backplane. The fuse has a 2 A rating.
- In addition to the 2 A protection, each individual IOP card has fast-action 0.5 A fuse protection that is located on the card. The fast-action 0.5 A fuse is soldered in place and is not field replaceable. You must replace the IOP card.
- Both HPMM cards, High-Performance Communications/Control and High-Performance I/O Link, and the HPM UCN Interface module are protected by a fast-action 3.2 A fuse that is located on the High-Performance I/O Link card. The fuse is field replaceable.
- A fast-action 2.0 A fuse protects the LLAI optical coupler module on the backplane, U1. It generates the line frequency phase reference signal that is used by LLAI IOPs.

Left 7-Slot card file

Table 2-5 lists the individual backplane fuses and their application for the Left 7-Slot card file. The fuse rating is 2 A for fuse locations F1 through F8.

Continued on next page

2.10.7 24 Vdc Fuse Protection, Continued

Fuse application

When HPMM cards occupy the left two slots of a card file, fuse F2 is not in use. Fuse F1 on the backplane is used to supply 24 Vdc to the UCN Interface Module.

Table 2-5 Left 7-Slot Card File Fuse Protection

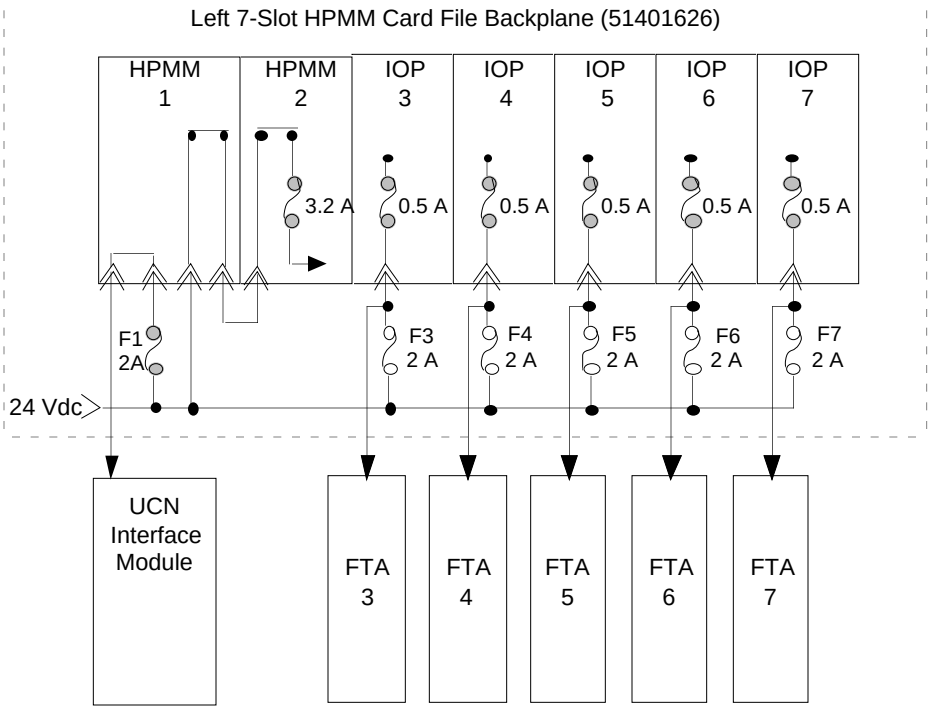
Fuse	Rating	Protection Application
F1	2 A fast-action	Slot 1 IOP card and associated FTA or UCN Interface Module (24 Vdc) if HPMM exists in card file
F2	2 A fast-action	Slot 2 IOP card and associated FTA
F3	2 A fast-action	Slot 3 IOP card and associated FTA
F4	2 A fast-action	Slot 4 IOP card and associated FTA
F5	2 A fast-action	Slot 5 IOP card and associated FTA
F6	2 A fast-action	Slot 6 IOP card and associated FTA
F7	2 A fast-action	Slot 7 IOP card and associated FTA
F8	2 A fast-action	HLAI Optical Coupler Module, U1

Continued on next page

Left 7-Slot HPMM card file 24 Vdc distribution

Figure 2-34 illustrates the 24 Vdc power distribution on the Left 7-Slot HPMM card file backplane.

Figure 2-34 Left 7-Slot HPMM Card File Backplane 24 Vdc Distribution



Notes:

A fast-action 2 A fuse that is located on the backplane protects each IOP/nongalvanically isolated FTA combination.

A fast-action 0.5 A fuse that is located on the IOP card protects the IOP card.

A fast-action 3.2 A fuse that is located on the High-Performance I/O Link card protects the HPMM cards and HPM UCN Interface module.

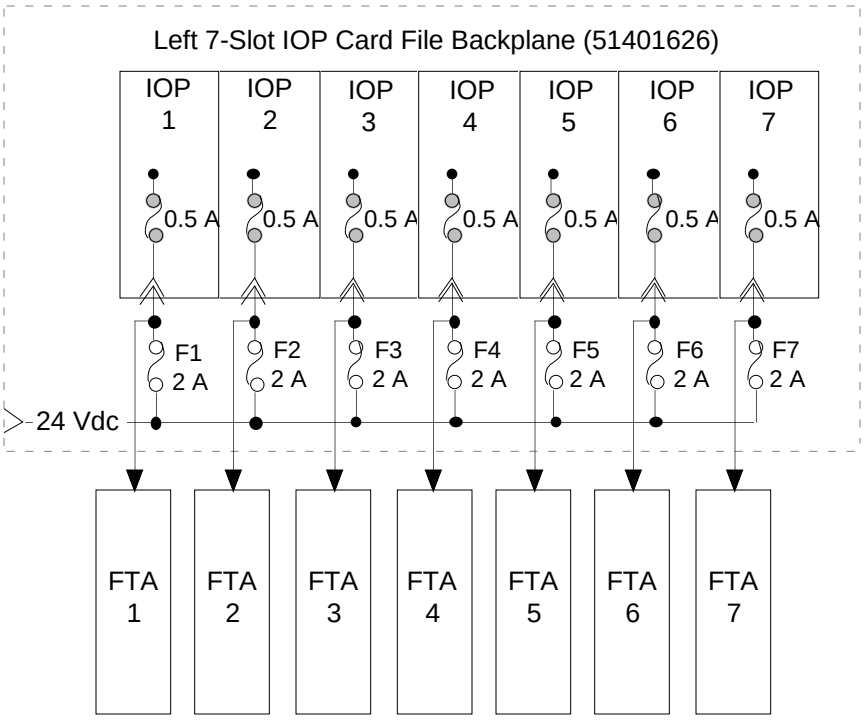
32764

Continued on next page

Left 7-Slot IOP card file 24 Vdc distribution

Figure 2-35 illustrates the 24 Vdc power distribution on the Left 7-Slot IOP card file backplane.

Figure 2-35 Left 7-Slot IOP Card File Backplane 24 Vdc Distribution



Notes:

A fast-action 2 A fuse that is located on the backplane protects each IOP/nongalvanically isolated FTA combination.

A fast-action 0.5 A fuse that is located on the IOP card protects the IOP card.

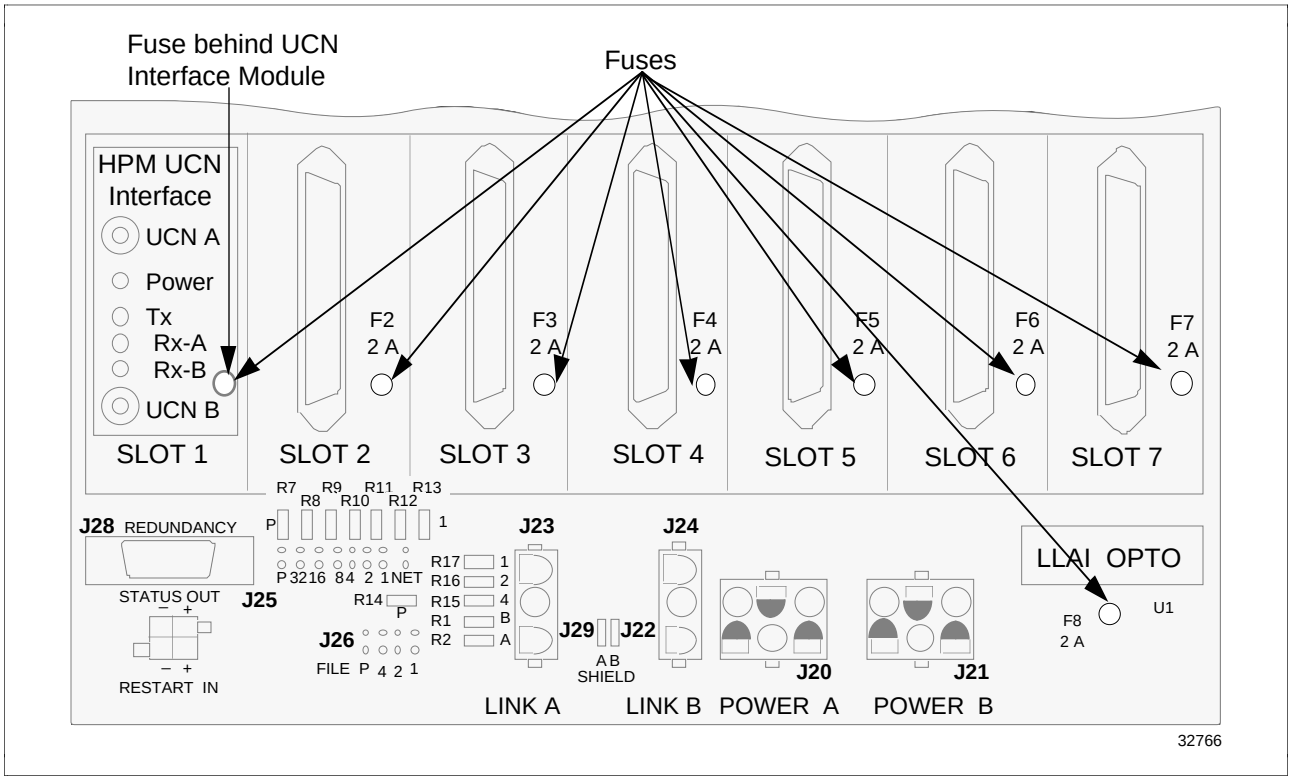
32765

Continued on next page

Left 7-Slot card file backplane fuse locations

Figure 2-36 illustrates the locations of the individual fuses on the Left 7-Slot card file backplane.

Figure 2-36 Left 7-Slot Card File Backplane Fuse Locations



Continued on next page

2.10.7 24 Vdc Fuse Protection, Continued

Right 7-Slot card file

Table 2-6 lists the individual backplane fuses and their application for the Right 7-Slot card file. The fuse rating is 2 A for fuse locations F1 through F8.

Fuse application

When HPMM cards occupy the left two slots of a card file, fuse F2 is not in use. Fuse F1 on the backplane is used to supply 24 Vdc to the UCN Interface Module.

Table 2-6 Right 7-Slot Card File Backplane Fuse Protection

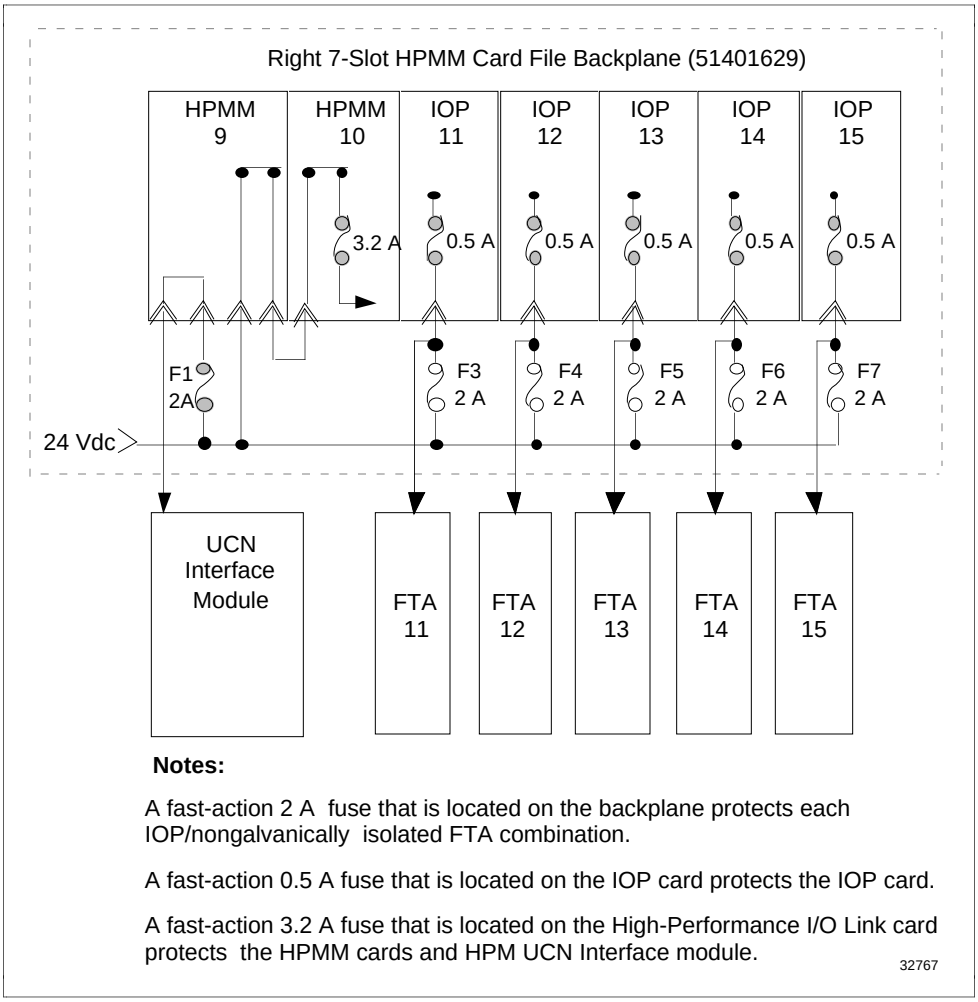
Fuse	Rating	Protection Application
F1	2 A fast-action	Slot 9 IOP card and associated FTA or UCN Interface Module (24 Vdc) if HPMM exists in card file
F2	2 A fast-action	Slot 10 IOP card and associated FTA
F3	2 A fast-action	Slot 11 IOP card and associated FTA
F4	2 A fast-action	Slot 12 IOP card and associated FTA
F5	2 A fast-action	Slot 13 IOP card and associated FTA
F6	2 A fast-action	Slot 14 IOP card and associated FTA
F7	2 A fast-action	Slot 15 IOP card and associated FTA
F8	2 A fast-action	HLAI Optical Coupler Module, U1

Continued on next page

Right 7-Slot HPMM card file 24 Vdc distribution

Figure 2-37 illustrates the 24 Vdc power distribution on the Right 7-Slot HPMM card file backplane.

Figure 2-37 Right 7-Slot HPMM Card File Backplane 24 Vdc Distribution

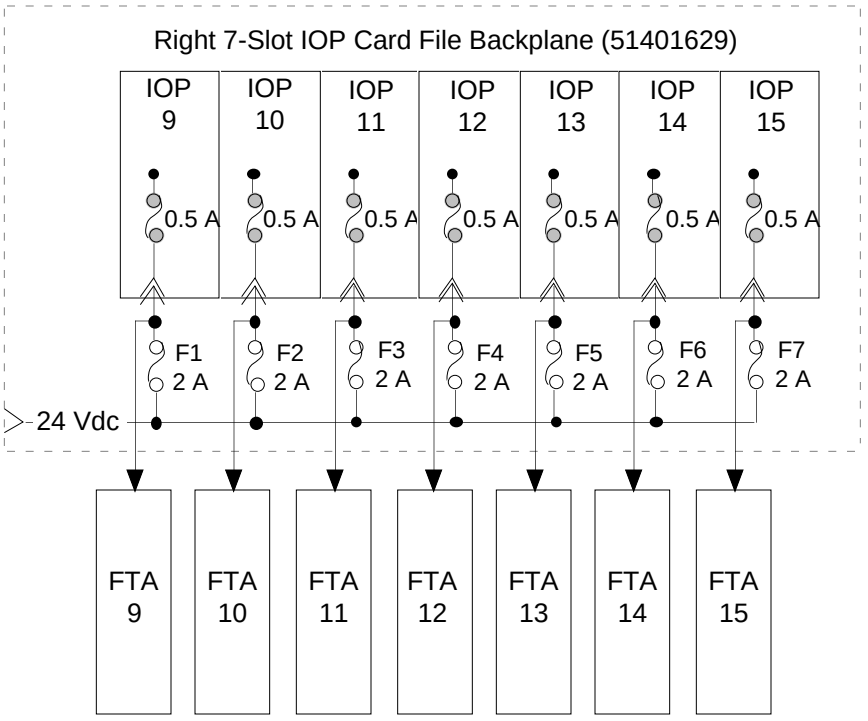


Continued on next page

Right 7-Slot IOP card file 24 Vdc distribution

Figure 2-38 illustrates the 24 Vdc power distribution on the Right 7-Slot IOP card file backplane.

Figure 2-38 Right 7-Slot IOP Card File Backplane 24 Vdc Distribution



Notes:

A fast-action 2 A fuse that is located on the backplane protects each IOP/nongalvanically isolated FTA combination.

A fast-action 0.5 A fuse that is located on the IOP card protects the IOP card.

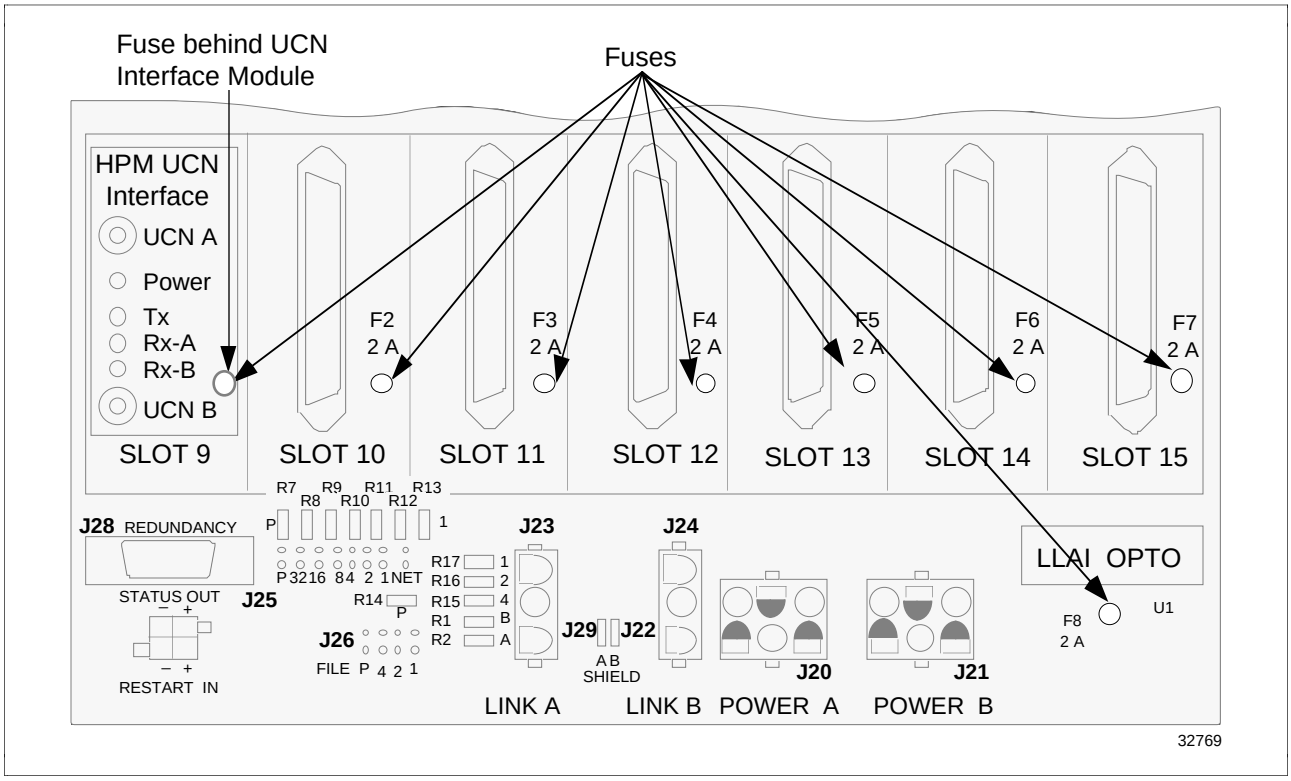
32768

Continued on next page

Right 7-Slot card file backplane fuse locations

Figure 2-39 illustrates the locations of the individual fuses on the Right 7-Slot card file backplane.

Figure 2-39 Right 7-Slot Card File Backplane Fuse Locations



Continued on next page

2.10.7 24 Vdc Fuse Protection, Continued

15-Slot card file

The 15-Slot card file provides 2 A fast-action fuse IOP card and associated standard FTA protection. The backplane assembly also provides fast-action 2.0 A fuse protection for the LLAI Optical Coupler Module on the backplane, U1.

When HPMM cards occupy the left two slots of a card file, fuse F2 is not in use. Fuse F1 on the backplane is used to supply 24 Vdc to the UCN Interface Module.

Fuse application

Table 2-7 lists the individual backplane fuses and their application for the 15-Slot card file. The fuse rating is 2 A for fuse locations F1 through F16.

Table 2-7 15-Slot Card File Backplane Fuse Protection

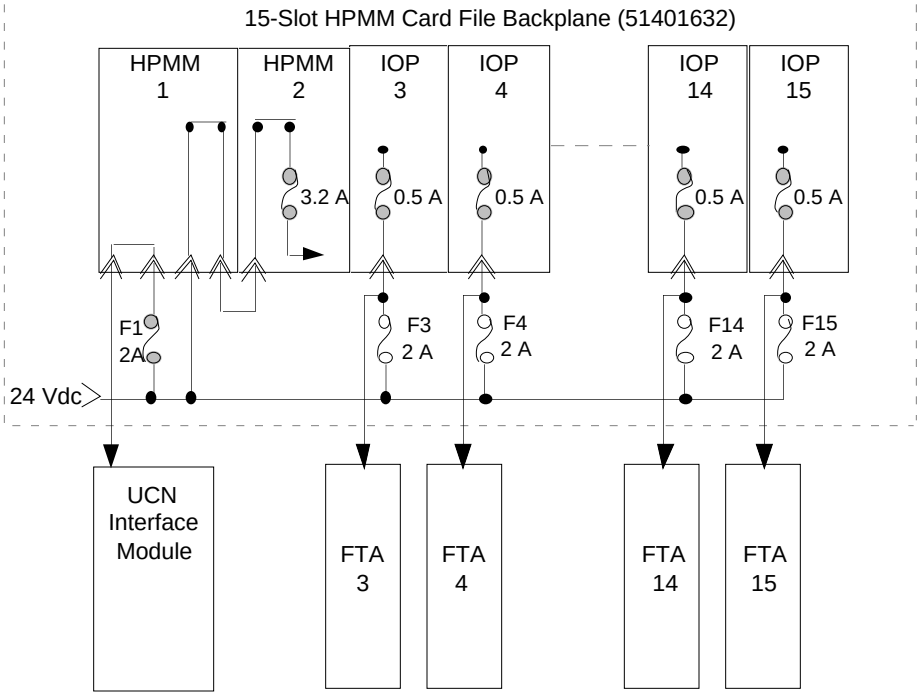
Fuse	Rating	Protection Application
F1	2 A fast-action	Slot 1 IOP card and associated FTA or UCN Interface Module (24 Vdc) if HPMM exists in card file
F2	2 A fast-action	Slot 2 IOP card and associated FTA
F3	2 A fast-action	Slot 3 IOP card and associated FTA
F4	2 A fast-action	Slot 4 IOP card and associated FTA
F5	2 A fast-action	Slot 5 IOP card and associated FTA
F6	2 A fast-action	Slot 6 IOP card and associated FTA
F7	2 A fast-action	Slot 7 IOP card and associated FTA
F8	2 A fast-action	Slot 8 IOP card and associated FTA
F9	2 A fast-action	Slot 9 IOP card and associated FTA
F10	2 A fast-action	Slot 10 IOP card and associated FTA
F11	2 A fast-action	Slot 11 IOP card and associated FTA
F12	2 A fast-action	Slot 12 IOP card and associated FTA
F13	2 A fast-action	Slot 13 IOP card and associated FTA
F14	2 A fast-action	Slot 14 IOP card and associated FTA
F15	2 A fast-action	Slot 15 IOP card and associated FTA
F16	2 A fast-action	LLAI Optical Coupler Module, U1

Continued on next page

15-Slot HPMM card file 24 Vdc distribution

Figure 2-40 illustrates the 24 Vdc power distribution on the 15-Slot HPMM card file backplane.

Figure 2-40 15-Slot HPMM Card File Backplane 24 Vdc Distribution



Notes:

A fast-action 2 A fuse that is located on the backplane protects each IOP/nongalvanically isolated FTA combination.

A fast-action 0.5 A fuse that is located on the IOP card protects the IOP card.

A fast-action 3.2 A fuse that is located on the High-Performance I/O Link card protects the HPMM cards and HPM UCN Interface module.

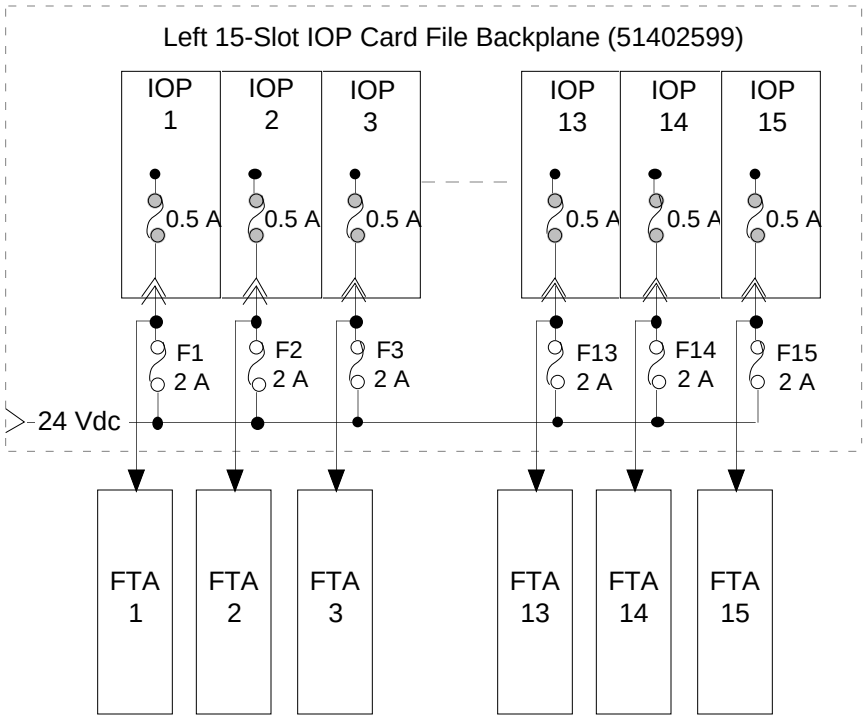
32770

Continued on next page

15-Slot IOP card file 24 Vdc distribution

Figure 2-41 illustrates the 24 Vdc power distribution on the 15-Slot IOP card file backplane.

Figure 2-41 15-Slot IOP Card File Backplane 24 Vdc Distribution



Notes:

A fast-action 2 A fuse that is located on the backplane protects each IOP/nongalvanically isolated FTA combination.

A fast-action 0.5 A fuse that is located on the IOP card protects the IOP card.

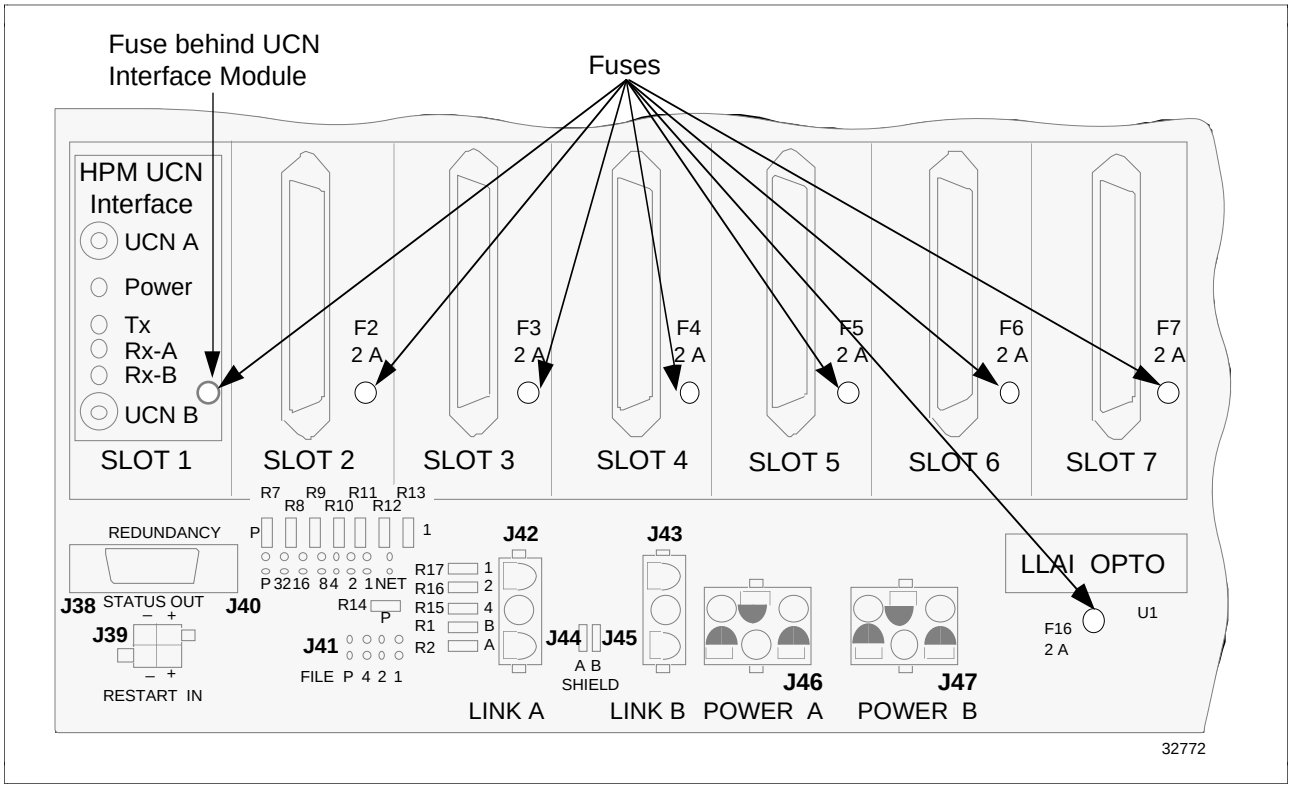
32771

Continued on next page

15-Slot card file backplane fuse locations

Figure 2-42 illustrates a portion of the locations of the individual fuses on the 15-Slot card file backplane.

Figure 2-42 15-Slot Card File Backplane Fuse Locations



Continued on next page

2.10.7 24 Vdc Fuse Protection, Continued

IOP Only card file

The "IOP Only" card file assembly used by the Process Manager and Advanced Process Manager can be used with the High-Performance Process Manager. When upgrading a PM or APM to HPM hardware, it is not necessary to also convert the IOP card file(s) to 15-Slot IOP card file(s).

IOP Only card file assemblies

An early version of the IOP Only card file did not offer card and FTA fuse protection at the backplane. This backplane can be identified by the assembly number 51401129, revision A. Later versions of the 51401129 backplane have time-delay 3 A fuse protection for the IOP card and its associated standard FTA. They are identified by assembly 51401129, revision B, or later. Assembly 51401406 and 51402599 backplanes, all revisions, have fast-action 2 A fuse card and FTA protection. All card file backplane assemblies provide a fast-action 0.5 A fuse for the LLAI optical coupler module on the backplane, U1.

Fuse application

Table 2-8 lists the individual backplane fuses and their application for the 15-Slot card file. The fuse rating is 2 A for fuse locations F1 through F16.

Table 2-8 IOP Only Card File Fuse Protection

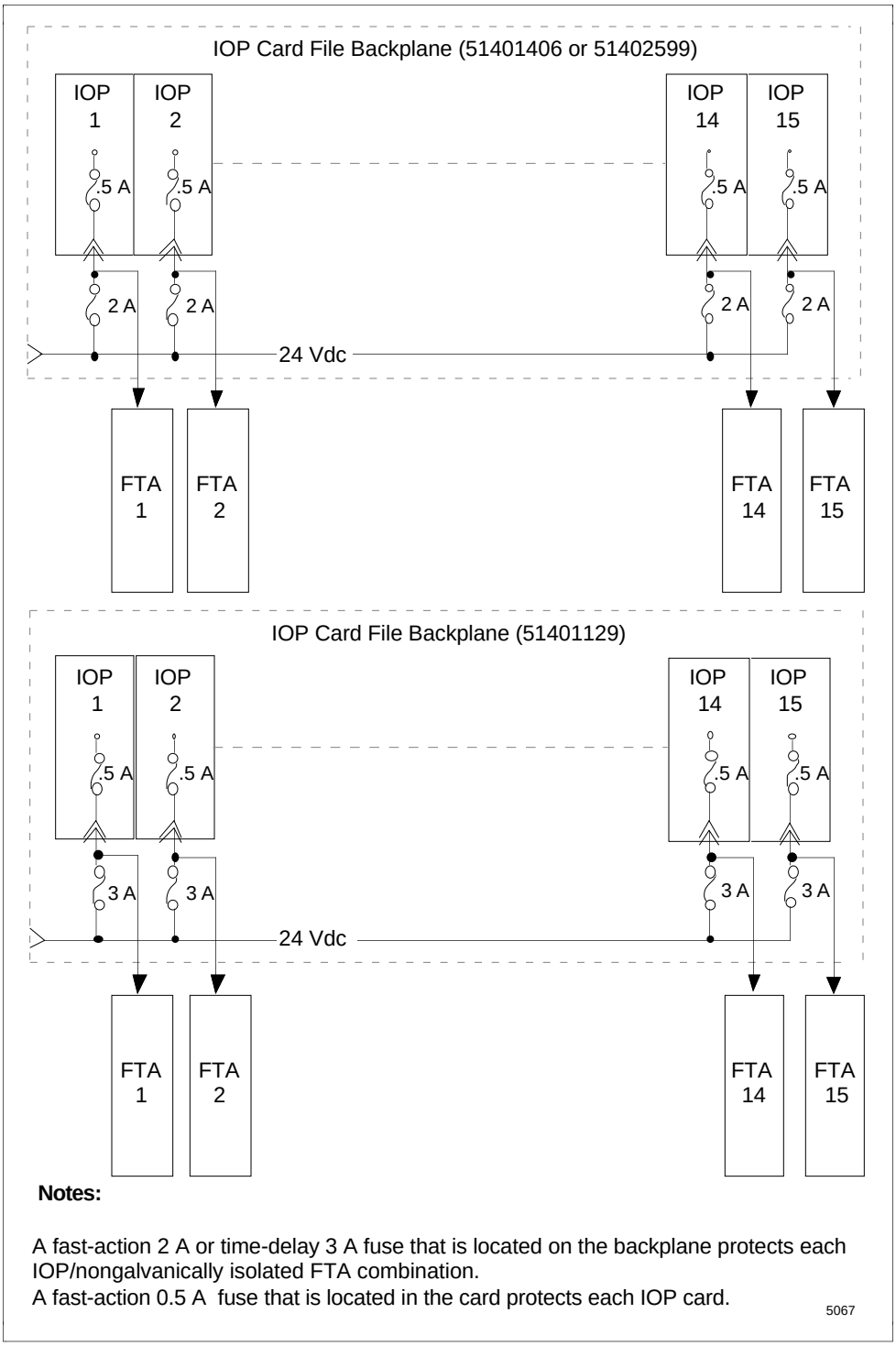
Fuse	Rating	Protection Application
F1	2 A fast-action/3 A time-delay	Slot 1 IOP card and associated FTA
F2	2 A fast-action/3 A time-delay	Slot 2 IOP card and associated FTA
F3	2 A fast-action/3 A time-delay	Slot 3 IOP card and associated FTA
F4	2 A fast-action/3 A time-delay	Slot 4 IOP card and associated FTA
F5	2 A fast-action/3 A time-delay	Slot 5 IOP card and associated FTA
F6	2 A fast-action/3 A time-delay	Slot 6 IOP card and associated FTA
F7	2 A fast-action/3 A time-delay	Slot 7 IOP card and associated FTA
F8	2 A fast-action/3 A time-delay	Slot 8 IOP card and associated FTA
F9	2 A fast-action/3 A time-delay	Slot 9 IOP card and associated FTA
F10	2 A fast-action/3 A time-delay	Slot 10 IOP card and associated FTA
F11	2 A fast-action/3 A time-delay	Slot 11 IOP card and associated FTA
F12	2 A fast-action/3 A time-delay	Slot 12 IOP card and associated FTA
F13	2 A fast-action/3 A time-delay	Slot 13 IOP card and associated FTA
F14	2 A fast-action/3 A time-delay	Slot 14 IOP card and associated FTA
F15	2 A fast-action/3 A time-delay	Slot 15 IOP card and associated FTA
F16	0.5 A fast-action	LLAI Optical Coupler Module, U1

Continued on next page

IOP Only card file 24 Vdc power distribution

Figure 2-43 illustrates the 24 Vdc power distribution on the IOP Only card file backplane.

Figure 2-43 IOP Only Card File Backplane 24 Vdc Power Distribution

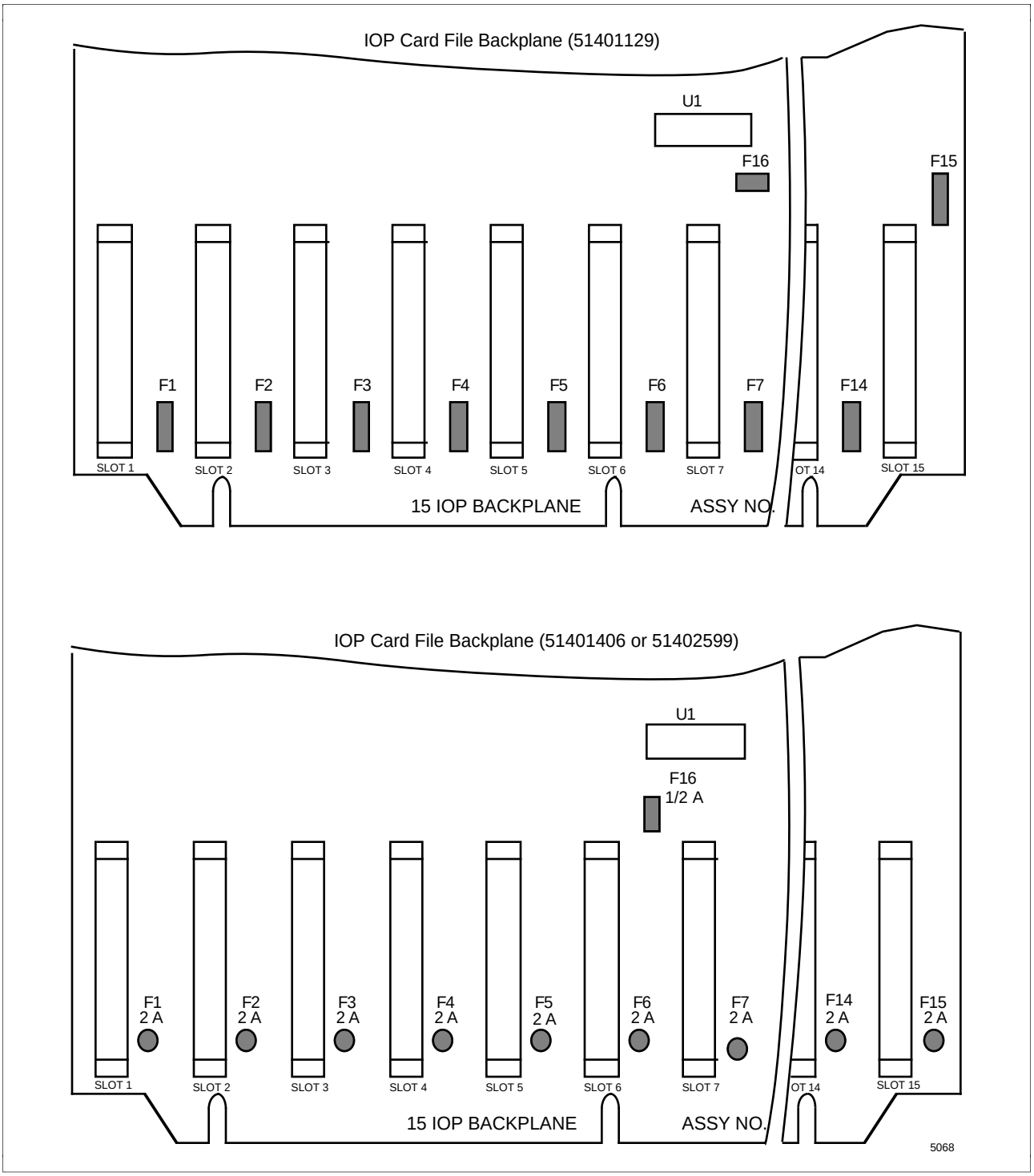


Continued on next page

IOP Only card file backplane fuse locations

Figure 2-44 illustrates the locations of the individual fuses on the IOP Only card file backplane.

Figure 2-44 IOP Only Card File Backplane Fuse Locations



Continued on next page

2.10.7 24 Vdc Fuse Protection, Continued

FTA fuse protection

Some individual FTAs may have fuse protection on the assembly. In general, output type FTAs are fused, but not exclusively. Fuse information for the individual FTAs can be found in the *Process Manager I/O Installation* manual.

Cabinet Fan assembly fuse protection

Each cabinet Fan Assembly is protected by fast-action 0.5 A fuse located on the Power System backplane assembly. A High-Performance Process Manager cabinet can contain two individually fused Fan Assemblies. Both the early production Standard, HPM Standard, and AC Only Power System configurations provide fused circuits for four Fan assemblies. Refer to Figure 2-25, 2-26 or 2-27 for the locations of the Fan Assembly fuses.

2.10.8 5 Vdc Fuse Protection

HPMM power routing and fuses

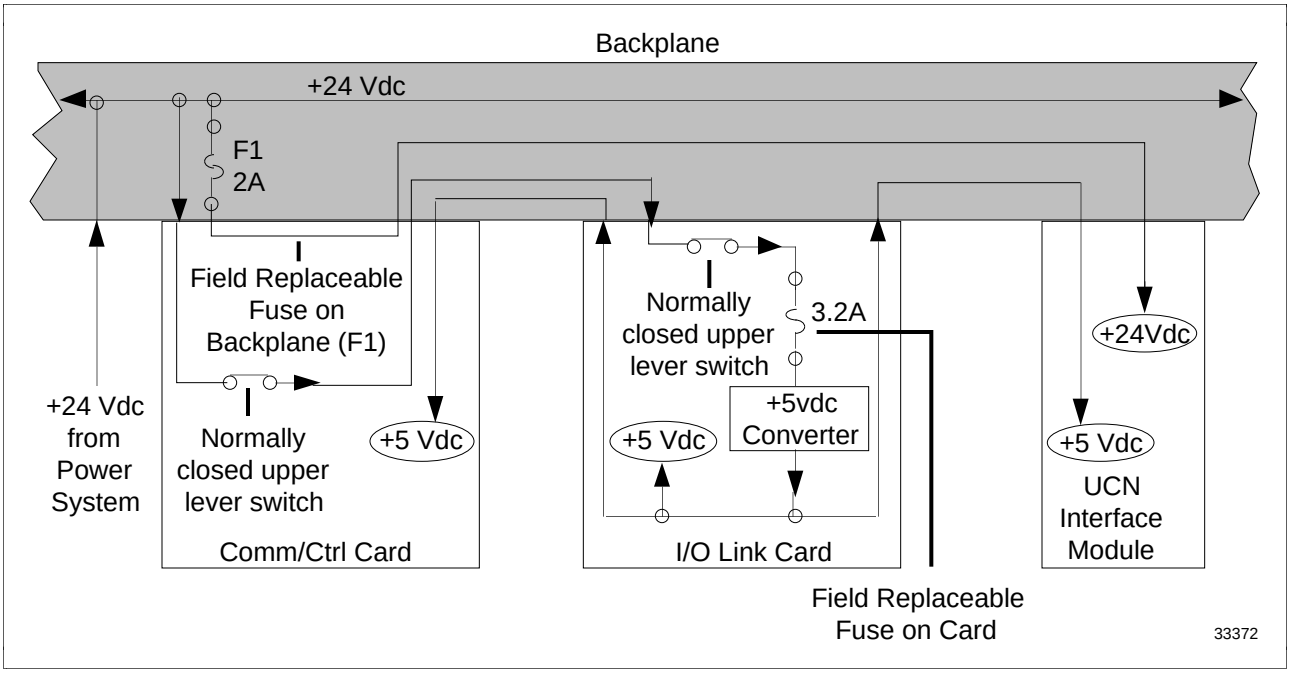
The High-Performance I/O Link card provides the 5 Vdc operating power for the High-Performance Comm/Control and the HPM UCN Interface module by converting the unfused 24 Vdc from the backplane. The 5 Vdc power is protected at the input to the converter by a 3.2 A surface-mounted fuse on the High-Performance I/O Link card. The 5 Vdc converter output is used by the High-Performance I/O Link card itself and is also routed to the High-Performance Comm/Control card and the UCN Interface Module through the backplane.

The HPMM components consist of the High-Performance Comm/Control card, High-Performance I/O Link card, and the HPM UCN Interface module. Figure 2-45 illustrates the power routing and fusing as it applies to the HPMM components.

Note the location of the of the two fuses involved

- 3.2 amp fuse on High-Performance I/O Link card (Located near the upper card lever)
- 2 amp fuse (F1) on the backplane (Located on the backplane, immediately to the right of the FTA cable connector for the leftmost slot in the card file.)

Figure 2-45 HPMM Power Routing and Fuses



2.10.9 Card File Power Cabling

Card file power connectors

Each card file receives power (24 Vdc, 3.6 Vdc, and 6 Vac) from the Power System through dual cables that connect to the Power System which are listed in Table 2-9.

Table 2-9 Card File Power Cabling

Card File Type	Dual Power Connectors
7-Slot	J20 and J21
15-Slot	J46 and J47
IOP Only	J33 and J37

Power Distribution assemblies

Digital Input Power Distribution assemblies and Galvanic Isolation Power Distribution assemblies require 24 Vdc power and require the same type of power cable as the card files.

Power System power connectors

The early production Standard Power System and the AC Only Power System have eight power connectors, labeled **Output 1** through **Output 8**. Connectors are not "assigned" to any particular card file or Power Distribution assembly. The connectors are located at the upper right side of the backplane of the Standard Power System as shown in Figure 2-25. The AC Only Power System power connectors are located at the right side of its AC/DC Distribution assembly as shown in Figure 2-27.

The HPM Standard Power System has 12 power output connectors as shown in Figure 2-26.

Power distribution examples

Figures 2-42 through 2-45 illustrate typical power cabling of various combinations of card files and Power Distribution assemblies using the Standard Power System. The AC Only Power System cabling would be similar.

Continued on next page

2.10.9 Card File Power Cabling, Continued

Power distribution methods

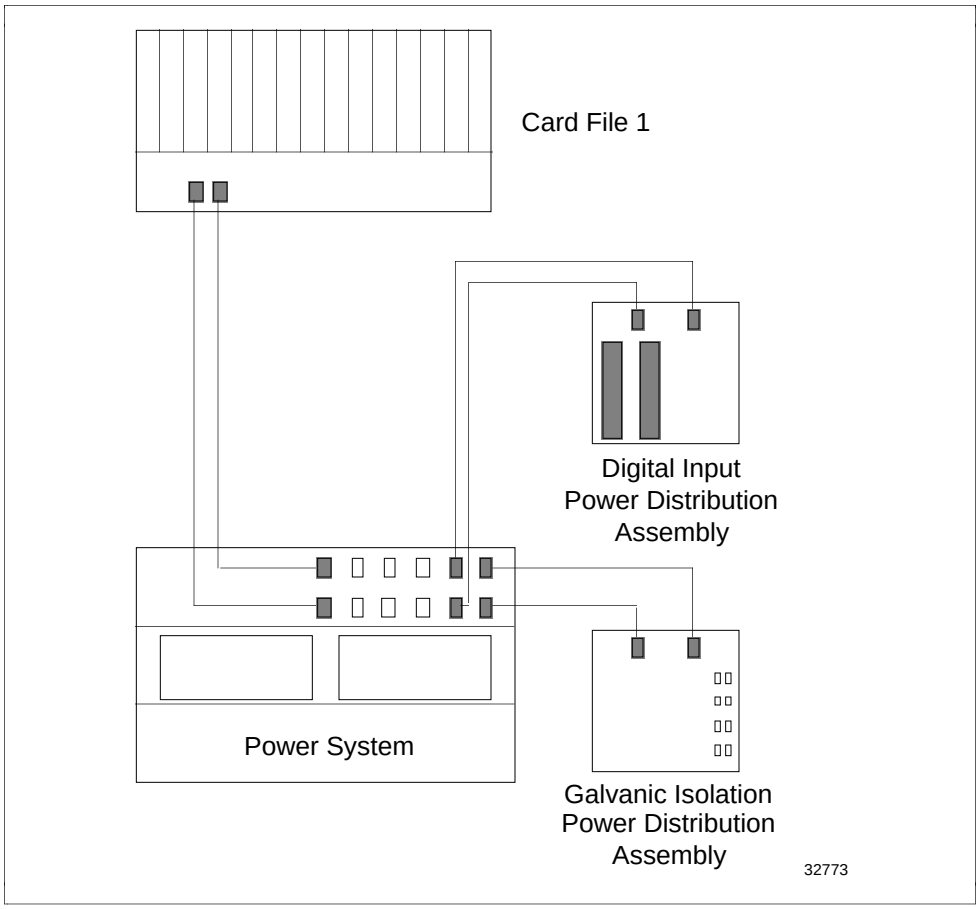
The early production Standard Power System and the AC Only power system are limited to eight power output connectors. The eight connectors provide power for various combinations, depending upon power requirements of card files, Digital Input Power Distribution assemblies, and Galvanic Isolation Power Distribution assemblies. Redundant power cabling to each assembly is recommended. However, an exception must be made when three card files, a Digital Input Power Distribution assembly, and a Galvanic Isolation Power Distribution assembly are present in the cabinet, since only eight power output connectors are available. The power cables are then daisy-chained. See Figure 2-50

The HPM Standard Power System provides 12 power output connectors which eliminates the need to daisy-chain power from one file to file.

Power cabling illustration

Figure 2-46 is an illustration of power cabling for a typical High-Performance Process Manager configuration of a single 15-Slot card file and Power Distribution assemblies.

Figure 2-46 Typical Standard Power System Power Cabling – 15-Slot Card File with Power Distribution Assemblies



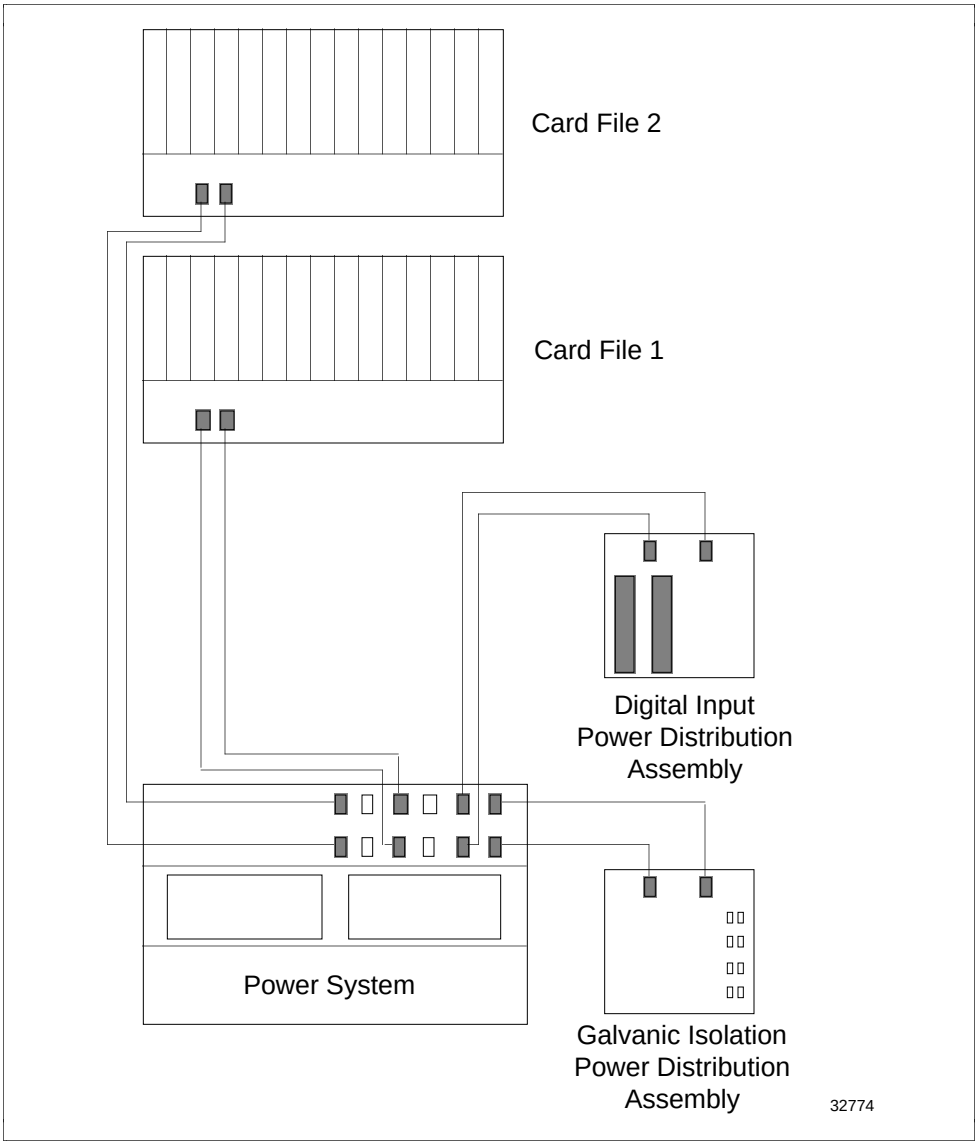
Continued on next page

2.10.9 Card File Power Cabling, Continued

Power cabling illustration, continued

Figure 2-47 is an illustration of power cabling for a typical High-Performance Process Manager configuration of two 15-Slot card files and two Power Distribution assemblies.

Figure 2-47 Typical Standard Power System Power Cabling – Two 15-Slot Card Files with Power Distribution Assemblies



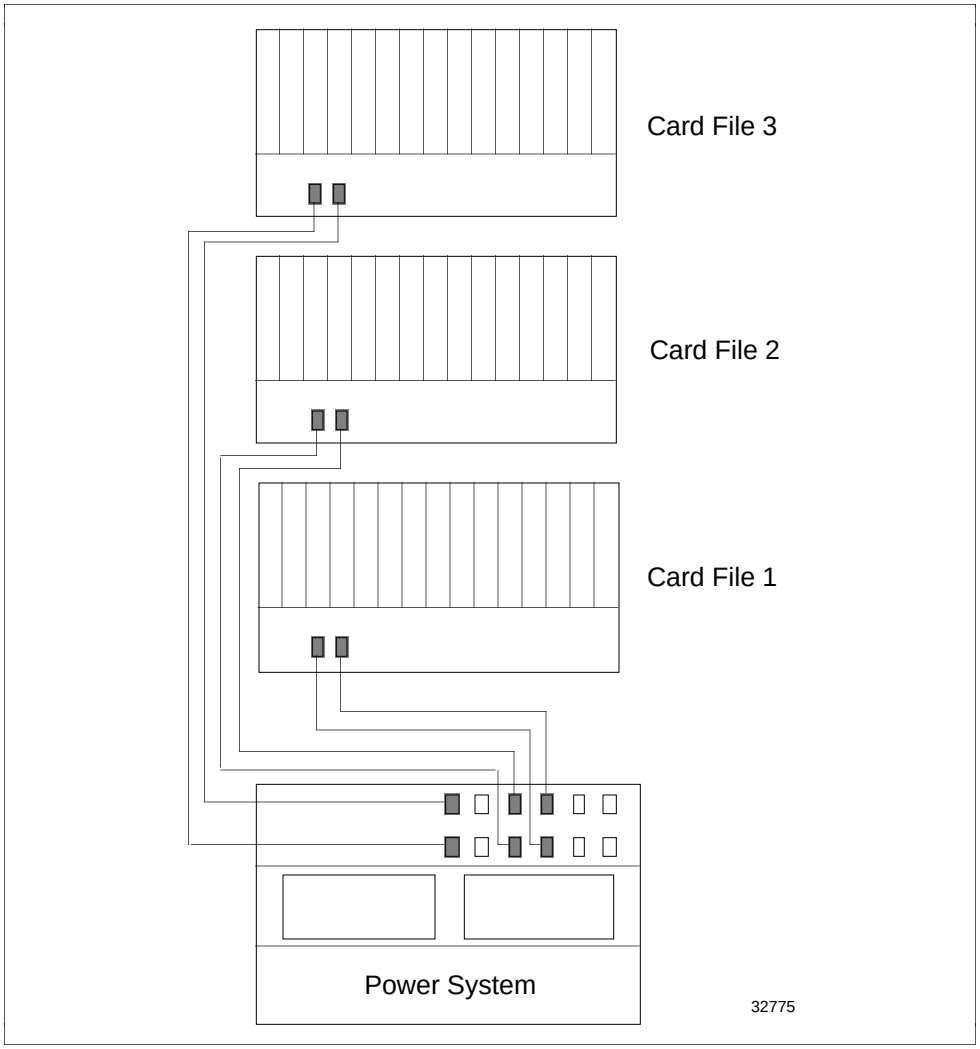
Continued on next page

2.10.9 Card File Power Cabling, Continued

Power cabling illustration, continued

Figure 2-48 is an illustration of power cabling for a typical High-Performance Process Manager configuration of three 15-Slot card files.

Figure 2-48 Typical Standard Power System Power Cabling – Three 15-Slot Card Files



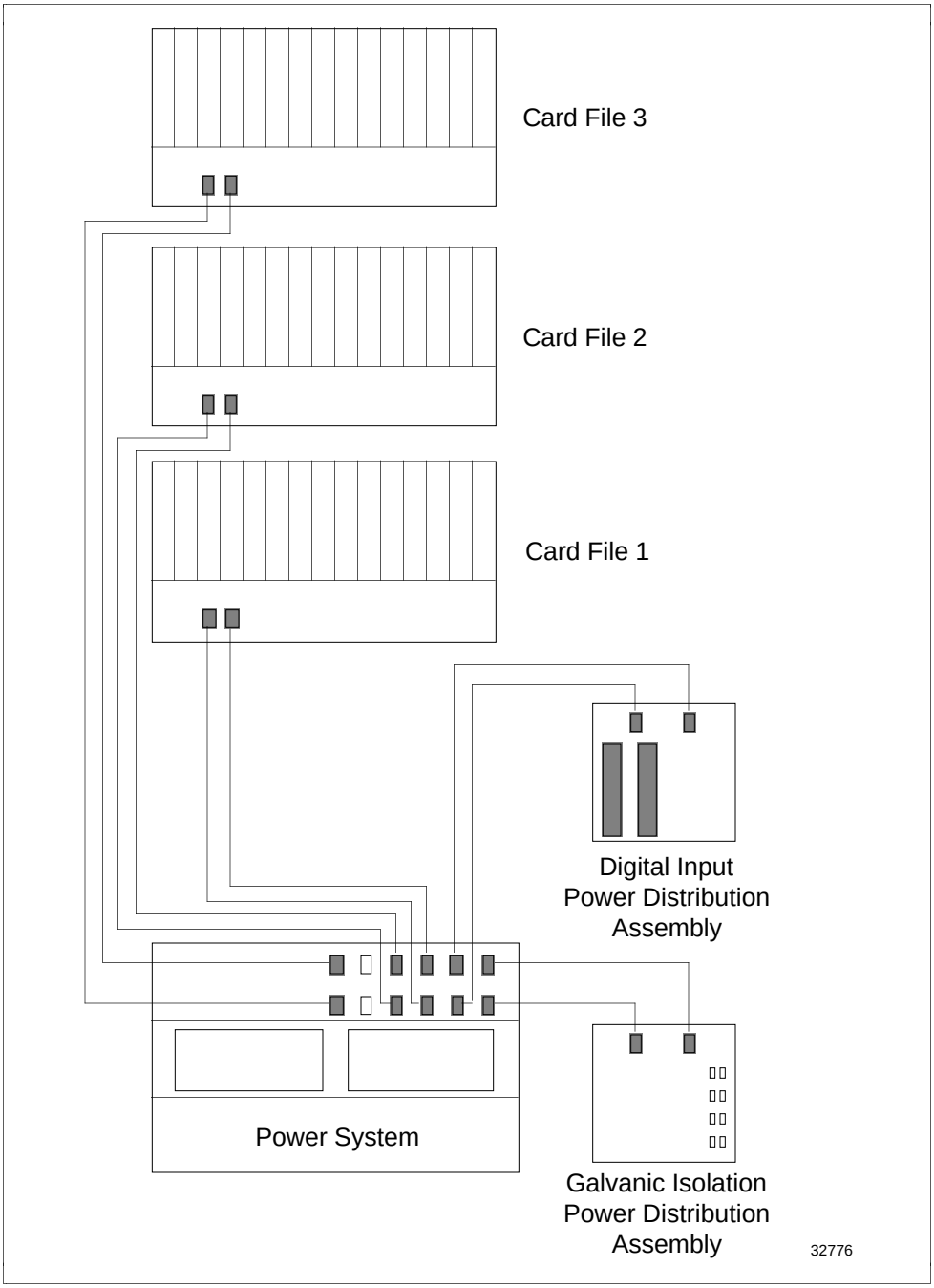
Continued on next page

2.10.9 Card File Power Cabling, Continued

Power cabling illustration, continued

Figure 2-49 is an illustration of power cabling for a typical High-Performance Process Manager configuration of three 15-Slot card files and two Power Distribution assemblies.

Figure 2-49 Typical Standard Power System Power Cabling – Three 15-Slot Card Files with Power Distribution Assemblies

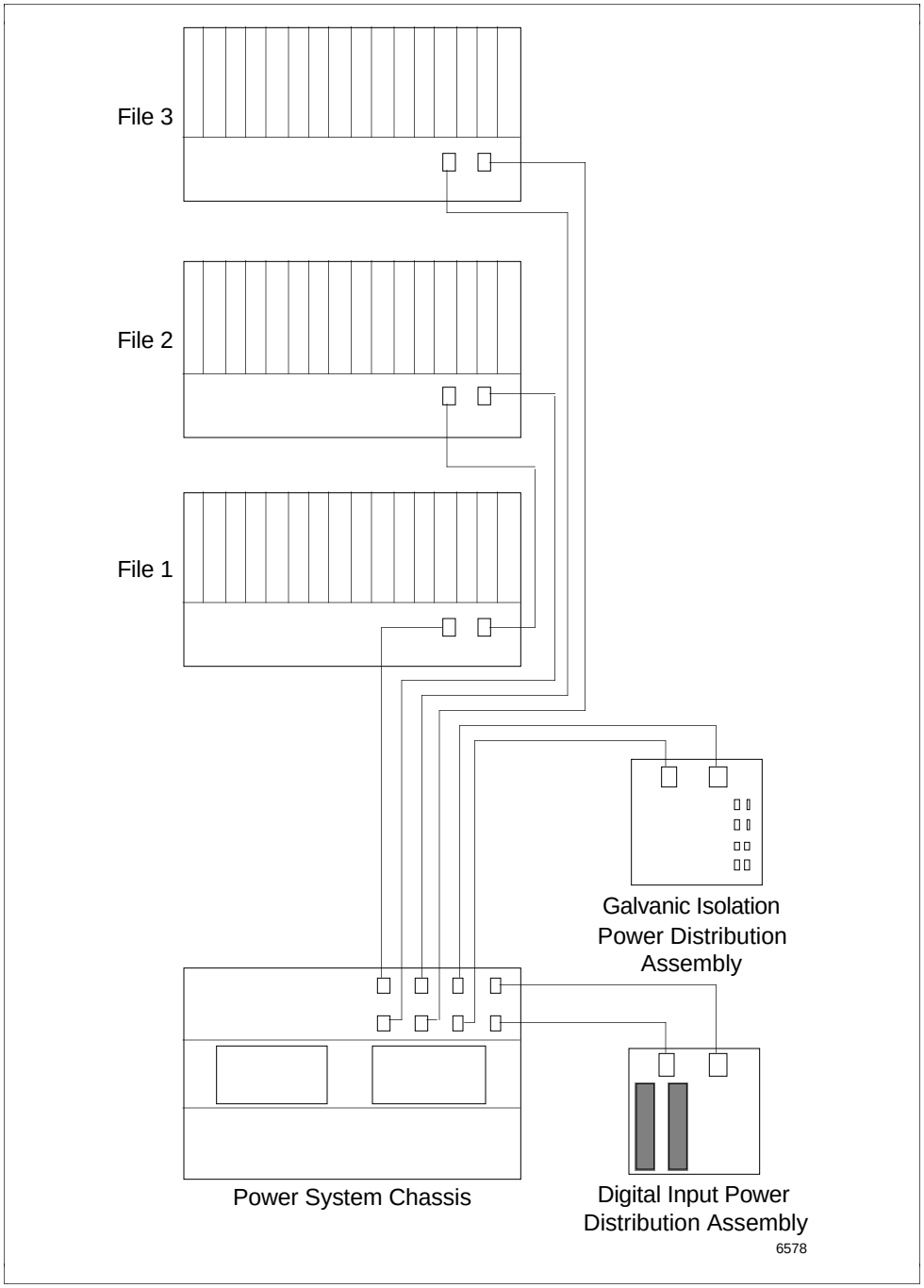


Continued on next page

Power cabling illustration, continued

Early production Standard Power Systems and AC Only Power Systems are limited to eight power output connectors. Figure 2-50 illustrates how power is distributed when the number of available connectors does not meet the total need for redundant cabling.

Figure 2-50 Typical Early Production Power System Cabling – Three 15-Slot Card Files with Power Distribution Assemblies



2.11 I/O Link Interface Cabling

Introduction

The I/O Link Interface is a dual serial communications link between the HPMM(s) and IOP card files. If there are more than two card files, the cables are daisy-chained. Figures 2-51 and 2-52 illustrate a typical I/O Link Interface cable installations. Table 2-10 identifies the I/O Link Interface connectors on the 7-Slot, 15-Slot, and IOP Only card file backplanes.

Table 2-10 I/O Link Interface Cabling Card File Connector Assignments

Card File Type	I/O Link A Connector	I/O Link B Connector
7-Slot	J23	J24
15-Slot	J42	J43
IOP Only	J32	J31

Cable length

I/O Link Interface cables are to be no longer than 10 m (33 feet) in total length and are not to leave the cabinet or cabinet complex.

Redundant cables

Two cables are required because the I/O Link Interface is redundant for reliability. One cable is designated Link A and the other Link B.

No cable termination

The I/O Link Interface cabling does not involve external terminators and therefore an empty I/O Link Interface connector on the backplane is an acceptable situation.

CAUTION

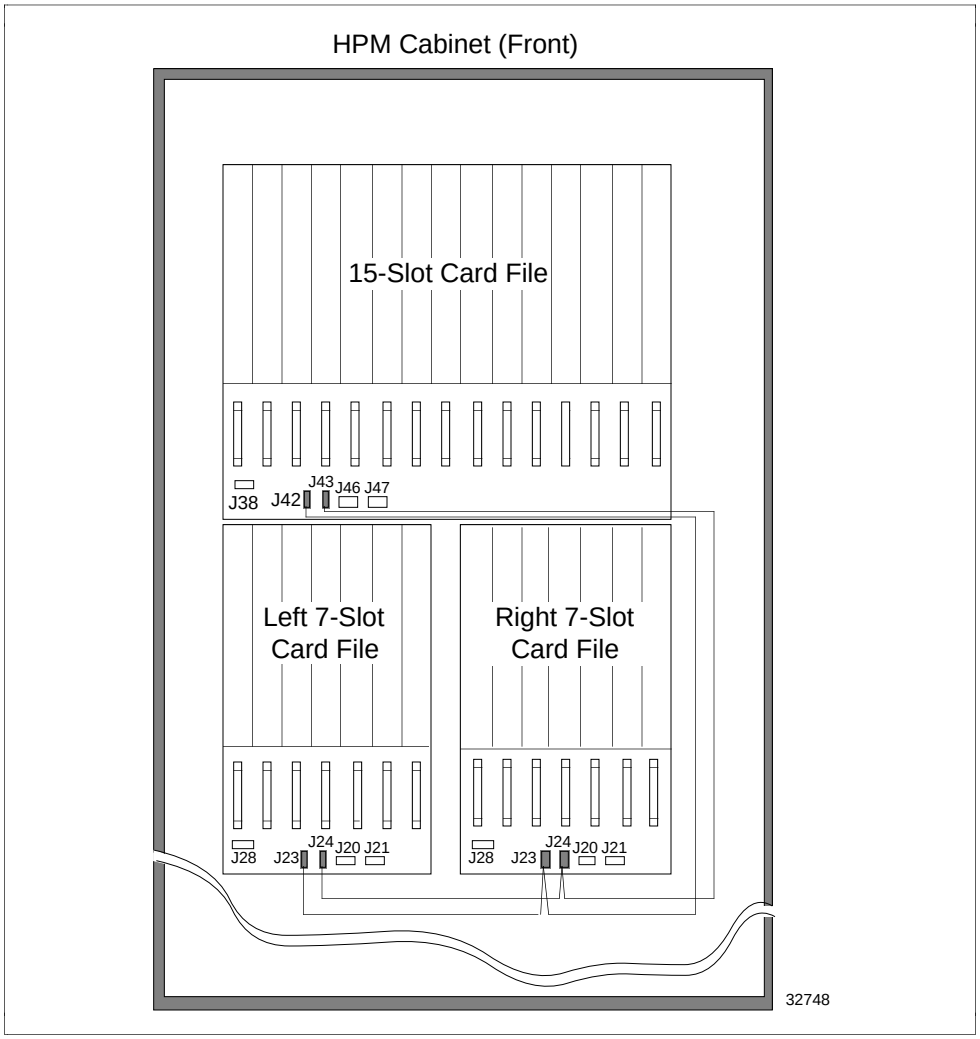
CAUTION—The High-Performance Process Manager accommodates four types of card files. Use caution when connecting the I/O Link Interface cables because of the differences between the card files. All card files have two I/O Link Interface receptacles marked **LINKA** and **LINKB**.

Continued on next page

I/O Link Interface cabling illustration

Figure 2-51 is an illustration of the I/O Link Interface cabling for an High-Performance Process Manager configuration that consists of two 7-Slot HPMM card files and one 15-Slot IOP card file.

Figure 2-51 I/O Link Interface Cabling – Three Card Files

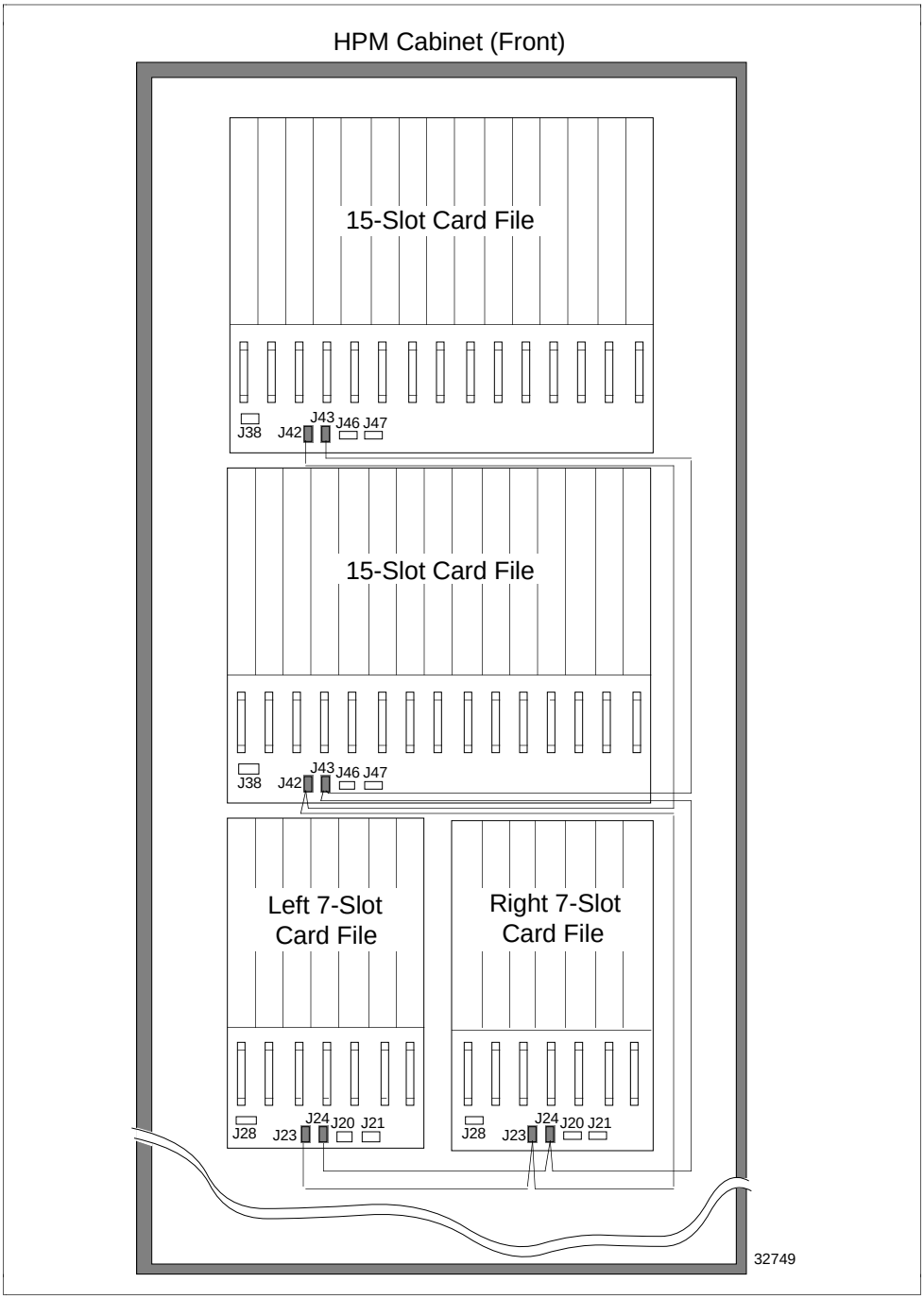


Continued on next page

I/O Link Interface cabling illustration, continued

Figure 2-52 is an illustration of the I/O Link Interface cabling for an High-Performance Process Manager configuration that consists of two 7-Slot HPMM card files and two 15-Slot IOP card files.

Figure 2-52 I/O Link Interface Cabling – Four Card Files



Continued on next page

I/O Link Interface Cables in adjacent cabinets

The I/O Link Interface cable daisy chain can be extended to include additional intermediate drops. Longer daisy chain runs from card file to card file in one cabinet can continue to include the card files in an adjacent cabinet. I/O Link Interface cables with the appropriate number of drops must be ordered to satisfy your HPM subsystem configuration (number of card files).

I/O Link Interface cable shield grounding (non-CE Compliance)

Only one point along the I/O Link Interface cable daisy chain should provide ground to the cable chain shield. This is normally done on the backplane of the first HPMM card file (file position 1) in the first HPM cabinet (with jumpers on the backplane).

On a 7-Slot card file, J29 and J22 are located between the I/O Link Interface cable connectors. Both the A and B I/O Link Interface cables have their own jumper for grounding the cable shield. J29 is for the A cable shield and J22 is for the B cable shield. The cable shield is grounded if the jumper is bridged across both pins.

On the 15-Slot card file, J44 and J45 are located between the I/O Link Interface cable connectors and accomplish the same function.

The above I/O Link Interface cable shield grounding must be carefully adhered to when installing or upgrading a High-Performance Process Manager subsystem. Failure to follow the above guidelines can result in unwanted ground loops and abnormal system sensitivity to RFI and ESD influence from the surrounding environment.

I/O Link Interface cable shield grounding (CE Compliance)

CE Compliance requires that the I/O Link Interface cable shield be grounded to the card file chassis (Safety Ground) at each connector. This is accomplished with shield wire that attaches to a FASTON terminal on the card file backplane ground plate. Only cables with a part number of 51204042-xxx can be used. See the *High-Performance Process Manager Installation* manual for additional information.

2.12 IOP to FTA Cabling

Introduction

Each IOP has a cable that connects it to its associated FTA.

Standard FTAs

The cables for standard FTAs leave the FTAs at the top or center, travel up or down the right side of the Vertical FTA Mounting Channel, go over or under the center divider, and then connect to the associated IOP connector on the 7-Slot or 15-Slot card file backplane.

Galvanically Isolated FTAs

The cables for the Galvanically Isolated FTAs leave the top side of the FTAs, travel up or down the left side of the Horizontal FTA Mounting Channel, go over or under the center divider, and then connect to the associated IOP connector on the 7-Slot or 15-Slot card file backplane.

External cabinet installation

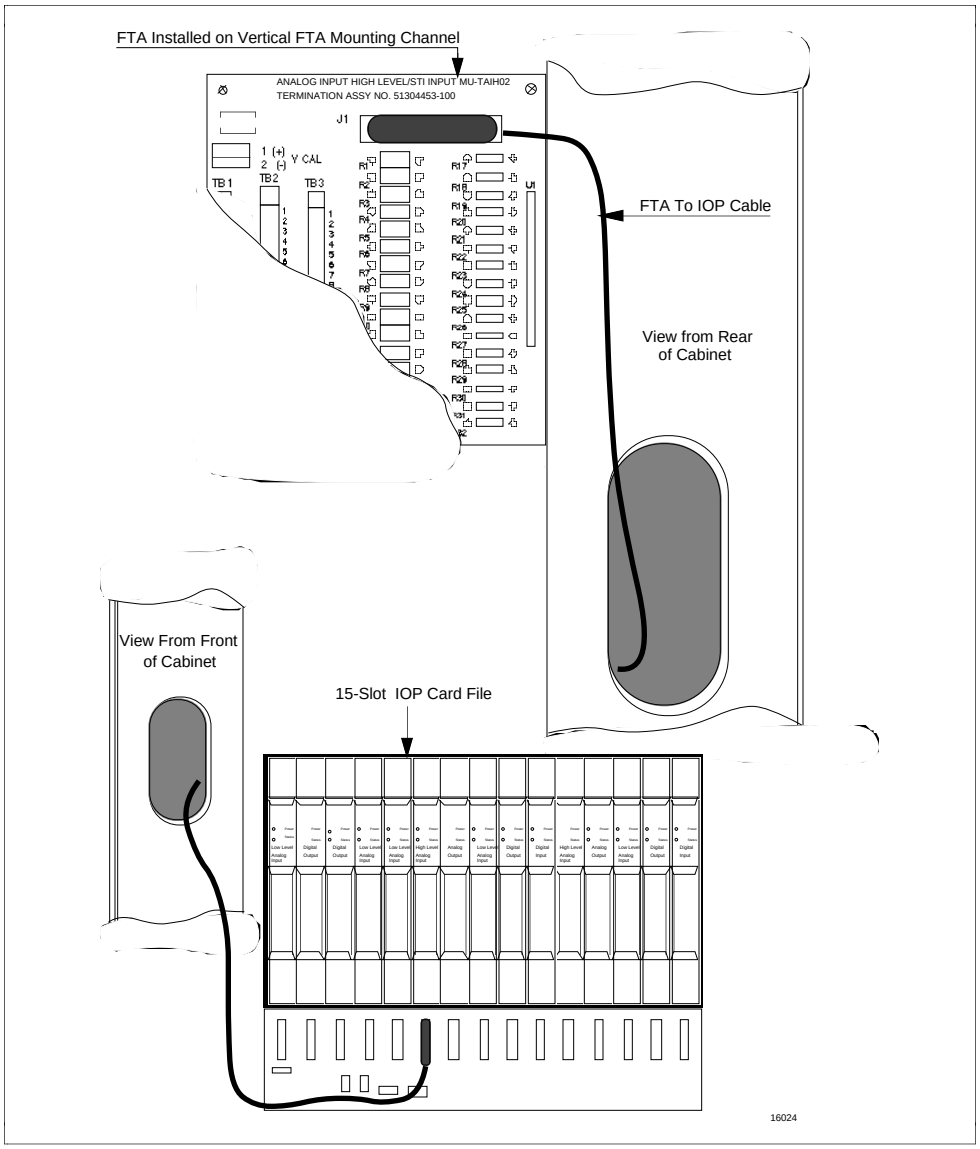
The FTAs can also be installed on a panel that is external to the cabinet, up to 50 meters (164 feet) cable length from the IOP. Shielded FTA cables must be used whenever the FTA is located outside of the HPMM cabinet complex. See the *High-Performance Process Manager Installation* manual for additional information.

Continued on next page

Typical cable routing

Figure 2-53 for an illustration of typical cable routing for a standard FTA in a cabinet or cabinet complex.

Figure 2-53 IOP to FTA Cabinet Cabling



2.13 Power Adapter Cabling

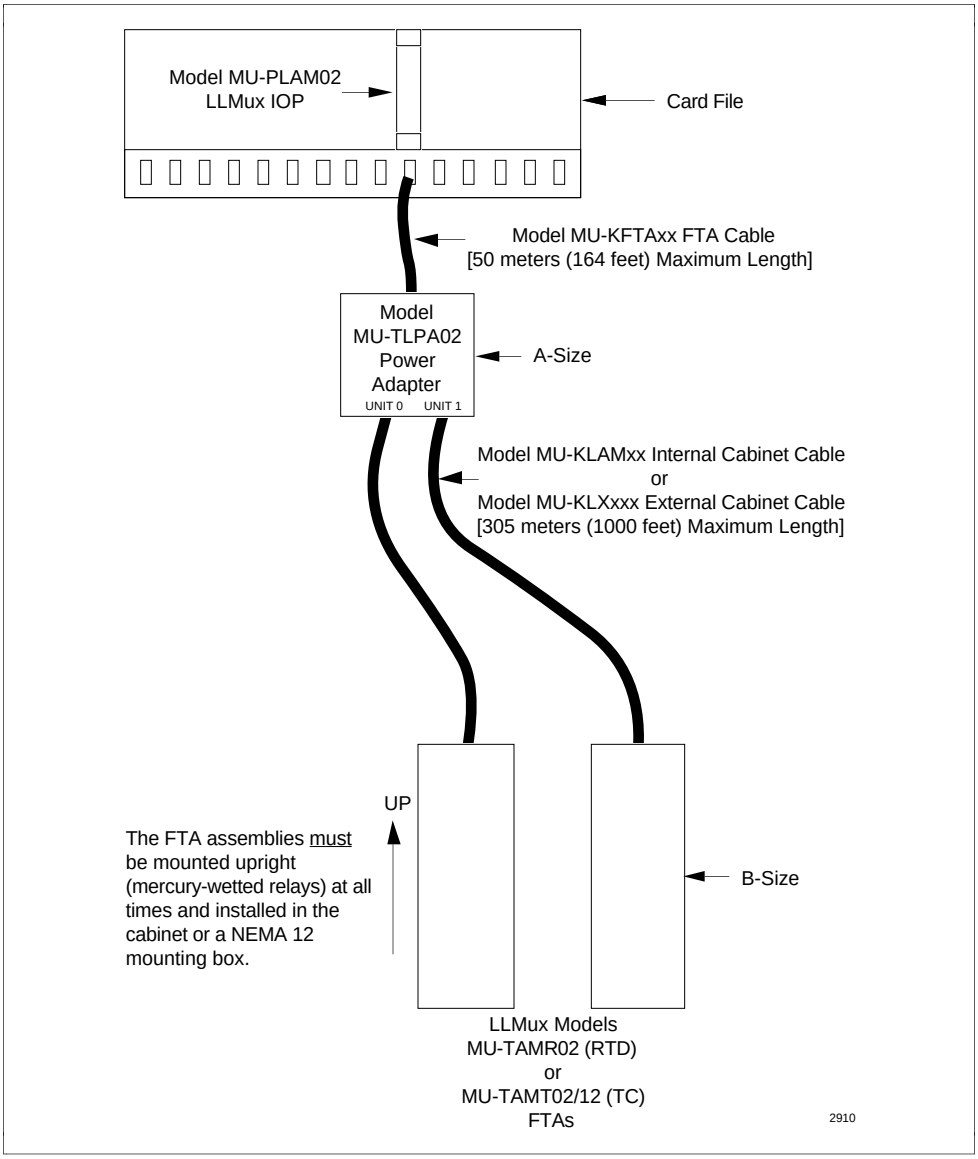
Introduction

Using a standard FTA cable, the model MU-TLPA02 Power Adapter can be located up to 50 meters (164 feet) distance from the card file containing the associated IOP card. The Power Adapter connects to one or two FTAs that can be installed at a remote location up to 305 meters (1000 feet) from the Power Adapter. Figures 2-54 through 2-56 illustrate its application with the Low Level Multiplexer, Serial Device Interface, and Serial Interface IOPs, respectively.

LLMux interconnections

Figure 2-54 illustrates the Power Adapter interconnections for a Low Level Multiplexer application.

Figure 2-54 Power Adapter Interconnections – LLMux Application

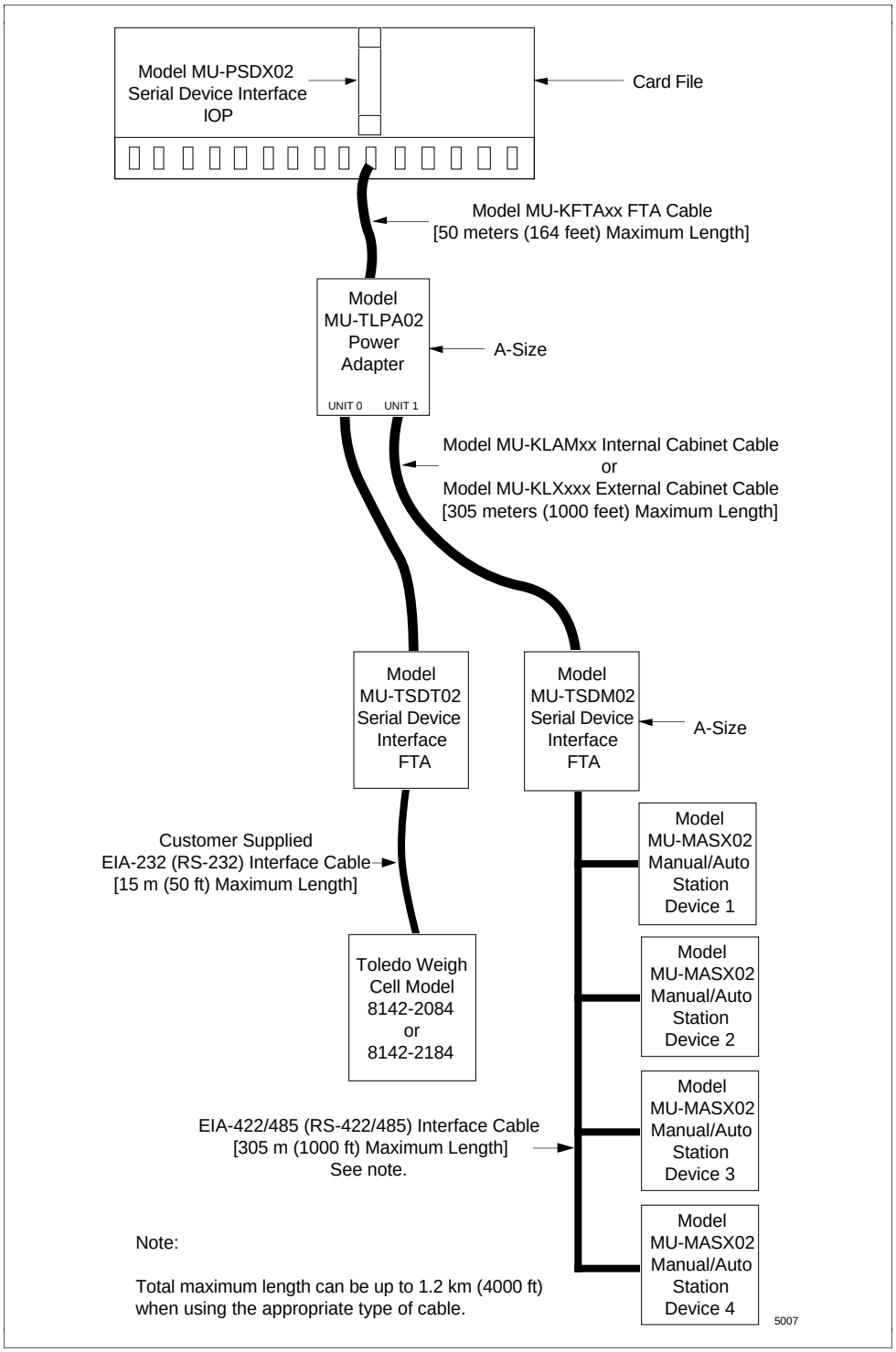


Continued on next page

SDI interconnections

Figure 2-55 illustrates the Power Adapter interconnections for a Serial Device Interface application.

Figure 2-55 Power Adapter Interconnections – SDI Application

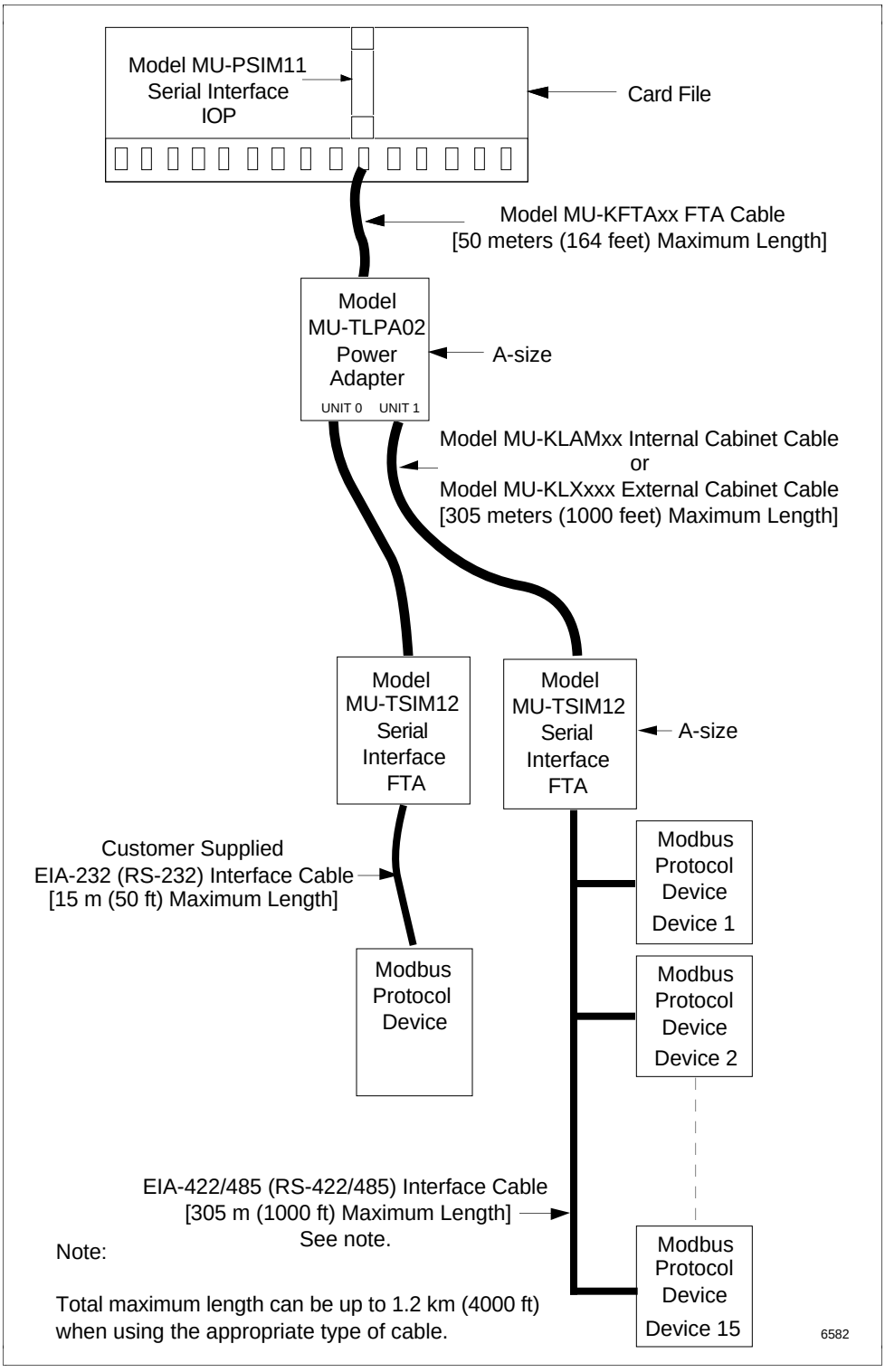


Continued on next page

SI interconnections

Figure 2-56 illustrates the Power Adapter interconnections for a Serial Interface application.

Figure 2-56 Power Adapter Interconnections – SI Application

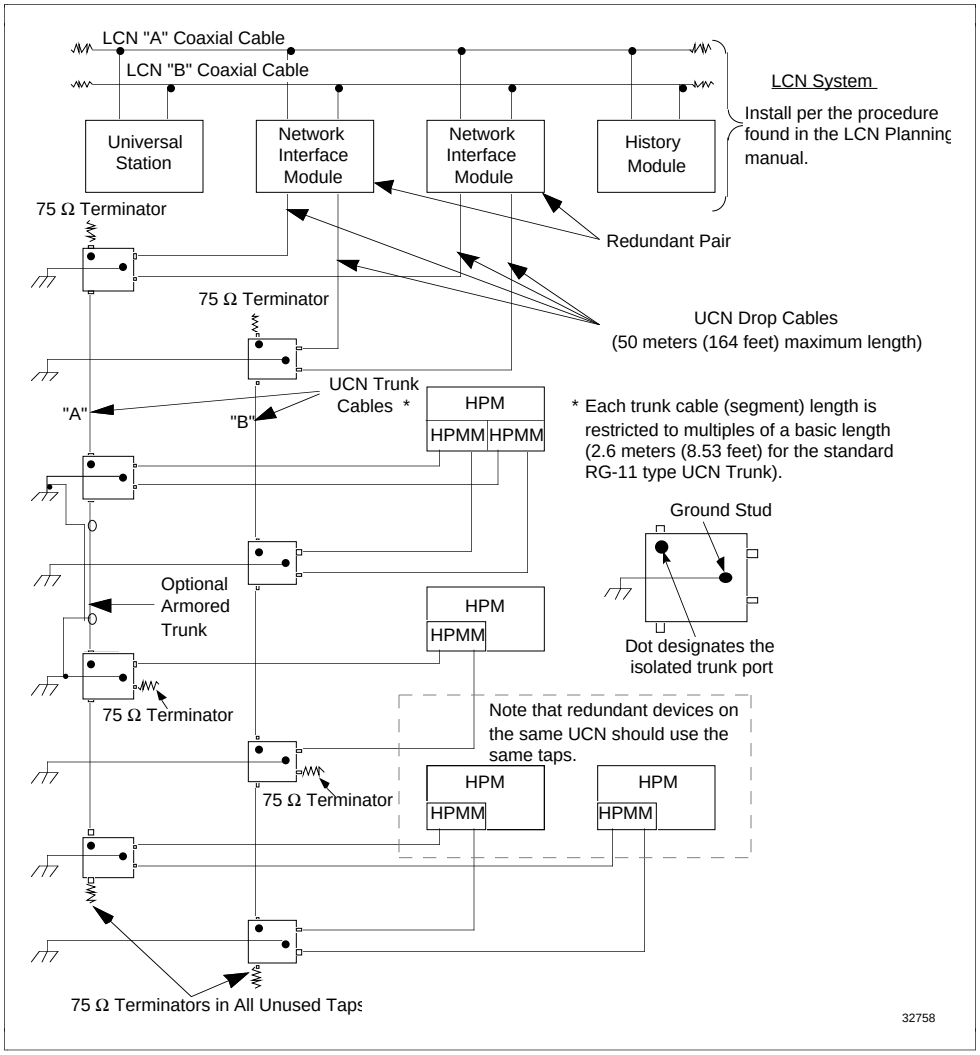


2.14 UCN Cable System

Introduction

The Universal Control Network (UCN) provides communication between High-Performance Process Manager Modules (HPMMs) and the Network Interface Module (NIM) on the LCN as illustrated in Figure 2-57. Use of the two-drop UCN cable tap is illustrated.

Figure 2-57 Universal Control Network (UCN) Components



Redundant UCN cables

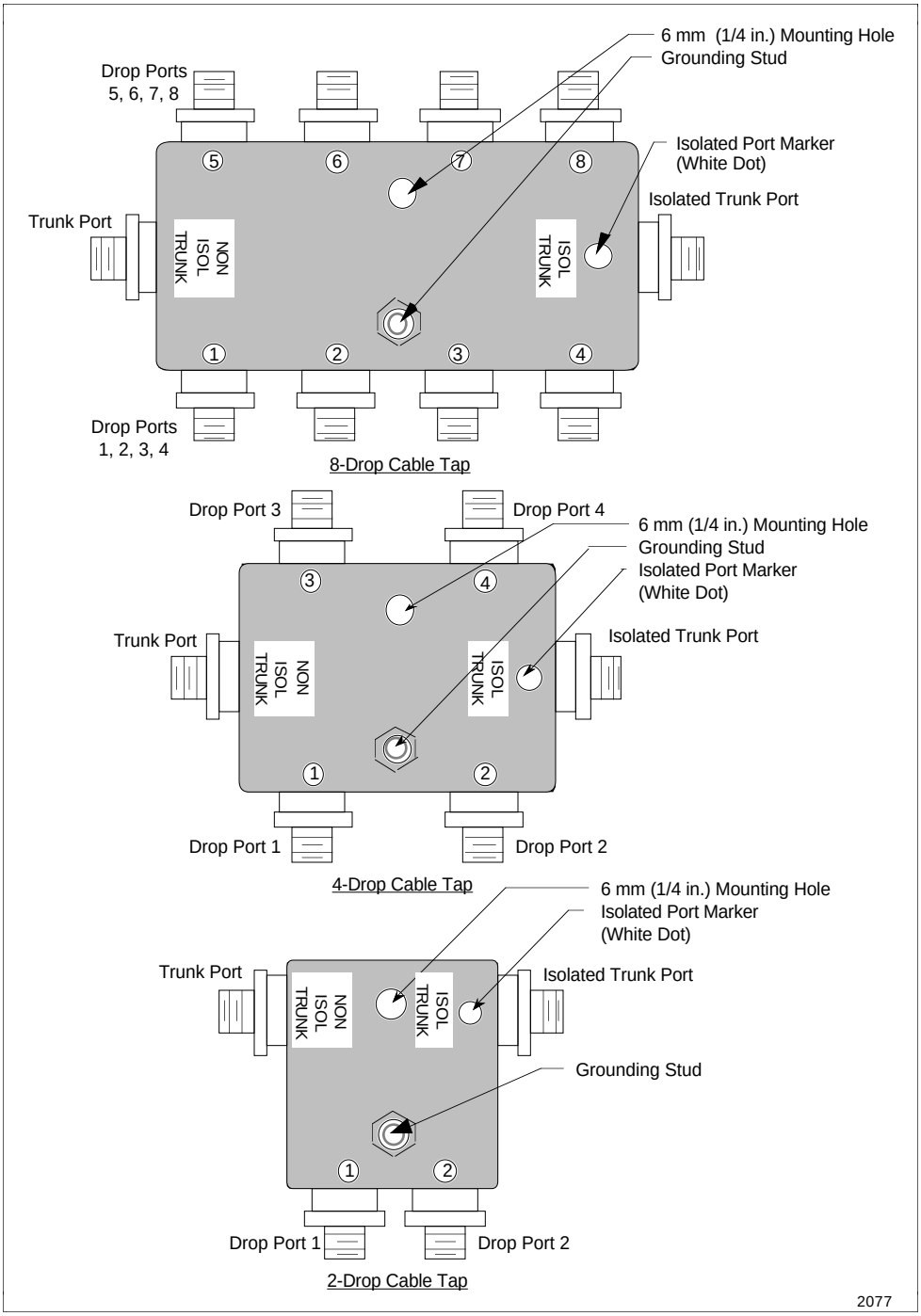
Communication is accomplished on a redundant cable system consisting of Cable A and Cable B. Trunk cables are interconnected by taps that allow connection of drop cables from both Cable A and Cable B. Redundant HPMMs should have their A cables connected to the same A tap, and their B cables connected to the same B tap.

Continued on next page

Cable tap types

The cable taps used on the UCN are available in 2-drop, 4-drop, and 8-drop models as illustrated in Figure 2-58.

Figure 2-58 UCN Taps



Continued on next page

Cable tap usage

Two-drop cable taps are used for connecting the UCN to a redundant or nonredundant High-Performance Process Manager at a location. Four-drop cable taps are used when there are two redundant High-Performance Process Managers (four HPMMs), or multiple nonredundant HPMs at a location. The eight-drop cable tap supports up to four redundant (eight HPMMs) or eight nonredundant High-Performance Process Managers at a location.

Isolated port identification

Each tap has an indicator dot located near the isolated port connector.

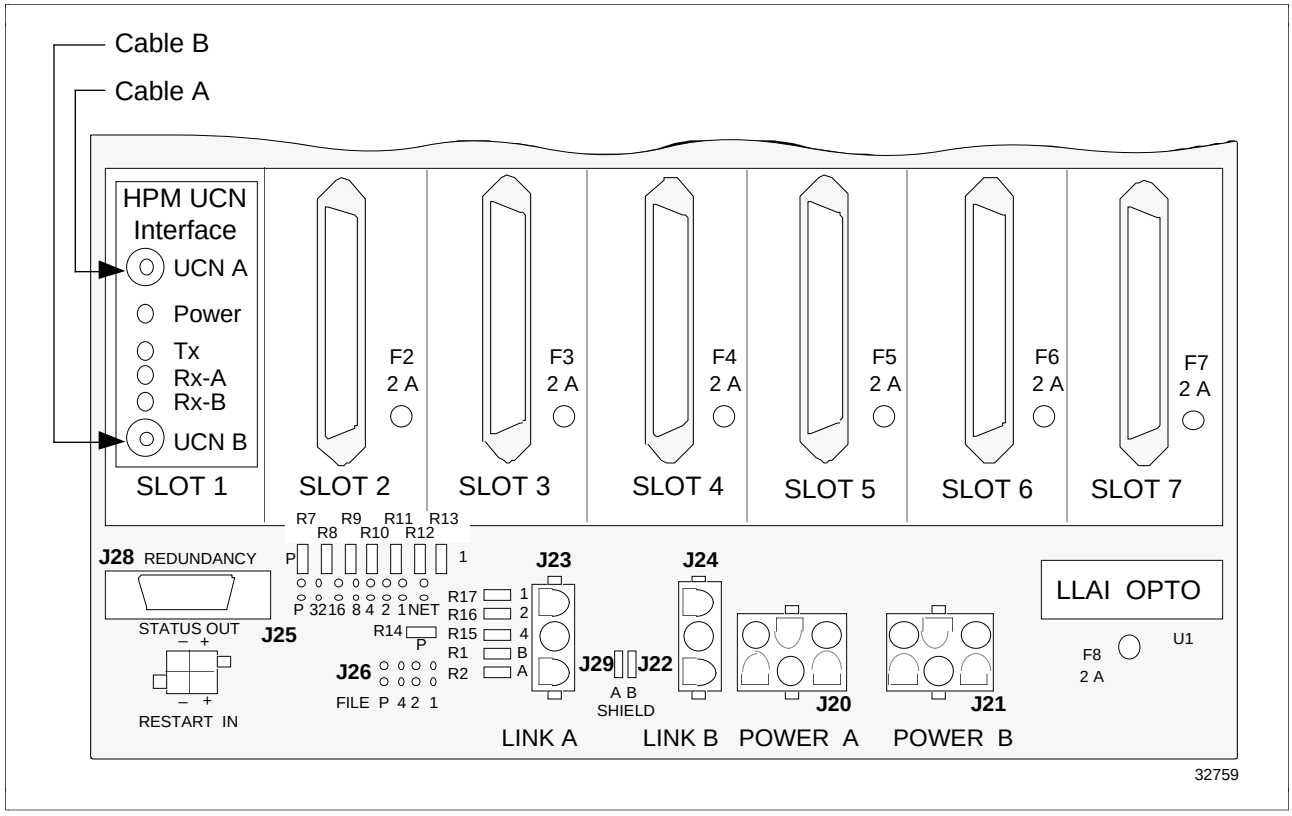
CAUTION

CAUTION—Cables between taps must be connected so that each cable segment connects the isolated port of one tap to the nonisolated port on the next tap.

Card file backplane connections

Figure 2-59 illustrates the A and B UCN drop cable connections to the HPM UCN Interface module in a 7-Slot HPMM card file.

Figure 2-59 UCN Drop Cable Connections to a 7-Slot HPMM Card File



2.15 UCN Node Address Pinning

Introduction

The UCN node address on the card file backplane is configured in the factory, but the node address can be changed or require verification in the field during installation.

One or two HPMM card files

A High-Performance Process Manager cabinet can have one or two (if redundant) card files that contain HPMMs, and possibly none or several card files that contain only IOPs. A card file that contains an HPMM must always be configured (pinned) for a UCN node address. The UCN node address pinning of a card file that contains only IOPs is ignored (not used).

Odd address pinning

The UCN node address for an HPMM is always configured as an odd number. The odd UCN node address is the address of the primary HPMM. The next consecutive address (even) is reserved for the secondary HPMM, whether physically present or not. For example, a UCN node address of 11 for the High-Performance Process Manager is odd, which is acceptable. A node address of 8 is even and is unacceptable for a primary HPMM.

Whether a card file contains the primary or secondary (redundant) High-Performance Process Manager Module (HPMM), it must always be configured (pinned) for the primary HPMM UCN node address, which is an odd number. Software takes care of the even node number for the backup HPMM.

Secondary HPMM determination

The system software logically determines the primary and secondary HPMM, either automatically or by System Console intervention.

Two methods of pinning

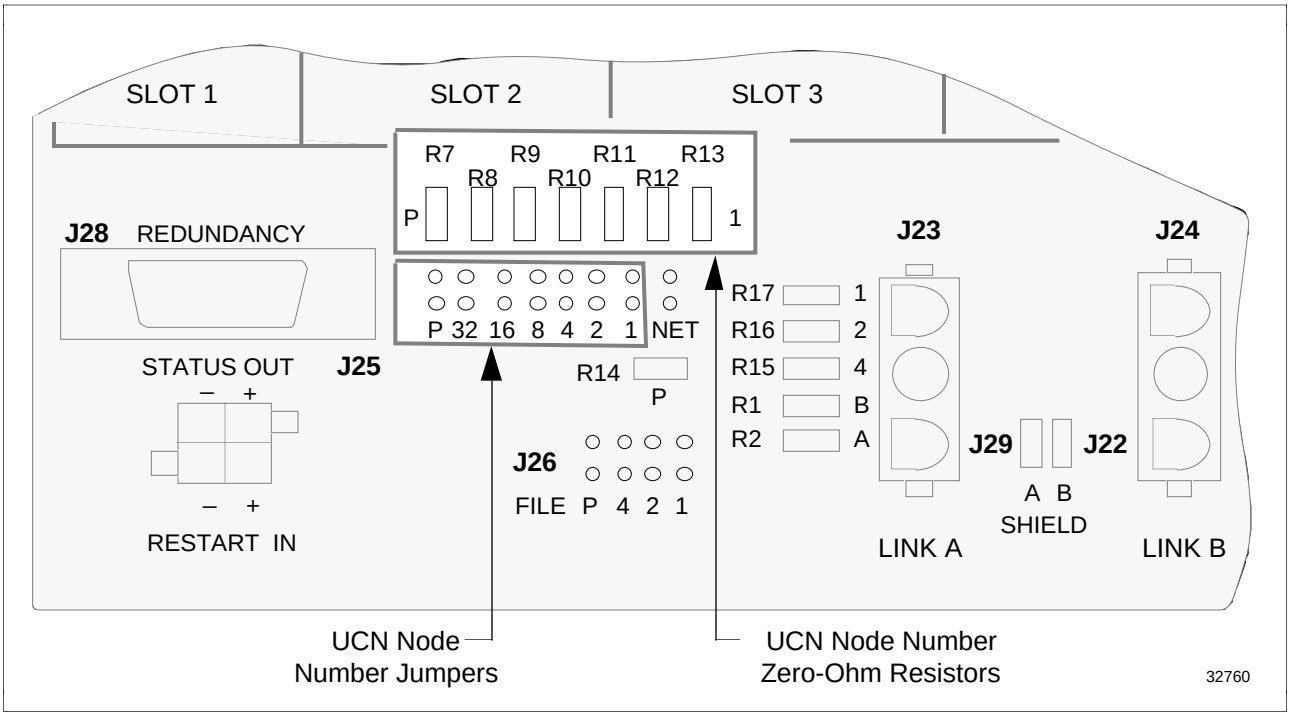
Two methods of UCN node address pinning are described later in this section. The HPM files normally use jumpers to define (pin) the UCN node address. Zero-ohm resistors (used in place of jumpers) are soldered in at the factory only by special request.

Continued on next page

7-Slot card file pinning

Figure 2-60 illustrates the location on a Left 7-Slot card file backplane where the odd UCN node address must be configured (pinned). The location on Right 7-Slot card file backplane is identical.

Figure 2-60 Left 7-Slot Card File UCN Node Address Pinning

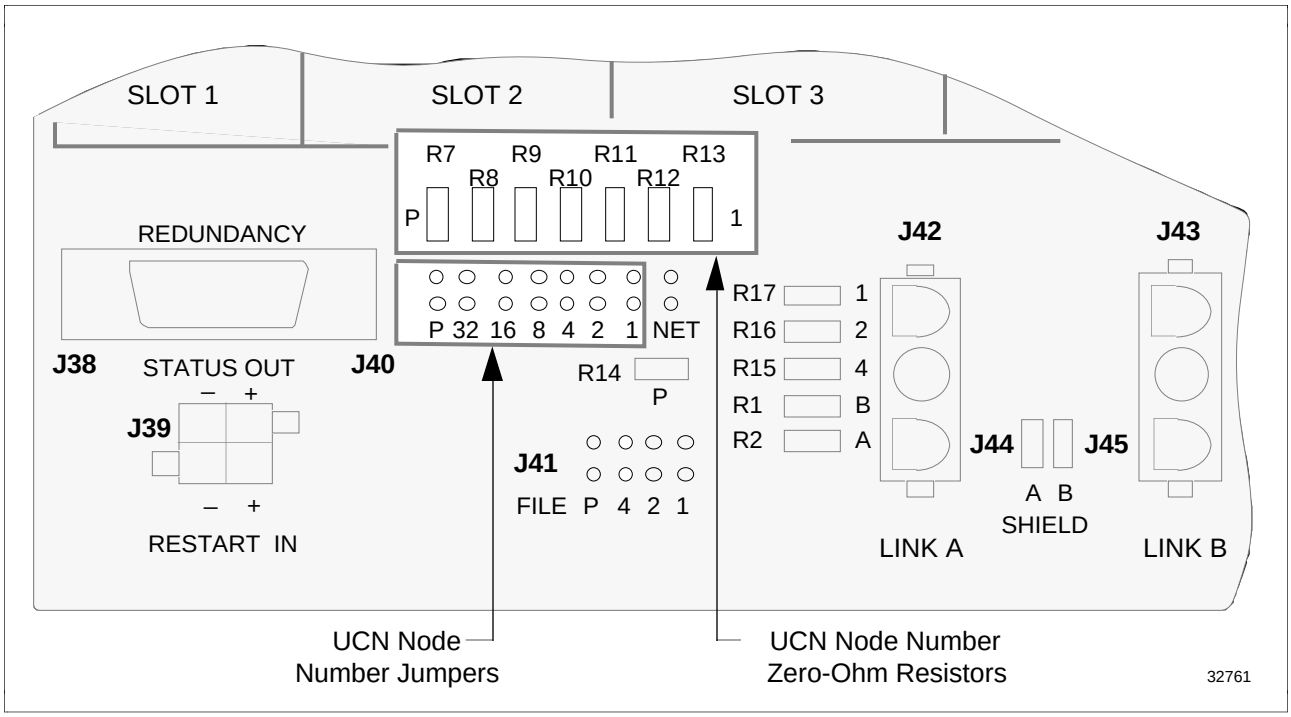


Continued on next page

15-Slot card file pinning

Figure 2-61 illustrates the location on a 15-Slot card file backplane where the odd UCN node address must be configured (pinned).

Figure 2-61 15-Slot Card File UCN Node Address Pinning



Two pinning methods

The High-Performance Process Manager has two means of configuring the UCN node address.

- Plug jumpers — Also known as "padlock" or "cowbell" jumpers
- Zero-ohm resistor jumpers — Basically, jumper wires that are soldered on the backplane printed wire board.

Currently the factory ships HPMs with plug jumpers unless the customer specifically requests zero-ohm resistor jumpers. Since both versions may exist in the field, both versions are covered in the following examples.

Pinning method differences

Plug jumpers are convenient to set up and change. Zero-ohm resistor jumpers are reliable and permanent. One method or the other must be disabled at initial installation before the system will function properly.

Odd number of jumpers required

For either address selection method, the hardware is designed so that an odd number of jumpers must be used. That is, regardless of the numerical value of the node address, the parity (P) plug/resistor jumper must be added or removed to provide an odd number of jumpers.

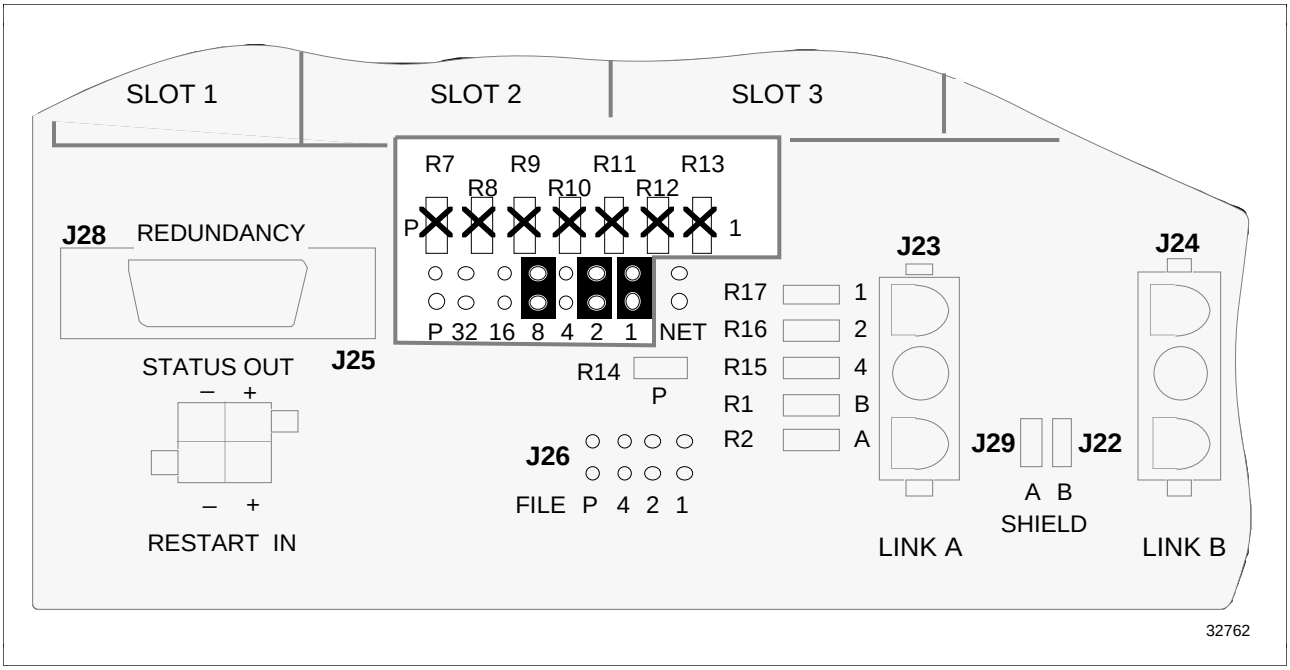
Continued on next page

2.15 UCN Node Address Pinning, Continued

Plug jumper method

To use the plug jumpers to configure the UCN node address, take diagonal cutters and remove all the zero-ohm resistor jumpers as illustrated in Figure 2-62 (if they exist). As an example, to configure a HPM for a UCN node address of 11, install jumpers at positions 1, 2, and 8 (1 + 2 + 8 = 11) by bridging the two circuit pins at each position. Because an odd number of jumpers is used, the P (parity) jumper must be removed along with those at positions 4, 16, and 32. The unused plug jumpers can be stored at their positions by hanging them on one pin.

Figure 2-62 UCN Node Address Pinning Using Plug Jumpers

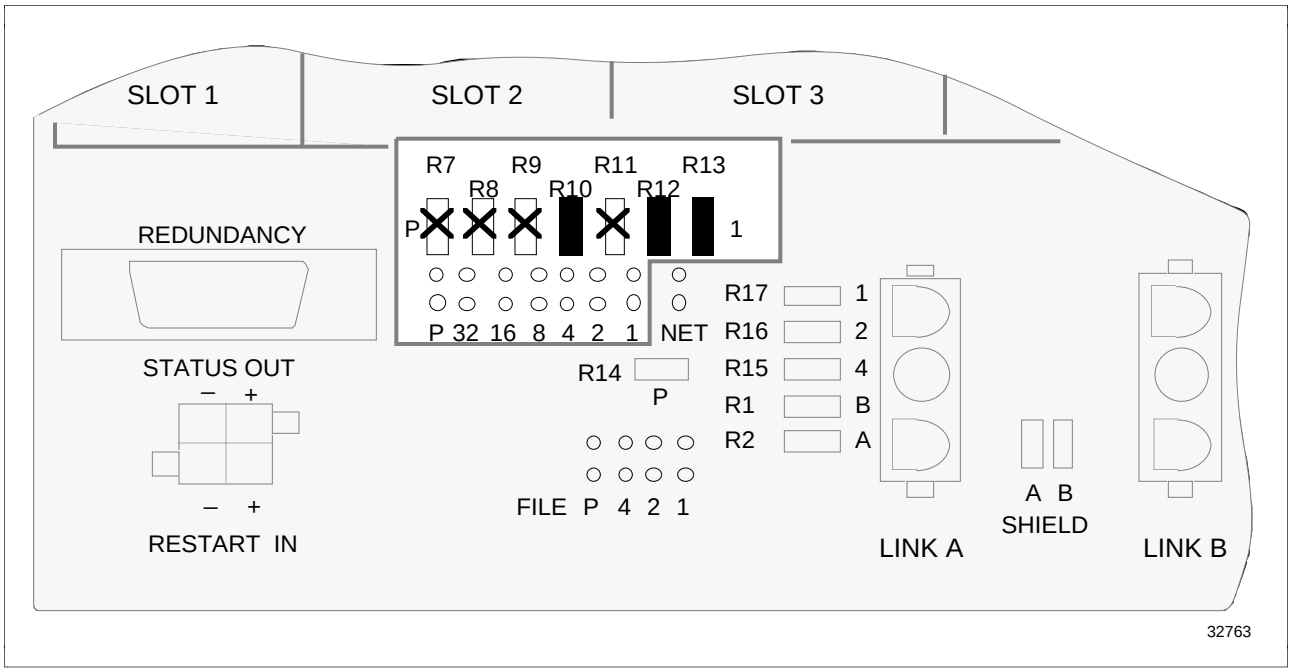


Continued on next page

Zero-ohm jumper method

To use zero-ohm resistors to configure the UCN node address, unplug, discard, or store all the plug jumpers as noted above. As an example in Figure 2-63, to configure a High-Performance Process Manager for a UCN node address of 11, do not remove the resistors at the 1, 2, and 8 (1 + 2 + 8 = 11) positions. Because an odd number of resistors is required, the P (parity) jumper must be removed along with those at positions 4, 16, and 32. Use a diagonal cutter to clip out the unwanted resistors.

Figure 2-63 UCN Node Address Pinning Using Zero-Ohm Resistors



CAUTION

CAUTION—If a mistake is made and a wrong jumper is removed, do not attempt to correct the problem by resoldering the jumper back into position. The backplane is easily damaged. Instead, remove all the zero-ohm jumpers and use the plug jumper method for UCN address configuration.

2.16 I/O Link Interface Address Pinning

Introduction

Input/Output Processor (IOP) cards can be installed in any of the four types of card files that are available for installation in a High-Performance Process Manager subsystem. The four types of card files are:

- Left 7-Slot card file
- Right 7-Slot card file
- 15-Slot card file (New design – accommodates an HPMM)
- IOP Only 15-Slot card file (exists in current PMs and APMs)

The IOP Only 15-Slot card file is a current PM/APM card file that can continue to be used when a PM or APM subsystem is upgraded to an HPM subsystem.

I/O Link Interface configuration

All card files must be hardware configured (pinned) for an address on the I/O Link Interface. I/O Link Interface address selection is implemented (pinned) with jumpers (or zero-ohm resistors) on each card file backplane.

Consecutive address assignment

The card file I/O Link Interface addresses must be configured (pinned) consecutively. However, three addressing schemes must be considered and they are based upon the High-Performance Process Manager's card file configuration.

Two methods of pinning

Two methods of I/O Link Interface address pinning are described later in this subsection. The HPM files normally use jumpers to define (pin) the card file address. Zero-ohm resistors that are used in place of jumpers are soldered in at the factory only by special request.

Continued on next page

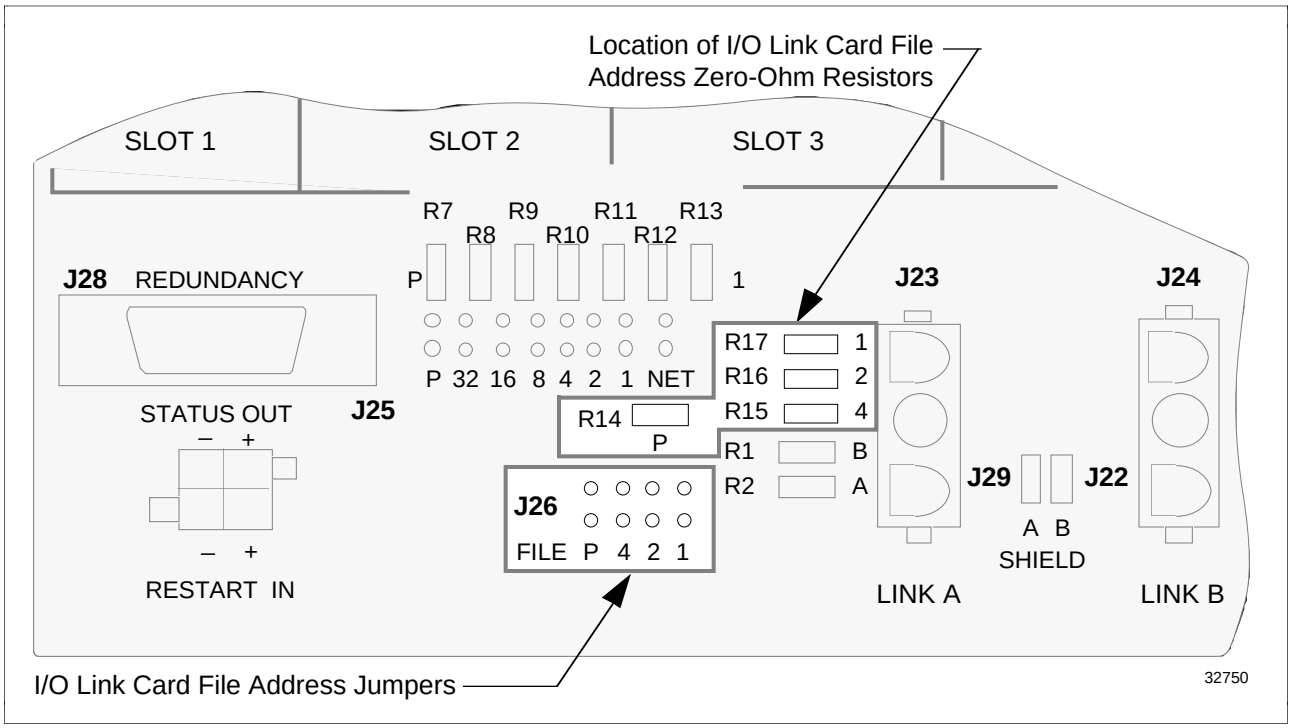
Nonredundant HPMM subsystem

For a HPM subsystem with a nonredundant HPMM and supporting I/O card files, the card file that contains the HPMM must be pinned for an I/O Link Interface address of zero (0), and the I/O card files that contain IOPs must be pinned for consecutive addresses that start at one (1).

See Figure 2-64 for the location of the jumpers on the 7-Slot card file and Figure 2-65 for the location of the jumpers on the 15-Slot card file. If IOP Only card files are used, see Figure 2-66.

Remember that software will see these card file addresses as a value of +1 when compared to the value actually pinned. (i. e. pinned value of 0 = card file 1, pinned value of 1 = card file 2, etc.)

Figure 2-64 Left 7-Slot Card File I/O Link Interface Address Pinning



7-Slot card files

If the HPMM is resident in a Left 7-Slot card file and a its Right 7-Slot card file exists, both 7-Slot card files must be pinned for an I/O Link Interface address of zero (0). The I/O card files that contain IOPs must be pinned for consecutively addresses that start at one (1).

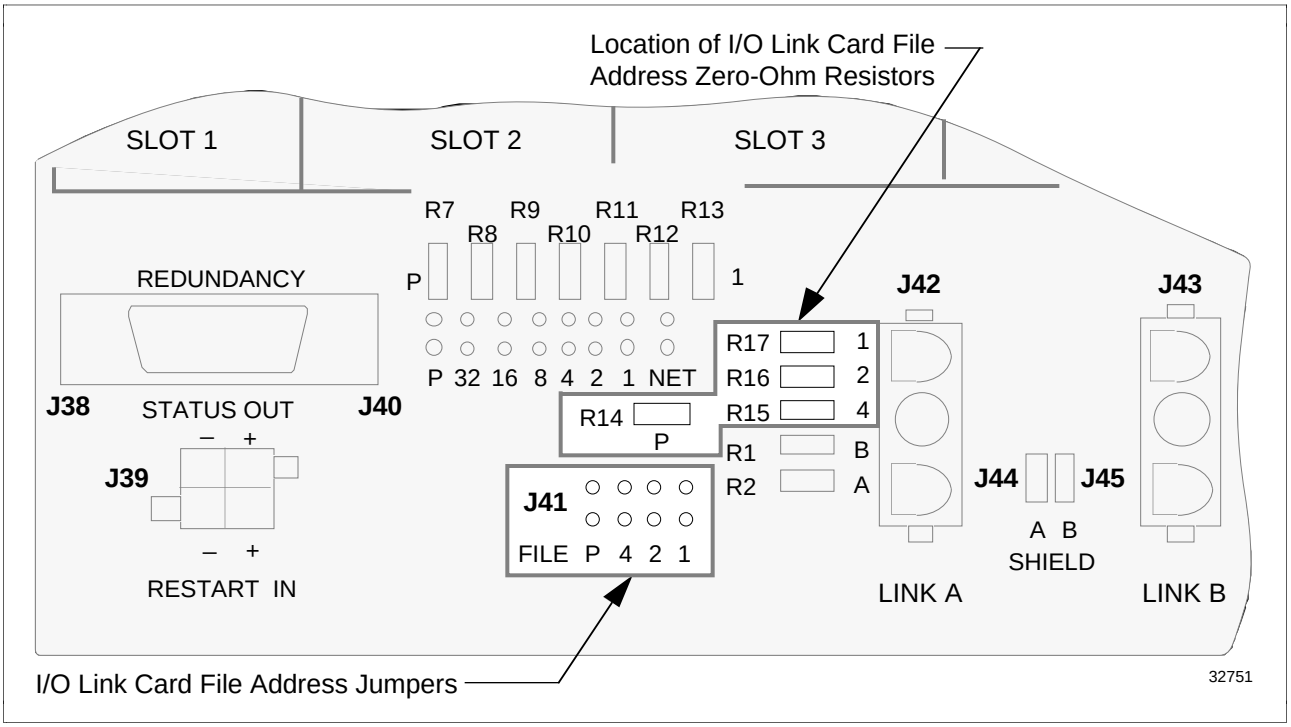
Continued on next page

2.16 I/O Link Interface Address Pinning, Continued

15-Slot card file redundant HPMM subsystem

When redundant HPMMs are installed in two 15-Slot card files, the first card file must be configured for I/O Link Interface address zero (0) and the second card file must be configured for I/O Link Interface address one (1). Any additional I/O card files in the HPM subsystem must be addressed consecutively, starting at I/O Link Interface address two (2). See Figure 2-65 for the location of the jumpers on the 15-Slot card file.

Figure 2-65 15-Slot Card File I/O Link Interface Address Pinning



7-Slot card file redundant HPM subsystem

When redundant HPMMs are installed in left and right 7-Slot card files, both 7-Slot card files must be configured for the same I/O Link Interface address of zero (0) since the left 7-Slot card file contains I/O slots 3 through 7, and the right 7-Slot card file contains I/O slots 9 through 15. Any additional I/O card files in the subsystem must be addressed consecutively, starting at I/O Link Interface address one (1). See Figure 2-64 for the location of the jumpers on the 7-Slot card files.

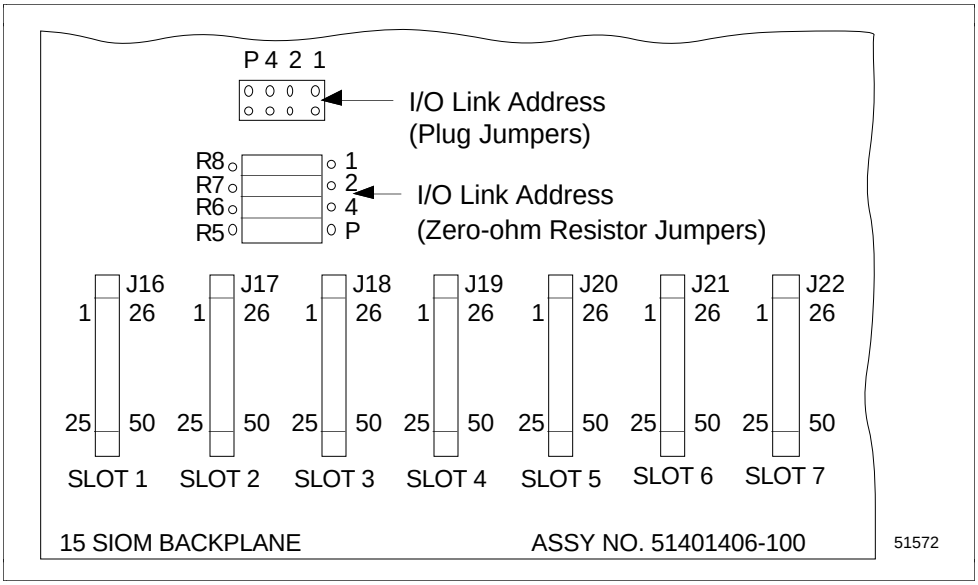
Continued on next page

2.16 I/O Link Interface Address Pinning, Continued

IOP Only card file pinning location

Figure 2-66 illustrates the location on the IOP Only card file backplane where the I/O Link Interface address is configured. The IOP Only card file may be part of the residual hardware from the upgrade of a PM or APM subsystem to an HPM subsystem.

Figure 2-66 IOP Only Card File I/O Link Interface Address Pinning



ATTENTION

ATTENTION – The numerical address displayed on the Operator Console displays is numbered one higher than the actual configured binary address. The binary card file address of 0 is displayed as a numerical address of 1 on the system displays.

Two pinning methods

A choice of two methods can be used to implement the I/O Link Interface addressing on the card file.

- Plug jumpers
- Zero-ohm resistor jumpers

One method only

One of the two methods must be disabled. Both cannot be active. Remove all jumpers and use the zero-ohm resistors or clip out the zero-ohm resistors and use the jumpers. The jumper method (without the resistors) is the most common method.

Continued on next page

Jumper method example

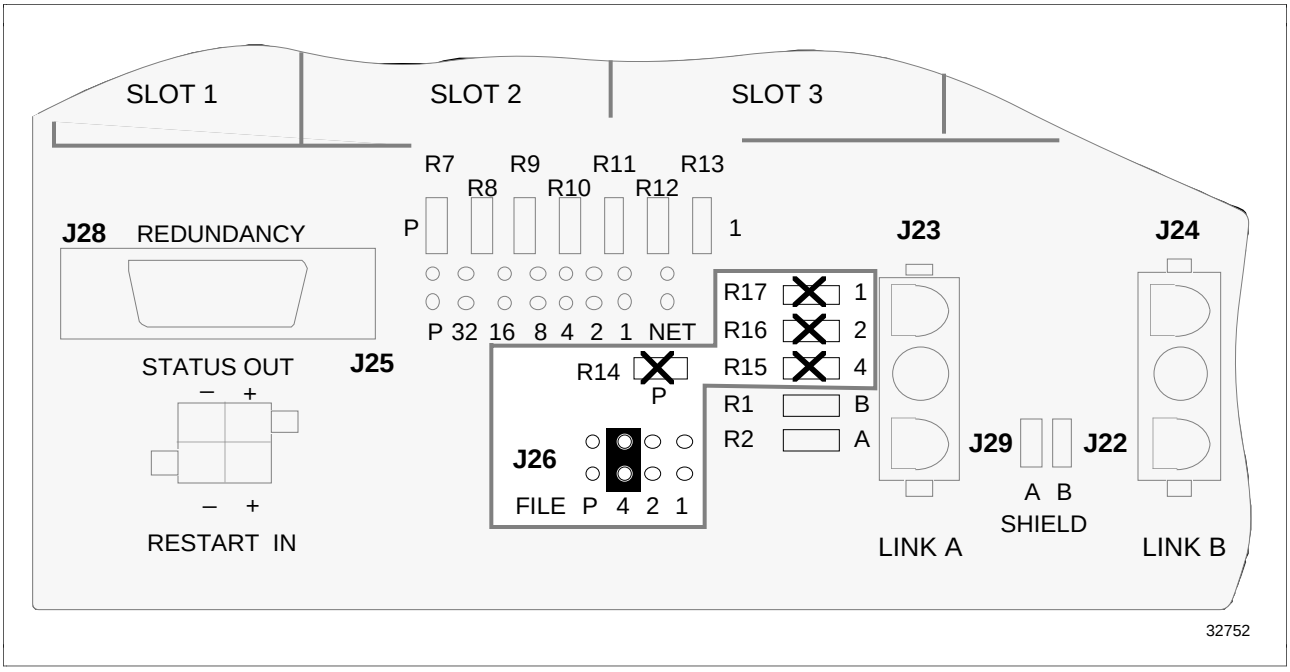
I/O Link Interface address configuration using plug jumpers is demonstrated with the following example.

Refer to Figure 2-67 to locate the card file pinning area (J26) in the following discussion.

Assume an I/O card file is to be configured for an I/O Link Interface hardware address of 4. The Operator Console will display this card file's I/O Link Interface address as 5. Take diagonal cutters and remove all the zero-ohm resistors. Install a plug jumper to bridge both pins at position 4. Because this single jumper constitutes an odd number of jumpers, remove the P (parity) plug jumper as well as all others.

Even though the J-number (J26 in this case) differs between the 7-Slot and 15-Slot card files, the method of pinning the card file address remains the same.

Figure 2-67 Left 7-Slot Card File I/O Link Interface Address Pinning with Plug Jumpers



Continued on next page

2.16 I/O Link Interface Address Pinning, Continued

Zero-ohm resistor jumper pinning example

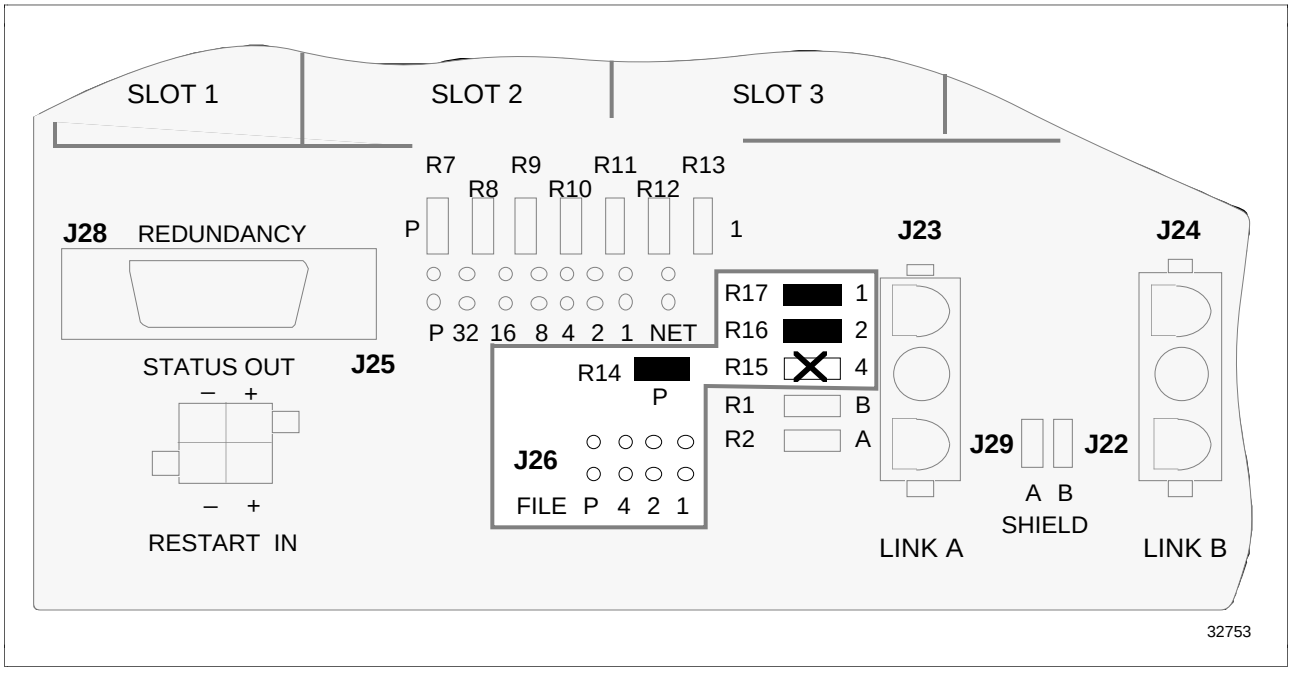
I/O Link Interface address configuration using zero-ohm resistor jumpers is demonstrated with the following 7-Slot card file example.

Refer to Figure 2-68 to locate the card file resistor jumper area in the following discussion.

An I/O card file is to be configured for an I/O Link Interface hardware address of 3. The Operator Console will display this card file's address as 4. Remove all the plug jumpers and set them aside. A logic one is created by leaving the zero-ohm resistor in place, a zero is created by removing the zero-ohm resistor. Leave the zero-ohm resistors at positions 1 and 2 (1 + 2 = 3), and leave the P (parity) zero-ohm resistor because an odd number of jumpers is required. Remove all other zero-ohm resistors with diagonal cutters.

Even though the jack number (J28 in this case) differs between the 7 and 15-Slot card files, the method of pinning the card file address remains the same.

Figure 2-68 Left 7-Slot Card File I/O Link Interface Address Pinning with Zero-Ohm Resistors



CAUTION

CAUTION—If a zero-ohm resistor jumper is incorrectly removed, do not attempt to correct the problem by resoldering the jumper. The backplane is easily damaged. Instead, remove all the zero-ohm resistor jumpers and configure the card file's I/O Link Interface address with the plug jumpers.

2.17 Firmware/Hardware/Software Correlation

Relationship

A definite correlation exists between the High-Performance Process Manager's firmware, hardware, and software. An explanation of this relationship and the latest information can be found in Appendix K of the *Customer Release Guide* manual.

Section 3 – UCN Status Displays

3.1 Overview

Section contents The topics covered in this section are:

	Topic	See Page
3.1	Overview	113
3.2	Display Definitions	115
3.2.1	NIM Detail Status Displays	115
3.2.2	HPMM Detail Status Displays	115
3.2.3	IOP Detail Status Displays	116
3.3	Detail Status Display Selection Procedures	116
3.3.1	NIM Detail Status Display	116
3.3.2	HPMM Detail Status Display	119
3.3.3	IOP Detail Status Display	121
3.4	Display Operation	122
3.4.1	UCN Status Displays	122
3.4.1.1	LOAD/SAVE RESTORE Target	127
3.4.1.2	CONTROL STATES Target	129
3.4.1.3	AUTO CHECKPT Target	131
3.4.1.4	UCN CABLE STATUS Target	133
3.4.1.5	RUN STATES Target	140
3.4.1.6	SLOT SUMMARY Target	142
3.4.1.7	DETAIL STATUS Target	143
3.4.2	HPM Status Displays	144
3.4.2.1	LOAD/SAVE RESTORE Target	151
3.4.2.2	CONTROL STATES Target	153
3.4.2.3	AUTO CHECKPT Target	154
3.4.2.4	IOL CABLE COMMANDS Target	155
3.4.2.5	RUN STATES Target	157
3.4.2.6	SLOT SUMMARY Target	159
3.4.2.7	DETAIL STATUS Target	160
3.4.3	NIM Detail Status Displays	161
3.4.4	HPMM Detail Status Displays	166
3.4.4.1	HPMM I/O Link Information Displays	169
3.4.4.2	IOM I/O Link Information Displays	173
3.4.4.3	HPMM Version/Revision Display	175
3.4.4.4	HPMM Control Configuration Display	177
3.4.4.5	HPM Write Lockout Displays	180
3.4.4.6	HPMM Schedule Information Display	183
3.4.4.7	HPMM UCN Statistics Displays	185
3.4.4.8	HPMM Maintenance Support Displays	187
3.4.4.9	HPMM Soft Failure Displays	194
3.4.5	IOP Detail Status Displays	197
3.4.5.1	IOP Box Soft Failures Displays	201
3.4.5.2	IOP Slot Soft Failures Displays	205
3.4.5.3	IOP Slots with Soft Failures Display	208
3.4.5.4	HLAI IOP Detail Status Display	209
3.4.5.5	LLAI IOP Detail Status Display	211
3.4.5.6	AO IOP Detail Status Display	216
3.4.5.7	LLMux IOP Detail Status Display	220

Continued on next page

Section contents

The topics covered in this section are:

	Topic	See Page
3.4.5.8	DI IOP Detail Status Display	223
3.4.5.9	DO IOP Detail Status Display	224
3.4.5.10	STI/STIM IOP Detail Status Display	226
3.4.5.11	PI IOP Detail Status Display	227
3.4.5.12	SDI IOP Detail Status Display	228
3.4.5.13	SI IOP Detail Status Display	229
3.4.5.14	DISOE IOP Detail Status Display	230

Introduction

The information in this section is intended to assist the reader in the operation and understanding of UCN Status displays as a service tool for the High-Performance Process Manager equipment. The UCN Status displays consist of three categories of displays, the NIM Detail Status displays, the HPMM Detail Status displays, and the IOP Detail Status displays for the following types of Input/Output Processors (IOPs).

- High Level Analog Input (HLAI)
- Low Level Analog Input (LLAI)
- Analog Output (AO)
- Digital Input (DI)
- Digital Output (DO)
- Smart Transmitter Interface (STIM)
- Low Level Multiplexer (LLMux)
- Pulse Input (PI)
- Serial Device Interface (SDI)
- Serial Interface (SI)
- Digital Input Sequence Of Events (DISOE)

References

Numerous references in this section are made to figures that represent screen prints of the actual Universal Station Console displays. It should be possible for the reader to make use of either the figures in this section, or the screen display on an available Universal Station hosting the Operator or Universal personality as a training or service tool.

Release 500 software displays

The displays shown in this section are reproductions of console screens created by Release 500 software.

3.2 Display Definitions

IOM definition

A common word in the display discussion is the term “IOM.” The Input /Output Module (IOM) is the Input/Output Processor (IOP) card that resides in an High-Performance Process Manager card file. It interfaces to an associated Field Termination Assembly (FTA). In the case of redundancy, the IOM consists of two IOPs with the associated FTA.

Target selection

Often, a figure has the title of a display followed by the name of a target on a display, such as: **IOM IOL INFO**. This is the target that must be selected on a previous display to produce the display in the figure.

3.2.1 NIM Detail Status Displays

Introduction

These displays provide the operator with access to the current status of a primary or secondary NIM as a UCN node. The display contains a fixed portion showing the current state of the NIM on the UCN and a set of targets that invoke displays of the UCN Driver configuration and the NIM local UCN statistics. The NIM Local UCN Statistics display has a target that allows the operator to reset the UCN Driver statistics for test purposes.

3.2.2 HPMM Detail Status Displays

Introduction

These displays provide the operator with access to the current status of a primary or secondary HPMM. The display contains a fixed portion showing the current status of the HPMM on the UCN and a set of targets that permits display of the following information.

- The status of the HPMM as a node on the I/O Link Interface
- The status of the I/O Link Supervisor (IOS) for a primary HPMM
- The current version/revision/personality and firmware version of the HPMM’s I/O Link, Communications, and Control processors
- Configuration of the HPMM Control processor (primary HPMM only)
- The current UCN communications statistics with reset capabilities
- The error information captured in the HPMM memory
- The current Soft failures in the HPMM
- A summary of the current I/O Link status of each IOP attached to the primary HPMM

3.2.3 IOP Detail Status Displays

Purpose

These displays provide the operator with access to the current status of a given IOP in the High-Performance Process Manager. The display consists of a fixed portion showing information common to all IOPs, and a variable portion showing information dependent on the IOP type. The display provides operator interaction that permits the following activity.

- Resetting of the IOP error counts
- Enabling/disabling of the IOP calibration operations
- Display and alteration of the IOP specific parameters

3.3 Detail Status Display Selection Procedures

Introduction

There are three types of Detail Status displays that can be selected. The following subsections detail the procedures to invoke the initial Detail Status display. The "Display Operation" subsection, 3.4, details the use of the display targets and descriptions of the displays.

3.3.1 NIM Detail Status Display

Display selection procedure

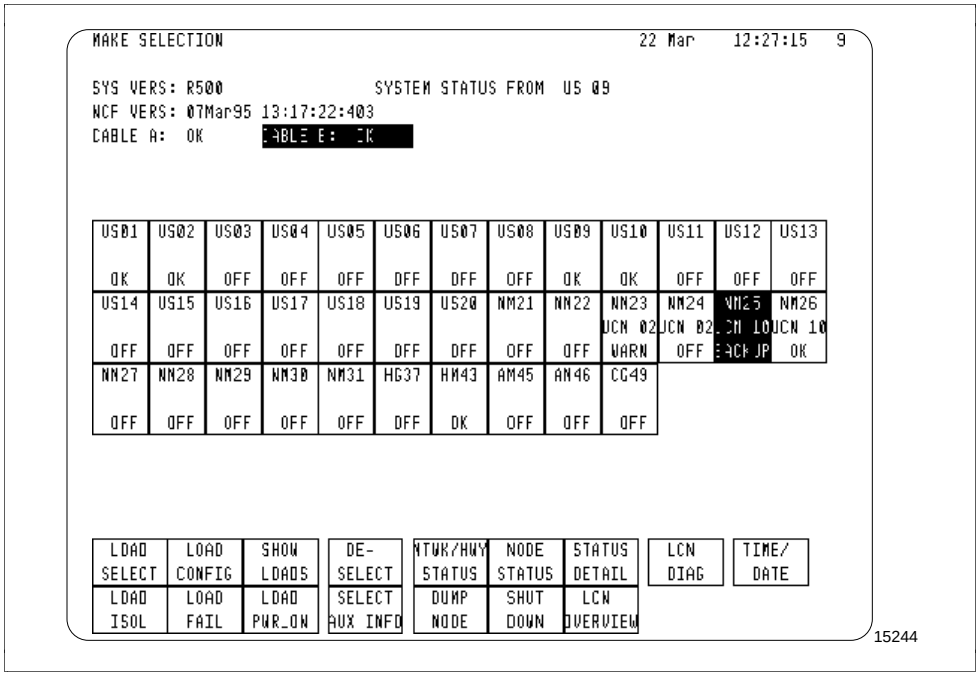
Use the following procedure to select a NIM Detail Status display.

Step	Action
1	Depress the **<SYST STAT>** (System Status) key on the console to invoke the System Status display. The System Status display is shown in Figure 3-1.
2	Choose the NIM node on the display grid and then select the **NTWK/HWY** target on the System Status display for the network you wish to examine to invoke the UCN Status display. The UCN Status display is shown in Figure 3-2.
3	Choose the NIM of interest on the display grid and then select the **DETAIL STATUS** target on the UCN Status display to invoke the NIM Detail Status display. The NIM Detail Status display is shown in Figure 3-3.

Continued on next page

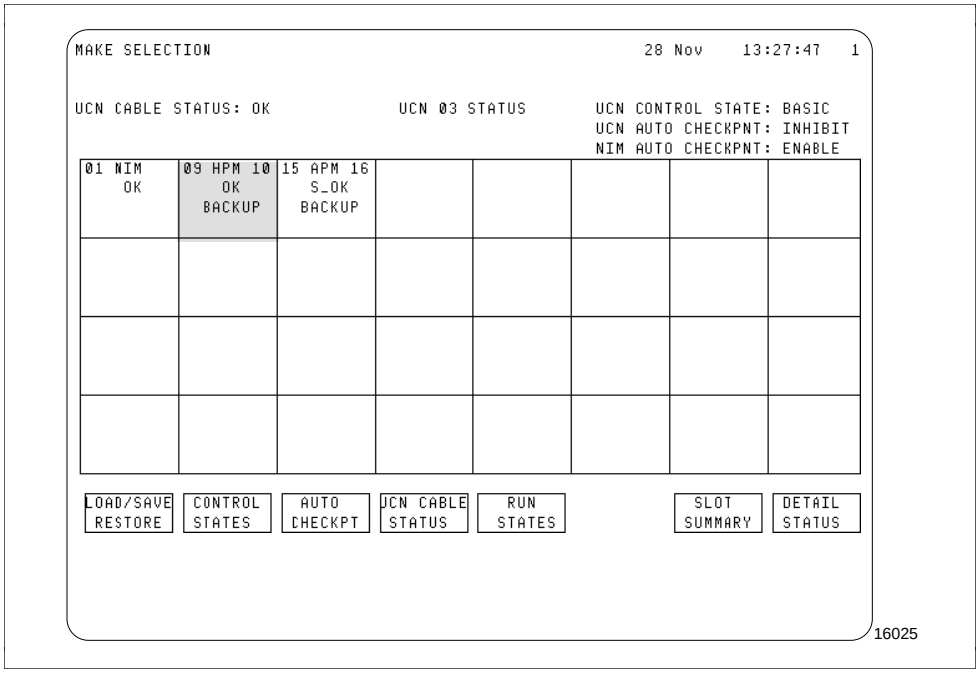
System Status display

Figure 3-1 System Status Display



UCN Status display

Figure 3-2 UCN Status Display

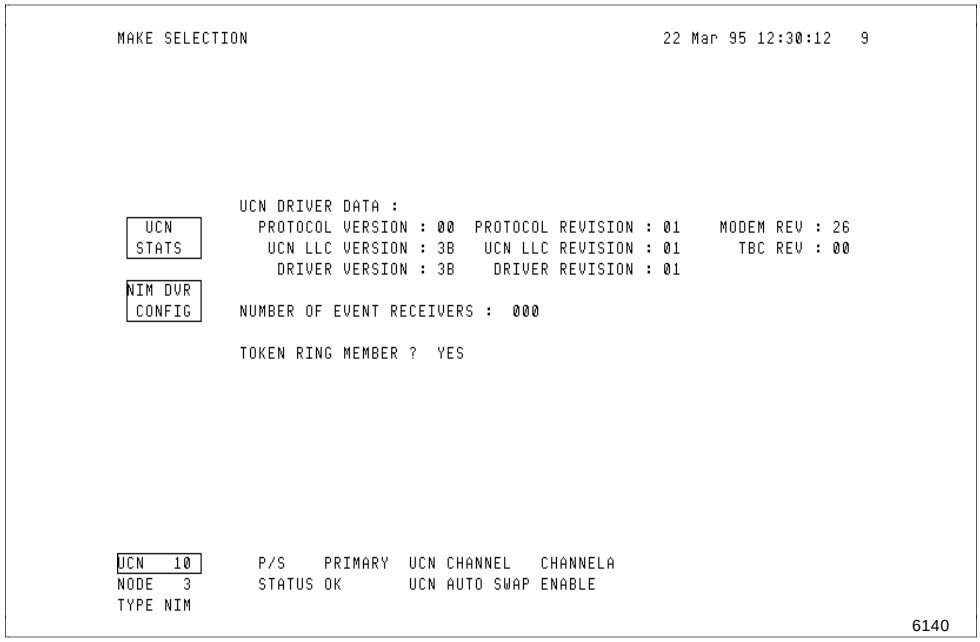


Continued on next page

3.3.1 NIM Detail Status Display, Continued

NIM Detail Status display

Figure 3-3 NIM Detail Status Display



3.3.2 HPMM Detail Status Display

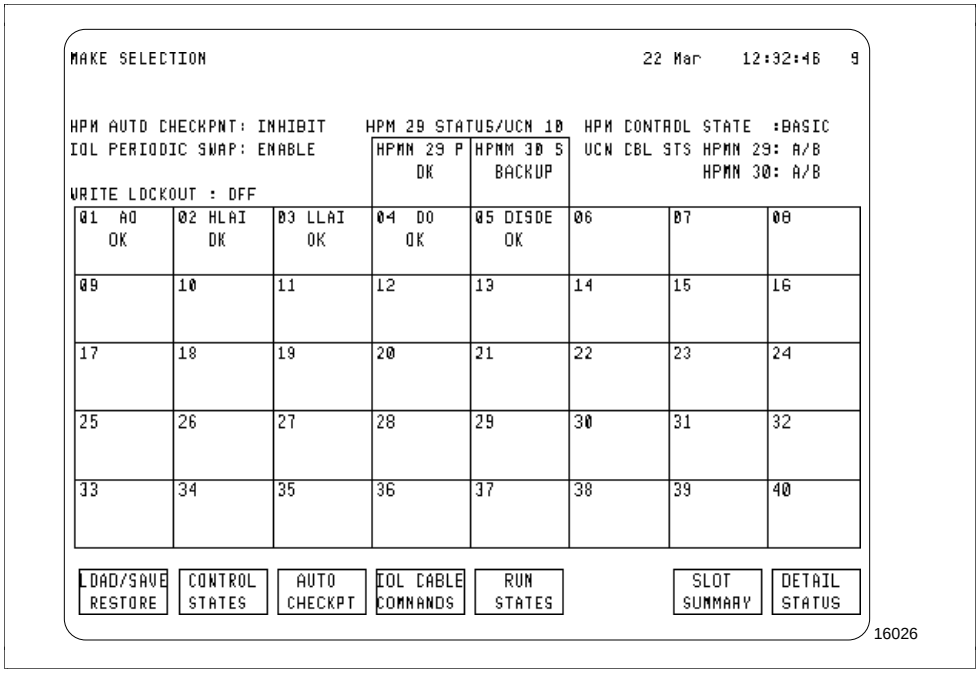
Display selection procedure

Use the following procedure to select an HPMM Detail Status display.

Step	Action
1	Depress the **<SYST STAT>** (System Status) key on the console to invoke the System Status display. The System Status display is shown in Figure 3-1.
2	Choose the NIM node on the display grid and then select the **NTWK/HWY** target on the System Status display for the network you wish to examine to invoke the UCN Status display. The UCN Status display is shown in Figure 3-2.
3	Choose the HPM of interest on the display grid and then select the **DETAIL STATUS** target on the UCN Status display to invoke the HPM Status display. The HPM Status display is shown in Figure 3-4.
4	Choose the HPMM (primary or secondary) of interest on the display grid and then select the **DETAIL STATUS** target on the HPM Status display to invoke the primary or secondary HPMM Detail Status display. The primary and secondary HPMM Status displays are shown in Figures 3-5 and 3-6, respectively.

HPM Status display

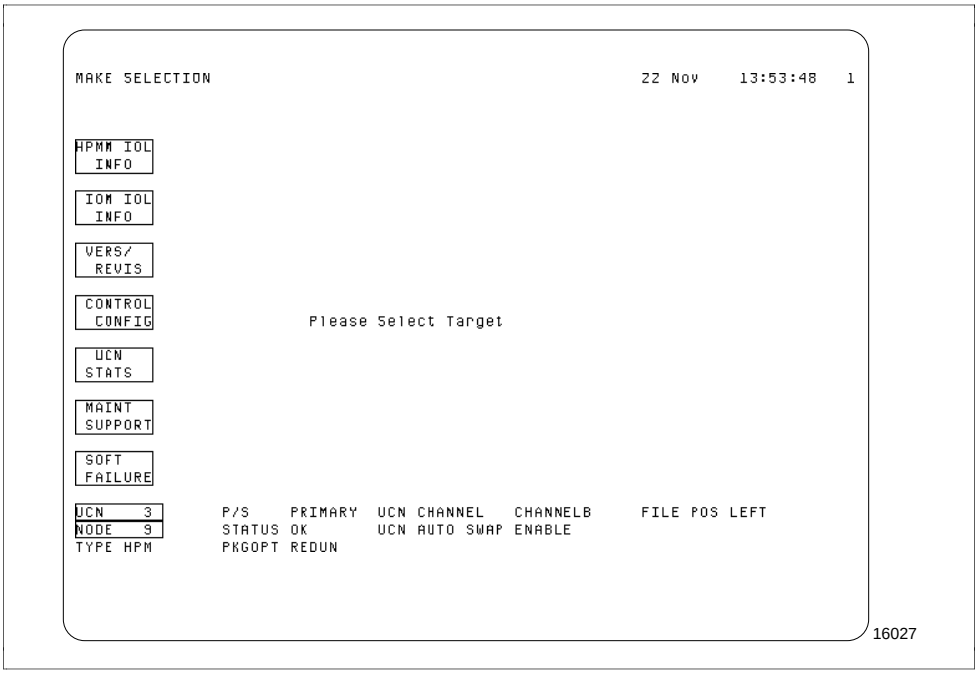
Figure 3-4 HPM Status Display



Continued on next page

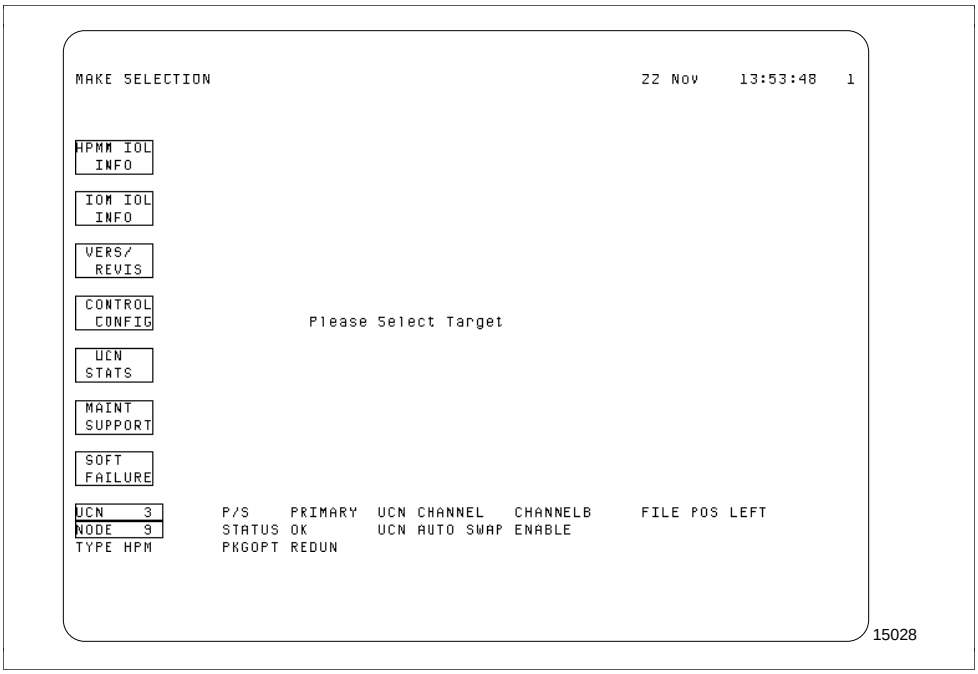
Primary HPMM Detail Status display

Figure 3-5 Primary HPMM Detail Status Display



Secondary HPMM Detail Status display

Figure 3-6 Secondary HPMM Detail Status Display



3.3.3 IOP Detail Status Display

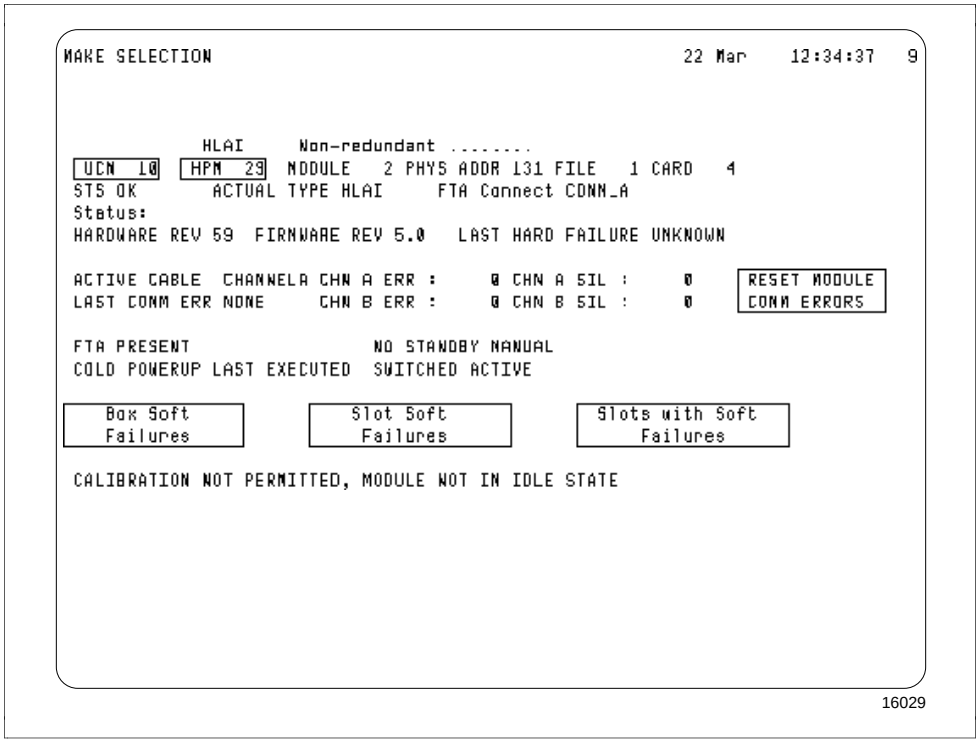
IOP Detail Status displays

Use the following procedure to select an IOP Detail Status display.

Step	Action
1	Depress the **<SYST STAT>** (System Status) key on the console to invoke the System Status display. The System Status display is shown in Figure 3-1.
2	Choose the NIM node on the display grid and then select the **NTWK/HWY** target on the System Status display for the network you wish to examine to invoke the UCN Status display. The UCN Status display is shown in Figure 3-2.
3	Choose the HPM that is associated with the IOP of interest on the display grid and then select the **DETAIL STATUS** target on the UCN Status display to invoke the HPM Status display. The HPM Status display is shown in Figure 3-4.
4	Choose the IOP of interest on the display grid and then select the **DETAIL STATUS** target on the HPM Status display to invoke the IOP Detail Status display. An example of an IOP Detail Status display is shown in Figure 3-7.

IOP Detail Status display

Figure 3-7 IOP Detail Status Display



3.4 Display Operation

Introduction

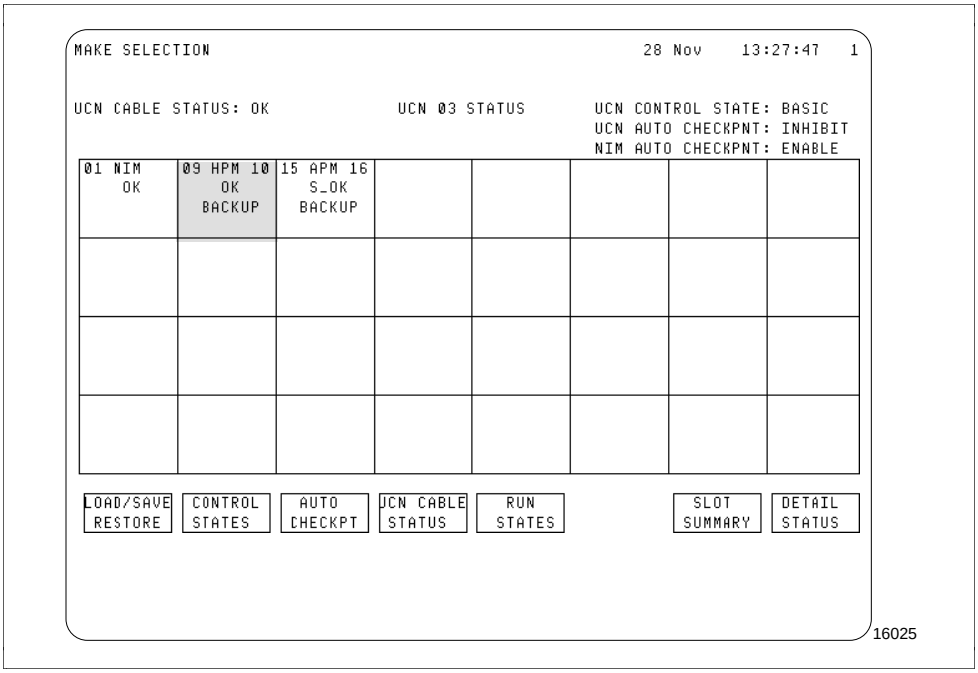
The following subsections describe the selection procedures for the UCN Status display, HPM Status display, IOP Status display, and their associated displays. The status, statistics, and targets on the displays are also described.

3.4.1 UCN Status Displays

UCN Status display

The UCN Status display is shown in Figure 3-8. The display is obtained by selecting the <**SYST STATS**> (System Status) key on the console and then selecting the **PROCESS NETWORK STATUS** target on the display for the network you wish to examine.

Figure 3-8 UCN Status Display



Three display sections

The display is divided into three sections.

Continued on next page

3.4.1 UCN Status Displays, Continued

Top section of display

The top section of the display provides information about the Universal Control Network (UCN).

The UCN status at the top of the display is defined in Table 3-1.

Table 3-1 UCN Status Display – UCN/NIM Status

Term	Definition
UCN CABLE STATUS	Indicates status of the UCN cables. (OK or FAIL)
UCN CONTROL STATE	There are two control states. The BASIC state does not permit LCN devices to write to any devices on the UCN. The FULL state permits LCN devices to write to the UCN devices.
UCN AUTO CHECKPNT	There are two automatic UCN Checkpoint states. The ENABLE state permits automatic Checkpointing. The database is saved in the History Module periodically for the devices that are individually Checkpoint enabled. The INHIBIT state prevents all devices on the UCN from Checkpointing.
NIM AUTO CHECKPNT	There are two automatic NIM Checkpoint states. The ENABLE state permits automatic Checkpointing. The database is saved in the History Module periodically for the devices that are individually Checkpoint enabled. The DISABLE state prevents all devices on the UCN from Checkpointing.

Middle section of display

The "status boxes" in the middle grid-like section of the display provide the status of the configured UCN node.

Type of device

The type of device on the UCN is identified at the upper center of the status box, such as HPM, APM, PM, LM, or NIM.

Primary or secondary

When redundant, the numerals in the left and right upper corners identify the primary and secondary (if present) node addresses of the device, respectively.

Device status

Two lines in the center of the status box indicate the device's primary and secondary (if present) status. For the HPM, the first line is the composite status of the primary HPMM, and the second line is the status of the secondary HPMM. The composite primary HPMM status reflects the status of the HPMM and all the IOPs.

Continued on next page

Status box target

The status box is also a target. A command target selected at the bottom of the display will execute the command, if applicable, for the status box chosen.

Selecting the status box target

When chosen, the status box is backlighted blue and the primary HPMM address is highlighted in white. Choosing the same status box a second time, before selecting a command target, highlights the secondary HPMM address. A status box selection toggles between the primary HPMM address and the secondary HPMM address each time it is chosen. Selecting a command target will execute a command against the primary or secondary HPMM, whichever has been chosen.

Continued on next page

Primary HPMM status

The possible status of the primary HPMM is defined in Table 3-2 with the color of the text indicated.

Table 3-2 UCN Status Display – Primary HPMM Status

Term	Definition
OK (Text color – blue)	Processing is in progress.
ALIVE (Text color – yellow)	Power is present, but no database or personality program is loaded.
IDLE (Text color – yellow)	The database and personality program are loaded, but no processing is in progress.
IOIDLE (Text color – yellow)	One or more IOPs are in the Idle state.
LOADING (Text color – yellow)	The HPM is being loaded with its personality program and database.
NOTCONFG (Text color – yellow)	There is no UCN node configured for the HPM's UCN node address.
POWERON (Text color – yellow)	The HPM is responding to the UCN but has not performed its self-tests. This is a transitory state that occurs when the HPMM is first powered on.
CONFGMIS (Text color – red)	The configured node type for the HPM's UCN node does not match the actual node type.
FAIL (Text color – red)	The HPM has a Hard failure and access to IOP status and data is unavailable. HPM control functions have ceased. Effectively, this is a total failure.
OFFNET (Text color – red)	The HPM is not responding on the UCN because 1) it does not exist, 2) power is off, or 3) there is a hardware failure that prohibits a response.
PARTFAIL (Text color – red)	There are one or more Partial failures.
PF_IDLE (Text color – red)	There are one or more Partial failures and the HPMM is in the Idle state.
PF_IOIDL (Text color – red)	There are one or more Partial failures, and at least one IOP is in the Idle state.

Continued on next page

Secondary HPMM status

The possible status of the secondary HPMM is defined in Table 3-3 with the color of the text indicated.

Table 3-3 UCN Status Display – Secondary HPMM Status

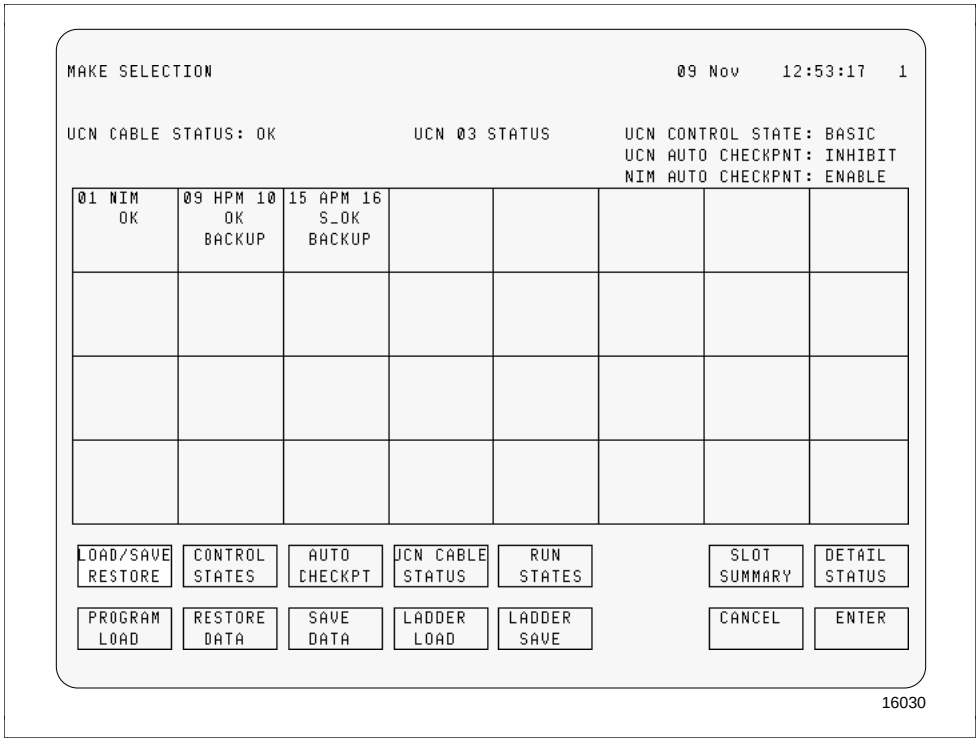
Term	Definition
BACKUP (Text color – blue)	Processing is in progress and the secondary HPMM database is synchronized with the primary HPMM database.
BKUP_SF (Text color – blue)	The HPMM is in the Run state, but has a Soft failure.
ALIVE (Text color – yellow)	Power is present, but no database or personality program is loaded.
BACKUP (Text color – yellow)	The secondary HPMM is in the Idle state, or its database is not synchronized with the primary HPMM.
BKUP_SF (Text color – yellow)	The HPMM is in the Idle state, but has a Soft failure.

3.4.1.1 LOAD/SAVE RESTORE Target

LOAD/SAVE RESTORE target

Selection of the **LOAD/SAVE RESTORE** command target on the UCN Status display invokes additional targets at the bottom of the display to either load the personality program, restore the database, or save the database for the UCN device chosen by its status box as shown in Figure 3-9.

Figure 3-9 UCN Status Display – LOAD/SAVE RESTORE Target Selected



Not applicable for NIM

The LOAD/SAVE RESTORE target functions are not applicable when a NIM is chosen on the UCN Status display.

Command targets

The command targets at the bottom of the display in Figure 3-9 perform the functions defined in Table 3-4.

Continued on next page

3.4.1.1 LOAD/SAVE RESTORE Target, Continued

LOAD/SAVE RESTORE display targets

The command targets at the bottom of the display in Figure 3-9 perform the functions that are defined in Table 3-4.

Table 3-4 UCN Status Display – LOAD/SAVE RESTORE Target Selected

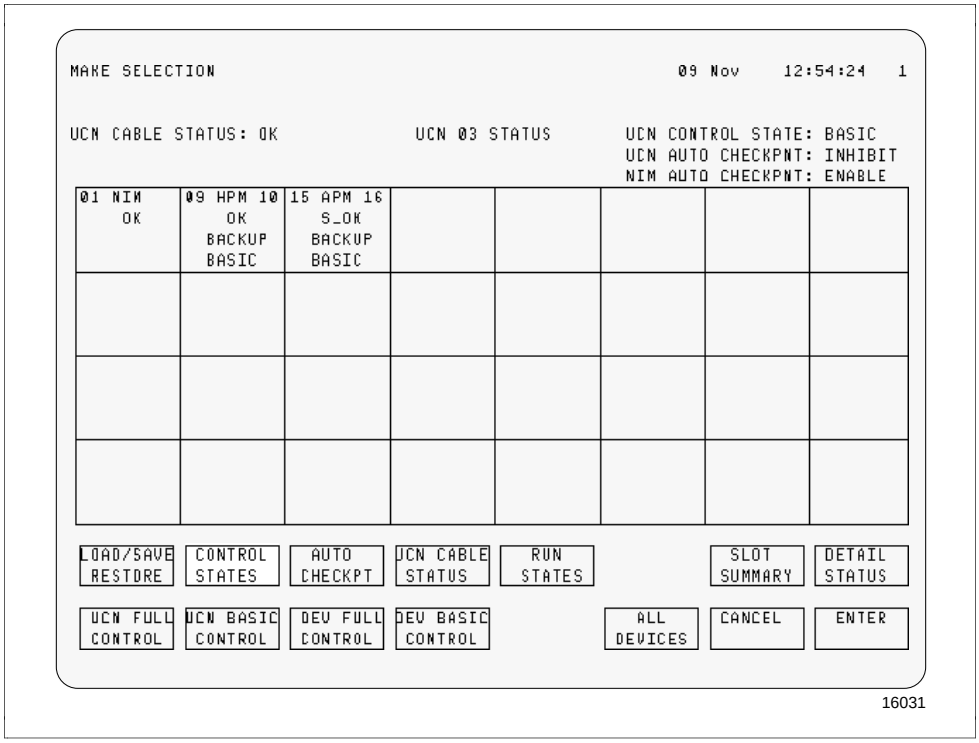
Target	Function
PROGRAM LOAD	Loads the program and data to the chosen UCN device. The device must be in the Alive state. The command is executed by selecting the ENTER target.
RESTORE DATA	Restores the database to the chosen UCN device. The device must be in the Idle state. The command is executed by selecting the ENTER target.
SAVE DATA	Saves the database from the chosen UCN device into either the History Module or removable media. This is sometimes called “Checkpointing.” The command is executed by selecting the ENTER target.
LADDER LOAD	This is a Logic Manager function.
LADDER SAVE	This is a Logic Manager function.
CANCEL	Clears the LOAD PROGRAM, RESTORE DATA, SAVE DATA, LADDER LOAD, LADDER SAVE, and ENTER command targets from the display.
ENTER	The ENTER target must be selected for the chosen LOAD/SAVE RESTORE function to be executed.

3.4.1.2 CONTROL STATES Target

CONTROL STATES target

Selecting the **CONTROL STATES** command target on the UCN Status display in Figure 3-10 invokes additional targets at the bottom of the display to change the control state of the UCN or the UCN device chosen by its status box.

Figure 3-10 UCN Status Display – CONTROL STATES Target Selected



Not applicable for NIM

The CONTROL STATES target functions are not applicable when a NIM is chosen on the UCN Status display.

Continued on next page

3.4.1.2 CONTROL STATES Target, Continued

CONTROL STATES display targets

The command targets at the bottom of the display in Figure 3-10 perform the functions defined in Table 3-5.

Table 3-5 UCN Status Display – CONTROL STATES Target Selected

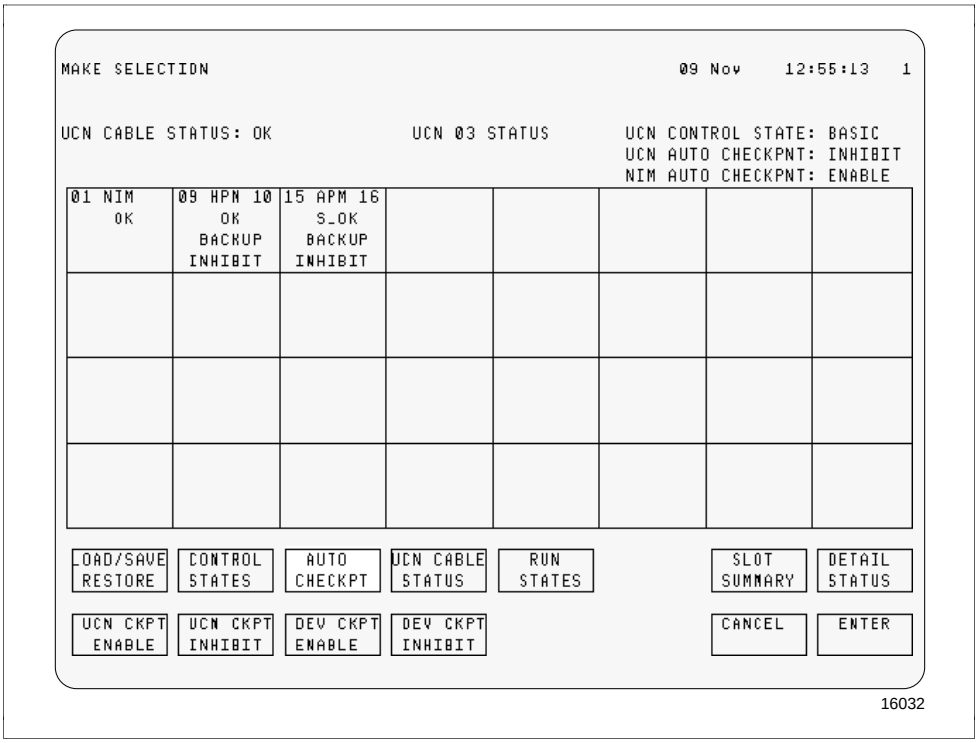
Target	Function
UCN FULL CONTROL	Changes the UCN's control state to FULL. The command is executed by selecting the ENTER target.
UCN BASIC CONTROL	Changes the UCN's control state to BASIC. The command is executed by selecting the ENTER target.
DEV FULL CONTROL	Changes the HPM's control state to FULL. The command is executed by selecting the ENTER target.
DEV BASIC CONTROL	Changes the HPM's control state to BASIC. The command is executed by selecting the ENTER target.
ALL DEVICES	Causes all the UCN devices to be affected by a control state change.
CANCEL	Clears the UCN FULL CONTROL, UCN BASIC CONTROL, DEV FULL CONTROL, DEV BASIC CONTROL, ALL DEVICES, and ENTER command targets from the display.
ENTER	The ENTER target must be selected for the chosen CONTROL STATES function to be executed.

3.4.1.3 AUTO CHECKPT Target

AUTO CHECKPT target

Selection of the **AUTO CHECKPT** command target invokes additional targets at the bottom of the display to change the Checkpointing state of the UCN or of the UCN device chosen by its status box as shown in Figure 3-11.

Figure 3-11 UCN Status Display – AUTO CHECKPT Target Selected



Not applicable for NIM

The AUTO CHECKPT target functions are not applicable when a NIM is chosen on the UCN Status display.

Continued on next page

3.4.1.3 AUTO CHECKPT Target, Continued

AUTO CHECKPT display targets

The command targets at the bottom of the display in Figure 3-11 perform the functions defined in Table 3-6.

Table 3-6 UCN Status Display – AUTO CHECKPT Target Selected

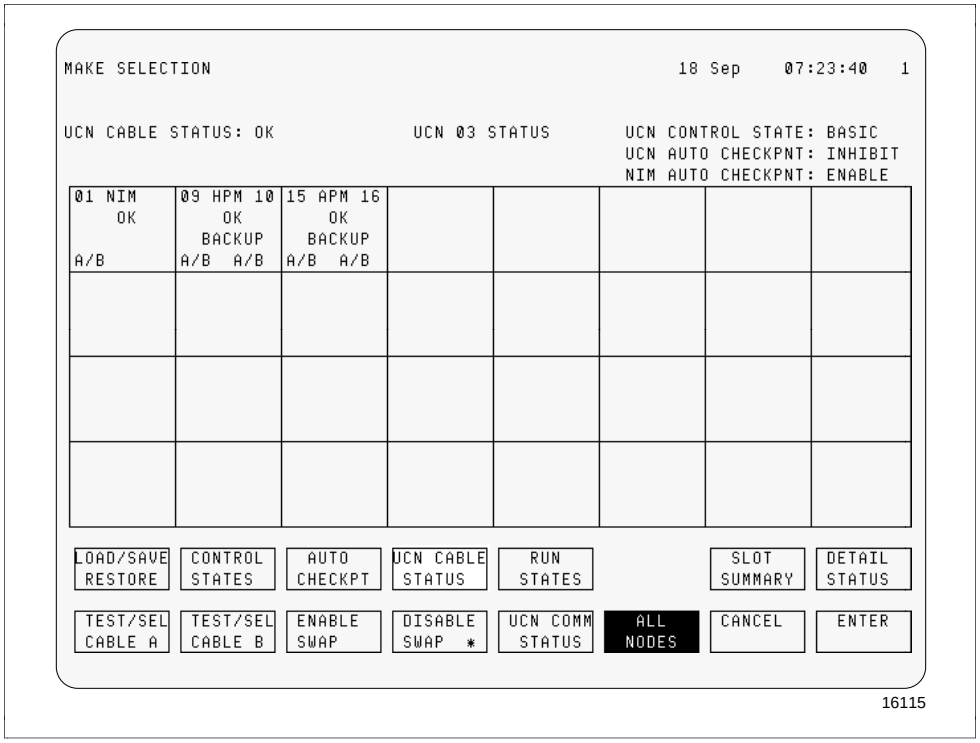
Target	Function
UCN CKPT ENABLE	Enables automatic Checkpointing of all the UCN devices. The command is executed by selecting the ENTER target.
UCN CKPT INHIBIT	Disables automatic Checkpointing of all the UCN devices. The command is executed by selecting the ENTER target.
DEV CKPT ENABLE	Enables automatic Checkpointing of the UCN device chosen by its status box. The command is executed by selecting the ENTER target.
DEV CKPT INHIBIT	Disables automatic Checkpointing of the UCN device chosen by its status box. The command is executed by selecting the ENTER target.
CANCEL	Clears the UCN CKPT ENABLE, UCN CKPT INHIBIT, DEV CKPT ENABLE, DEV CKPT INHIBIT, and ENTER command targets.
ENTER	The ENTER target must be selected for the chosen AUTO CHECKPT function to be executed.

3.4.1.4 UCN CABLE STATUS Target

UCN CABLE STATUS target

Selection of the **UCN CABLE STATUS** target on the UCN Status display as shown in Figure 3-12 invokes additional targets at the bottom of the display to change the active UCN cable or enable/disable automatic cable swapping.

Figure 3-12 UCN Status Display – UCN CABLE STATUS Target Selected



UCN COMM STATUS target

If a UCN node is selected after the **UCN COMM STATUS** target is selected, the **ENABLE SWAP** and **DISABLE SWAP** targets are removed at the bottom of the display, and the **TEST/SEL CABLE A** and **TEST/SEL CABLE B** targets are replaced by the **BACKUP CABLE TST** target as shown in Figures 3-13 and 3-14.

BACKUP CABLE TST target

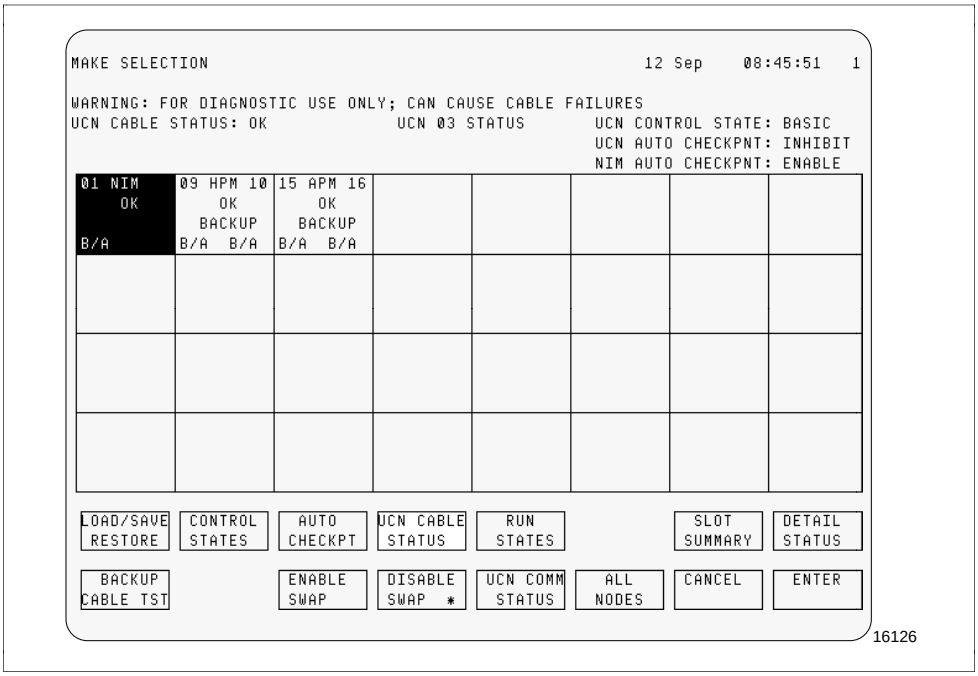
If the **BACKUP CABLE TST** target is selected, the UCN node will perform the Backup Cable test.

Continued on next page

3.4.1.4 UCN CABLE STATUS Target, Continued

NIM node/UCN CABLE STATUS targets selected

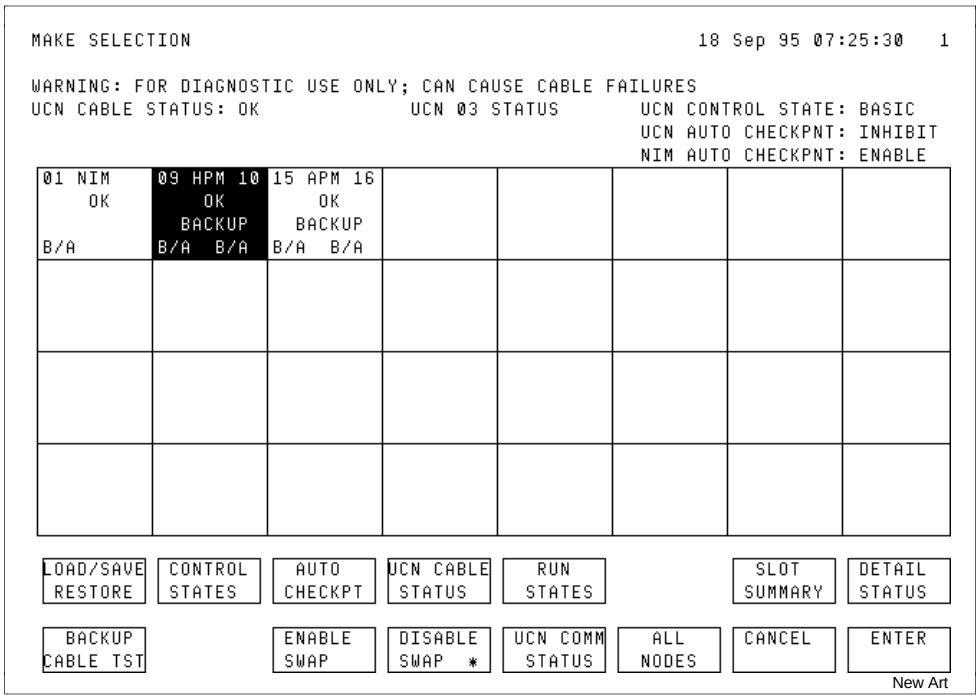
Figure 3-13 UCN Status Display – NIM Node and UCN CABLE STATUS Targets Selected



Continued on next page

HPM node/UCN CABLE STATUS targets selected

Figure 3-14 UCN Status Display – HPM Node and UCN CABLE STATUS Targets Selected



UCN CABLE STATUS targets

Table 3-7 defines the functions of the **UCN CABLE STATUS** targets.

Table 3-7 UCN Status Display – UCN CABLE STATUS Target Selected

Target	Function
TEST/SEL CABLE A	Initiates a Backup Cable Test sequence for UCN cable A. If no faults are detected, UCN cable A is activated for all UCN devices. The command is executed by selecting the ENTER target.
TEST/SEL CABLE B	Initiates a Backup Cable Test sequence for UCN cable B. If no faults are detected, UCN cable B is activated for all UCN devices. The command is executed by selecting the ENTER target.
ENABLE SWAP	Enables periodic swapping of the UCN cables. The command is executed by selecting the ENTER target.
DISABLE SWAP	Disables periodic swapping of the UCN cables. The command is executed by selecting the ENTER target.

Continued on next page

UCN CABLE STATUS targets, continued

Table 3-7 UCN Status Display – UCN CABLE STATUS Target Selected, Continued

Target	Function
UCN COMM STATUS	Selecting the UCN COMM STATUS target produces the UCN Network Statistics display as shown in Figure 3-15 which displays the statistics of the UCN nodes and provides the capability to do a global reset of the communications statistics. The reset is executed by first selecting the RESET STATS target and then selecting the ENTER target. When a node (NIM or HPM) is selected on the UCN Network Statistics display, the TEST/SEL CABLE A, TEST/SEL CABLE B, ENABLE SWAP, and DISABLE SWAP targets are replaced by the BACKUP CABLE TST target as shown in Figure 3-16. Selecting one of the SELECT NODES targets on the UCN Statistics display displays the statistics for a group of sixteen UCN nodes. The initial UCN Network Statistics display provides statistics for the first group of sixteen (16) nodes on the Universal Control Network that you previously selected. There are four groups. The node group of interest is chosen by selecting one of four targets, SELECT NODES 1-16 (initially displayed), 17-32, 33-48, or 49-64. The UCN Network Statistics 1-16 display selected by the SELECT NODES 1-16 target is shown in Figures 3-15 and 3-16. Selecting the RESET STATS target, followed by selecting the ENTER target, resets the UCN node statistics. When the BACKUP CABLE TST target is selected, followed by selecting the ENTER target on the UCN Statistics display, the selected UCN node will perform a test of the UCN backup cable (the one not currently selected). This will test the selected node's transmitter and the other nodes' receivers on the backup cable. When the TEST/SEL CABLE A or TEST/SEL CABLE B target is selected, followed by the ENTER command, the selected NIM will execute the Backup Cable test unless double cable faults are present. In this case, it will direct the NIM to recover the view to all nodes on the selected cable if possible. This assumes that the cable selected has been repaired.

Continued on next page

UCN CABLE STATUS targets, continued

Table 3-7 UCN Status Display – UCN CABLE STATUS Target Selected, Continued

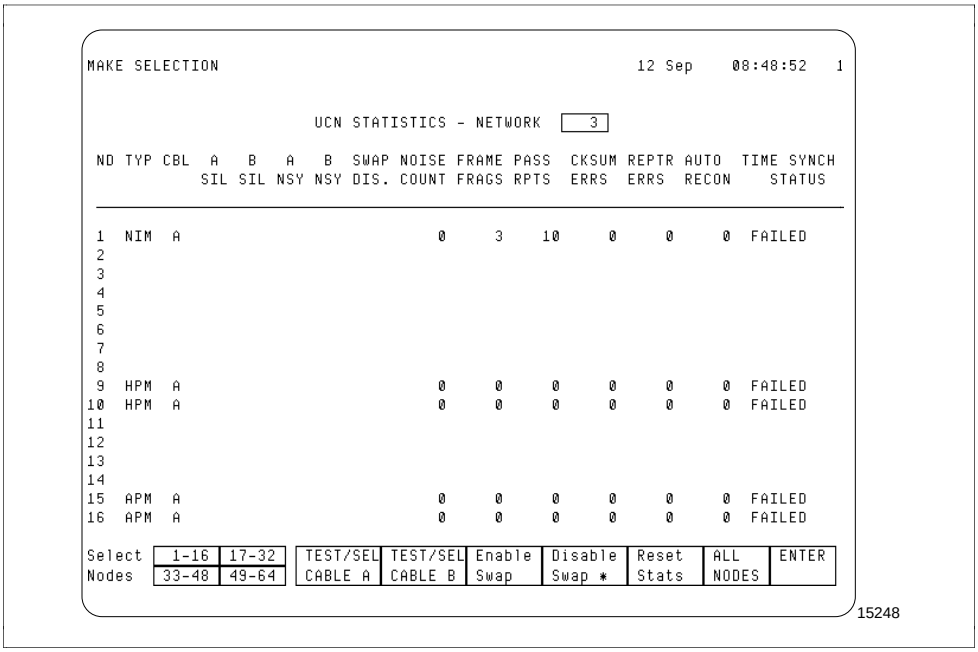
Target	Function
ALL NODES	Enables all UCN nodes to be affected by the cable function.
CANCEL	Clears the BACKUP CABLE TST, TEST/SEL CABLE A, TEST/SEL CABLE B, ENABLE SWAP, DISABLE SWAP, UCN COMM STATUS, ALL NODES, and ENTER command targets from the display.
ENTER	The ENTER target must be selected for the chosen UCN CABLE STATUS function to be executed.

Continued on next page

3.4.1.4 UCN CABLE STATUS Target, Continued

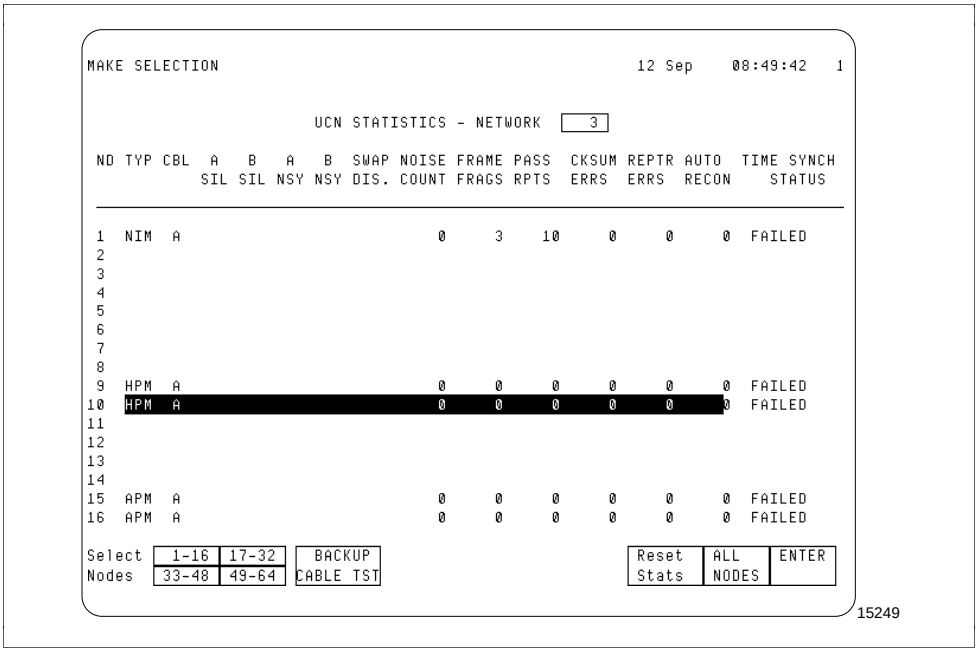
UCN Network Statistics display

Figure 3-15 UCN Network Statistics Display



UCN Network Statistics display with UCN node chosen

Figure 3-16 UCN Network Statistics Display – UCN Node Selected



Continued on next page

3.4.1.4 UCN CABLE STATUS Target, Continued

UCN Network Statistics display definitions

The information in the UCN Network Statistics display is defined in Table 3-8.

Table 3-8 UCN Network Statistics Display Definitions

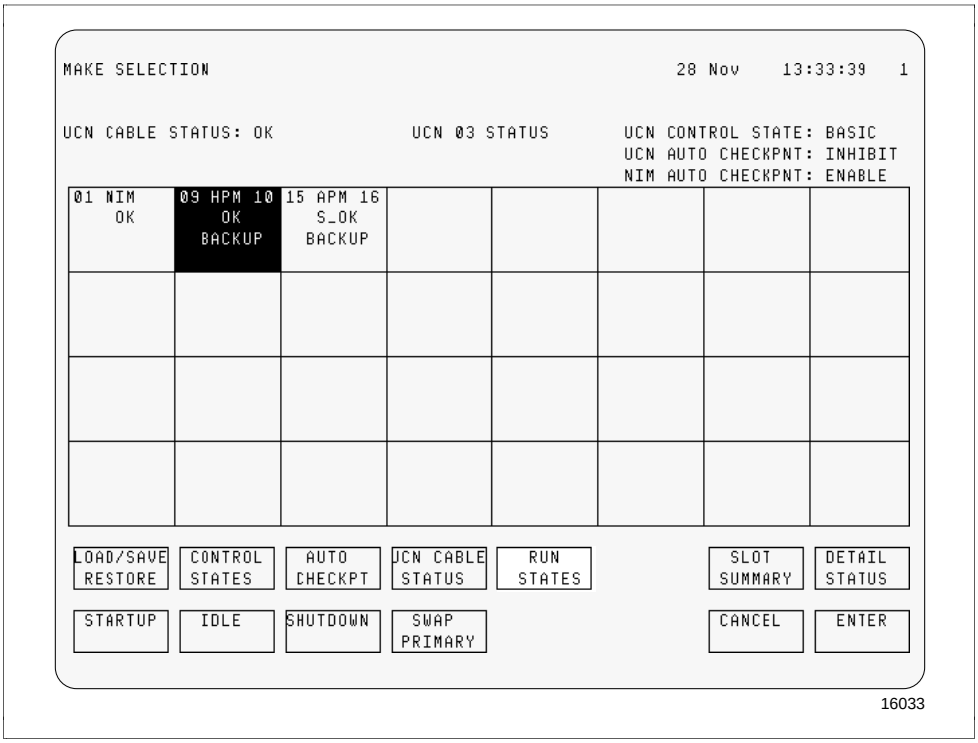
Term	Definition
ND	The node number.
TYP	The hardware type of node (NIM, LM, HPM, APM, or PM).
CBL	The active UCN cable (A or B).
A SIL	An asterisk indicates the node detected a silence event for Cable A.
B SIL	An asterisk (*) indicates the node detected a silence event for Cable B.
A NSY	An asterisk (*) indicates the node detected a noise event for Cable A.
B NSY	An asterisk (*) indicates the node detected a noise event for Cable B.
SWAP DIS	An asterisk (*) indicates that UCN cable auto-swap is disabled (partial frame with missing start delimiter).
NOISE COUNT	The total number of times the node detected a noise event (partial frame with missing end delimiter).
FRAME FRAGS	The total number of times the node detected frame fragments.
PASS RPTS	The total number of times the node retried a token pass to a successor node.
CKSUM ERRS	The total number of times the node detected a checksum error.
REPTR ERRS	The total number of times the node detected a repeater error.
AUTO RECON	The total number of times the node attempted auto reconnect.
TIME SYNCH STATUS	The status of the node's Time Synch. (INITIAL, FAILED, DEGRADED, LCN BAD, LCN OK, or OK)

3.4.1.5 RUN STATES Target

RUN STATES target display

Selection of the **RUN STATES** command target on the UCN Status display as shown in Figure 3-17 invokes additional targets at the bottom of the display to startup or idle the chosen UCN device.

Figure 3-17 UCN Status Display – RUN STATES Target Selected



Not applicable for NIM

The RUN STATES target functions are not applicable when a NIM is chosen on the UCN Status display.

Continued on next page

3.4.1.5 RUN STATES Target, Continued

RUN STATES display targets

The command targets at the bottom of the display in Figure 3-17 perform the functions defined in Table 3-9.

Table 3-9 UCN Status Display – RUN STATES Target Selected

Target	Function
STARTUP	Provides COLD and WARM STARTUP targets for starting the HPM on the UCN that was chosen by its status box. Changes the HPM chosen and all the IOPs that have a valid database from the Idle state to the OK state. The HPM will then begin processing data. The command is executed by selecting the ENTER target.
IDLE	The HPM is placed in a state where its microprocessor is running, but the HPM is not controlling the process. The HPM and all IOPs are set to the Idle state. The command is executed by selecting the ENTER target.
SHUTDOWN	Changes the chosen HPM from the Idle state to the Alive state. To place the HPM back in service after SHUTDOWN, its program and database must be reloaded using the LOAD/SAVE RESTORE target. The command is executed by selecting the ENTER target.
RECOVER	The RECOVER target replaces the SHUTDOWN target when the HPM indicates a fail status. Selecting the RECOVER target executes a SHUTDOWN command that results in the HPM recovering automatically, if possible, or entering the Alive state. The Alive state is the state from which an operator would initiate a reload and the eventual recovery.
SWAP PRIMARY	Swaps HPMMs in the chosen HPM. The present primary HPMM becomes the secondary HPMM. The command is executed by selecting the ENTER target.
CANCEL	Clears the STARTUP, IDLE, SHUTDOWN, SWAP PRIMARY, and ENTER command targets from the display.
ENTER	The ENTER target must be selected for the chosen RUN STATES function to be executed.

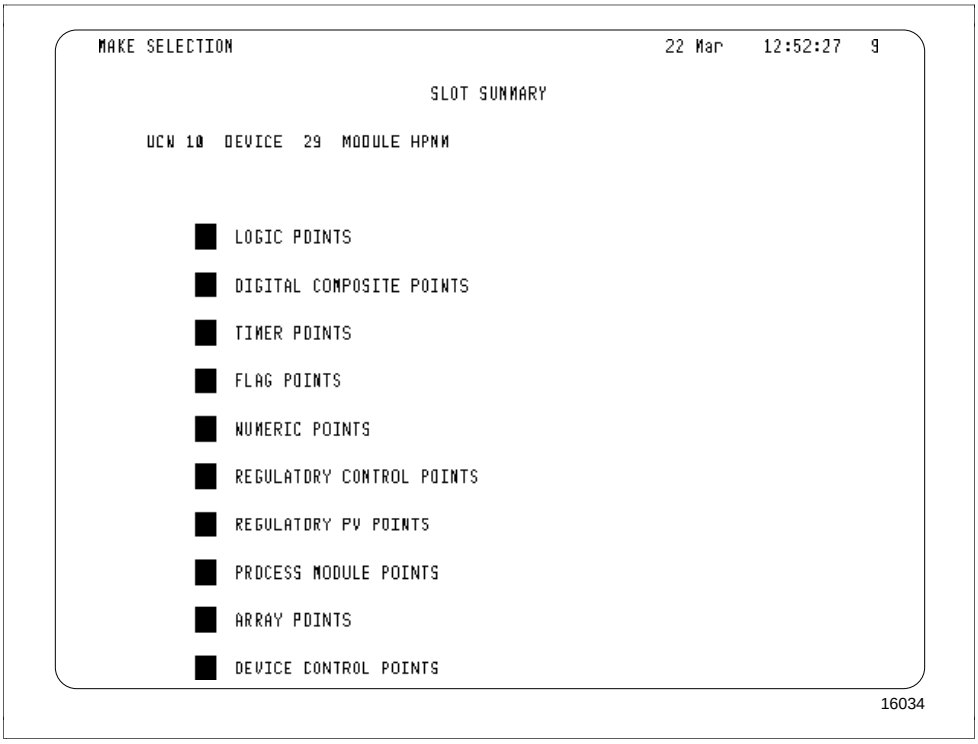
3.4.1.6 SLOT SUMMARY Target

SLOT SUMMARY target

Selection of the **SLOT SUMMARY** command target on the UCN Status display as shown in Figure 3-18 invokes the Slot Summary Menu display as shown in Figure 3-18. The point type of interest is selected on the display. The selection provides a Slot Summary display for the point type that displays the contents (point ID, descriptor, and active/inactive state) in the chosen HPM.

Choose the HPM of interest on the UCN Status display selection grid and then select the **SLOT SUMMARY** target.

Figure 3-18 UCN Status Display – SLOT SUMMARY Target Selected



Not applicable for NIM

The SLOT SUMMARY target functions are not applicable when a NIM is chosen on the UCN Status display.

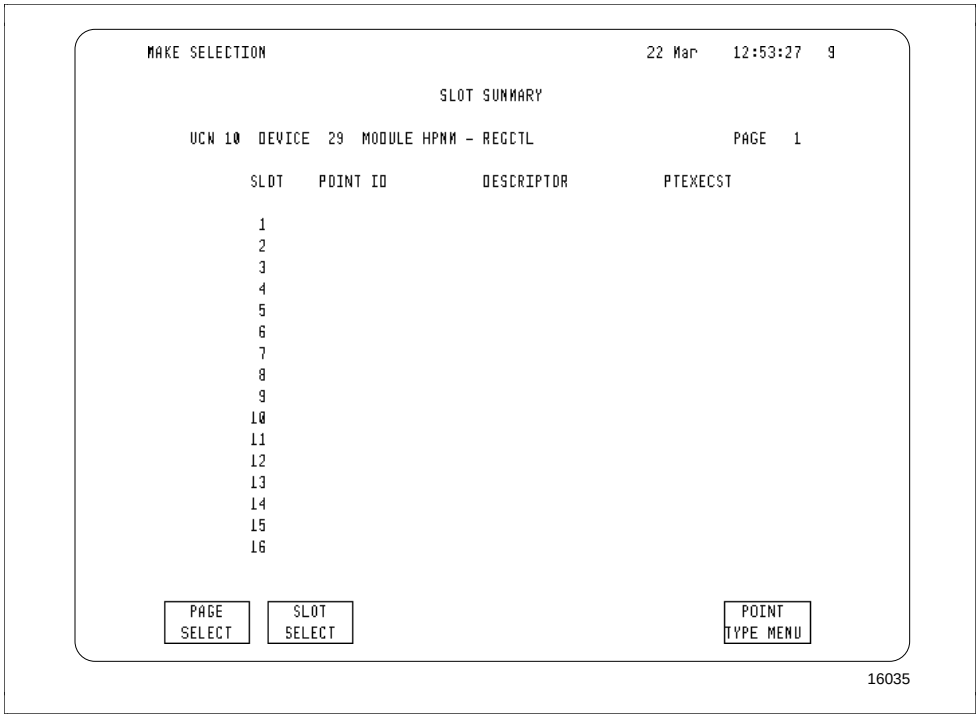
Continued on next page

3.4.1.6 SLOT SUMMARY Target, Continued

REGULATORY CONTROL POINTS target

An example of this is the Process Module Points display as shown in Figure 3-19. Selecting the **REGULATORY CONTROL POINTS** target on the Slot Summary Menu display invokes the display. The Slot Summary display provides access to commands that active/deactivate slots.

Figure 3-19 UCN Status Display – REGULATORY CONTROL POINTS Target Selected



Process Module Points display targets

Three targets are available on the Process Module Points display.

- Selecting the **PAGE SELECT** target produces a **ENTER PAGE NUMBER** response. Enter the page number of interest.
- Selecting the **SLOT SELECT** target produces a **ENTER SLOT NUMBER** response. Enter the slot number of interest.
- The **POINT TYPE MENU** target returns you to the Slot Summary Menu display.

3.4.1.7 DETAIL STATUS Target

DETAIL STATUS target

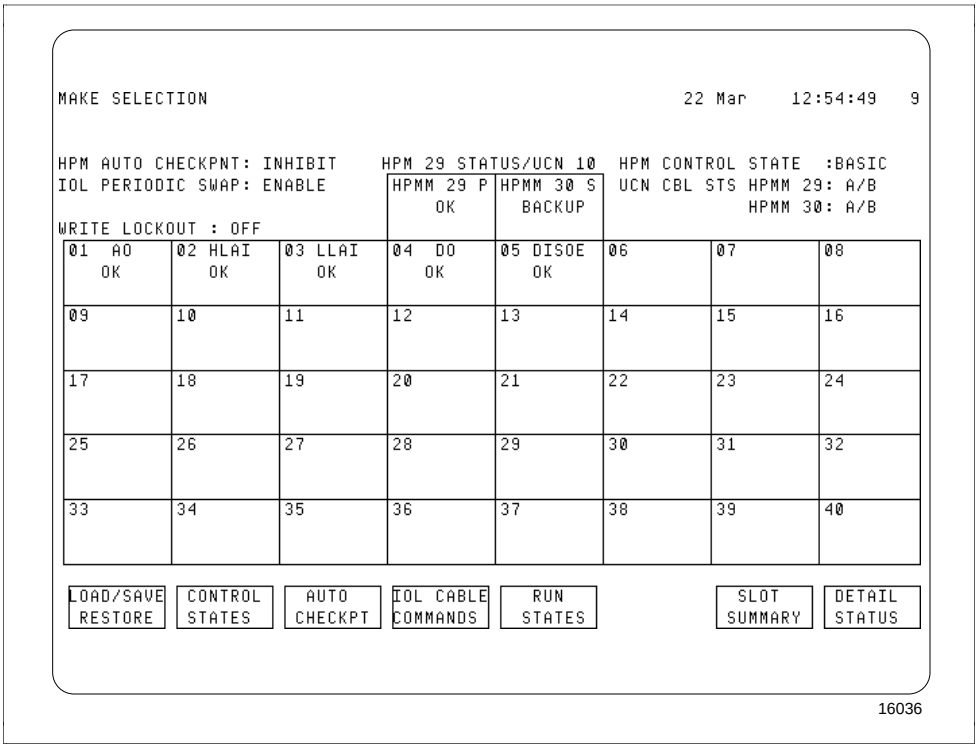
Selection of the **DETAIL STATUS** command target on the UCN Status display invokes either the NIM Detail Status display as shown in Figure 3-3 or the HPM Status display as shown in Figure 3-4.

3.4.2 HPM Status Displays

HPM Status display

The HPM Status display is shown in Figure 3-20. The display is obtained by selecting the <**SYST STATS**> (System Status) key on the console and then selecting the **PROCESS NETWORK STATUS** target on the display for the network you wish to examine. Choose the High-Performance Process Manager associated with the HPMM to be displayed. Select the **DETAIL STATUS** target to obtain the HPMM Status display.

Figure 3-20 HPM Status Display



Three display sections

The display is divided into three sections.

Continued on next page

Top section of display

The top section of the display provides information about the UCN and High-Performance Process Manager.

The UCN and HPM status at the top of the display is defined in Table 3-10.

Table 3-10 HPM Status Display – UCN and HPM Status

Term	Definition
HPM AUTO CHECKPNT	Indicates whether automatic Checkpoint storage to the History Module is enabled. (ENABLE or INHIBIT)
IOL PERIODIC SWAP	Indicates whether the I/O Link communications cable selection (cable A or cable B) is swapped periodically. (ENABLE or INHIBIT)
HPM CONTROL STATE	When in the BASIC state, LCN devices, such as the AM or CM, are prohibited from writing to the HPM. If in the FULL state, LCN devices are permitted to write to the HPM, providing the entire UCN is also in the FULL state.
UCN CBL STS	Identifies the HPMM's UCN node and identifies the active and inactive UCN cables, A or B. (B/A or A/B)

Middle section of display

The middle grid-like section of the display provides status information about the primary and secondary (if redundant) HPMMs and IOPs in the High-Performance Process Manager.

Status boxes

There are two HPMM "status boxes" and 40 IOP "status boxes" that represent the 40 possible IOP addresses on the I/O Link (IOL). All "status boxes" are targets and are backlighted a blue color when chosen for execution by the command targets at the bottom of the display.

HPMM status boxes

The HPMM information at the top of the middle grid-like section of the display defines the status of the HPMM. On the status display of a redundant HPMM subsystem, the left "status box" provides the status of the HPMM that is physically located in HPMM card file 1. The right "status box" provides the status of the HPMM that is located in HPMM card file 2.

Primary and secondary HPMMs

In the HPMM status boxes, the letters "P" and "S" identify which HPMM is the primary HPMM and which HPMM is the secondary HPMM, respectively.

Continued on next page

3.4.2 HPM Status Displays, Continued

HPMM node number	The numerals in the status box indicate each HPMM's UCN node address. The odd address is always associated with the primary HPMM.
HPMM operational states	The HPMM can be in various operational states. The status states are defined in Tables 3-11 and 3-12.

Continued on next page

Primary HPMM status

The possible status of the primary HPMM is defined in Table 3-11 with the color of the text indicated.

Table 3-11 HPM Status Display – Primary HPMM Status

Term	Definition
OK (Text color – blue)	Processing in the primary HPMM is in progress.
ALIVE (Text color – yellow)	Power has been applied to the primary HPMM, but no database or personality program has been loaded into the HPMM.
ALIVESF (Text color – yellow)	Power has been applied to the primary HPMM, but no database or personality program has been loaded into the HPMM. One of the powerup diagnostic tests has failed, but the HPMM is still capable of a program load.
IDLE (Text color – yellow)	The database and personality program has been loaded into the primary HPMM, but no processing is in progress.
LOADING (Text color – yellow)	The HPMM is being loaded with its personality program and data.
NOTCONFG (Text color – yellow)	There is no UCN node configured for the HPMM's UCN node address.
POWERON (Text color – yellow)	The HPMM is responding to the UCN but has not performed its self-tests. This is a transitory state that occurs when the HPMM is first powered on.
CONFGMIS (Text color – red)	The configured node type for the HPMM's UCN node address does not match the actual node type.
FAIL (Text color – red)	The HPM has a Hard failure and access to IOP status and data is unavailable. HPM control functions have ceased. Effectively, this is a total failure.
IDLESF (Text color – red)	The HPMM is in the Idle state and has one or more Soft failures.
OFFNET (Text color – red)	The HPMM is not responding on the UCN because 1) it does not exist, 2) power is off, or 3) there is a hardware failure that prohibits a response.
SOFTFAIL (Text color – red)	The HPMM is in the Run state and has one or more Soft failures.

Continued on next page

Secondary HPMM status

The possible status of the secondary HPMM is defined in Table 3-12 with the color of the text indicated.

Table 3-12 HPM Status Display Definitions – Secondary HPMM Status

Term	Definition
BACKUP (Text color – blue)	Processing in the secondary HPMM is in progress and the secondary database is synchronized with the primary database.
BKUP_SF (Text color – blue)	The HPMM is in the Run state, but has a Soft failure.
ALIVE (Text color – yellow)	Power has been applied to the secondary HPMM, but no database or personality program was loaded into the HPMM.
BACKUP (Text color – yellow)	The secondary HPMM is in the Idle state, or its database is not synchronized with the primary HPMM.
BKUP_SF (Text color – yellow)	The HPMM is in the Idle state, but has a Soft failure.

40 IOP status boxes

The IOP information, at the middle grid-like section of the display, defines the status of each IOP. There are 40 status boxes, representing 40 I/O link addresses. Not all status boxes may be occupied.

IOP status box definitions

The numerals in the upper left corner of the status box is the I/O Link address assigned to the IOP. The IOP type is identified in the upper center portion of the status box, such as HLAI or AO. In the center of the status box is the status of the IOP(s). If a slash (/) appears in the status statement, redundant IOPs, A and B respectively, are present.

IOP synchronization status

An “S” to the left of IOP A’s status and to the right of IOP B’s status represents the synchronization status of the redundant IOP pair. The “S” has two backlighting colors, red for **SYNC_FAIL** and yellow for **SYNC_WARNING**. A **SYNC_FAIL** status indicates the IOP has tried several times to synchronize the database between the IOPs with no success. A **SYNC_WARNING** status indicates the IOP is attempting, or will attempt soon, to synchronize the secondary’s database with the primary’s database.

IOP status states

For redundant Analog Output IOPs, IOP A is the preferred (biased) primary IOP.

Continued on next page

IOP A status states

The possible status of IOP A is defined in Table 3-13 with the color of the text indicated.

Table 3-13 HPM Status Display – IOP A Status

Term	Definition
BKP (Text color – blue)	IOP A is currently the secondary IOP and processing in the IOP is in progress.
OK (Text color – blue)	IOP A is currently the primary and processing in the IOP is in progress.
BKP (Text color – yellow)	IOP A is currently the secondary IOP and in the Idle state.
IDL (Text color – yellow)	IOP A is currently the primary IOP, but no processing is in progress.
BSF (Text color – red)	IOP A is currently the secondary IOP and processing is in progress, but a Soft failure has been detected in the IOP.
CFG (Text color – red)	The IOP type that occupies this card slot has a configuration mismatch.
NR (Text color – red)	IOP A is not responding on the I/O Link Interface.
SF (Text color – red)	IOP A is currently the primary IOP and processing is in progress, but a Soft failure has been detected in the IOP.

Continued on next page

IOP B status states

The possible status of IOP B is defined in Table 3-13 with the color of the text indicated.

Table 3-14 HPM Status Display – IOP B Status

Term	Definition
BKP (Text color – blue)	IOP B is currently the secondary IOP and processing in the IOP is in progress.
OK (Text color – blue)	IOP B is currently the primary and processing in the IOP is in progress.
BKP (Text color – yellow)	IOP B is currently the secondary IOP and in the Idle state.
IDL (Text color – yellow)	IOP B is currently the primary IOP, but no processing is in progress.
BSF (Text color – red)	IOP B is currently the secondary IOP and processing is in progress, but a Soft failure has been detected in the IOP.
CFG (Text color – red)	The IOP type that occupies this card slot has a configuration mismatch.
NR (Text color – red)	IOP B is not responding on the I/O Link Interface.
SF (Text color – red)	IOP B is currently the primary IOP and processing is in progress, but a Soft failure has been detected in the IOP.

Command targets

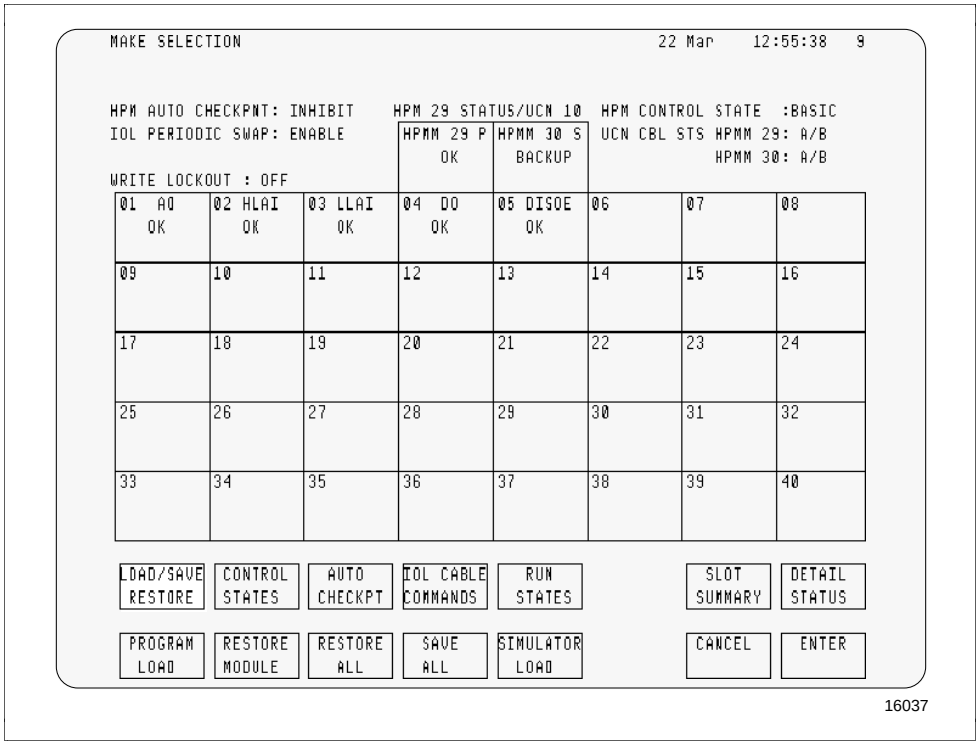
The command targets at the bottom of the display in Figure 3-20 perform the functions defined in the tables that follow.

3.4.2.1 LOAD/SAVE RESTORE Target

LOAD/SAVE RESTORE target

Selection of the **LOAD/SAVE RESTORE** command target on the HPM Status display as shown in Figure 3-21 invokes additional targets at the bottom of the display to either load the personality program, restore the database, or save the database for the HPMM or IOP chosen by its status box.

Figure 3-21 HPM Status Display – LOAD/SAVE RESTORE Target Selected



Continued on next page

3.4.2.1 LOAD/SAVE RESTORE Target, Continued

LOAD/SAVE RESTORE display targets

The command targets at the bottom of the display in Figure 3-21 perform the functions defined in Table 3-15.

Table 3-15 HPM Status Display – LOAD/SAVE RESTORE Target Selected

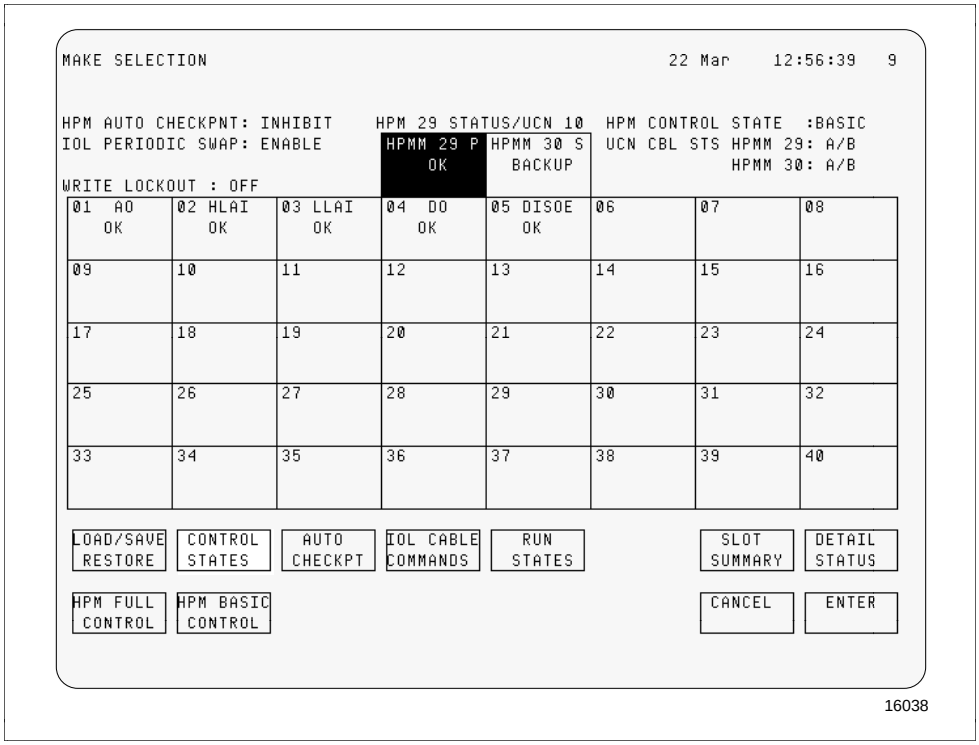
Target	Function
PROGRAM LOAD	Loads the on-process (regular) personality program and the selected database to the chosen HPMM. If the primary HPMM is chosen, the database is also restored in all IOPs that are in the Idle state. The command is executed by selecting the ENTER target.
RESTORE MODULE	Restores the database in the chosen HPMM or IOP. The module must be in the Idle state (not valid for the secondary HPMM). The command is executed by selecting the ENTER target.
RESTORE ALL	Restores the database in the chosen HPMM and all IOPs. The modules must be in the Idle state. The command is executed by selecting the ENTER target.
SAVE ALL	Saves the database from the chosen HPMM and all IOPs into either the History Module or removable media. This is sometimes called “Checkpointing.” The command is executed by selecting the ENTER target.
SIMULATOR LOAD	Loads the I/O Simulator personality and selected database to the chosen HPMM. If the primary HPMM is chosen, the database is also restored in all simulated IOPs that are in the Idle state. The command is executed by selecting the ENTER target.
CANCEL	Clears the PROGRAM LOAD, RESTORE MODULE, RESTORE ALL, SAVE ALL, and ENTER command targets from the display.
ENTER	Executes the LOAD/SAVE RESTORE function command.

3.4.2.2 CONTROL STATES Target

CONTROL STATES target

Selecting the **CONTROL STATES** command target on the HPM Status display as shown in Figure 3-22 invokes additional targets at the bottom of the display to change the control state of the HPMM chosen by its status box.

Figure 3-22 HPM Status Display – CONTROL STATES Target Selected



CONTROL STATES display targets

The command targets at the bottom of the display in Figure 3-22 perform the functions defined in Table 3-16.

Table 3-16 HPM Status Display – CONTROL STATES Target Selected

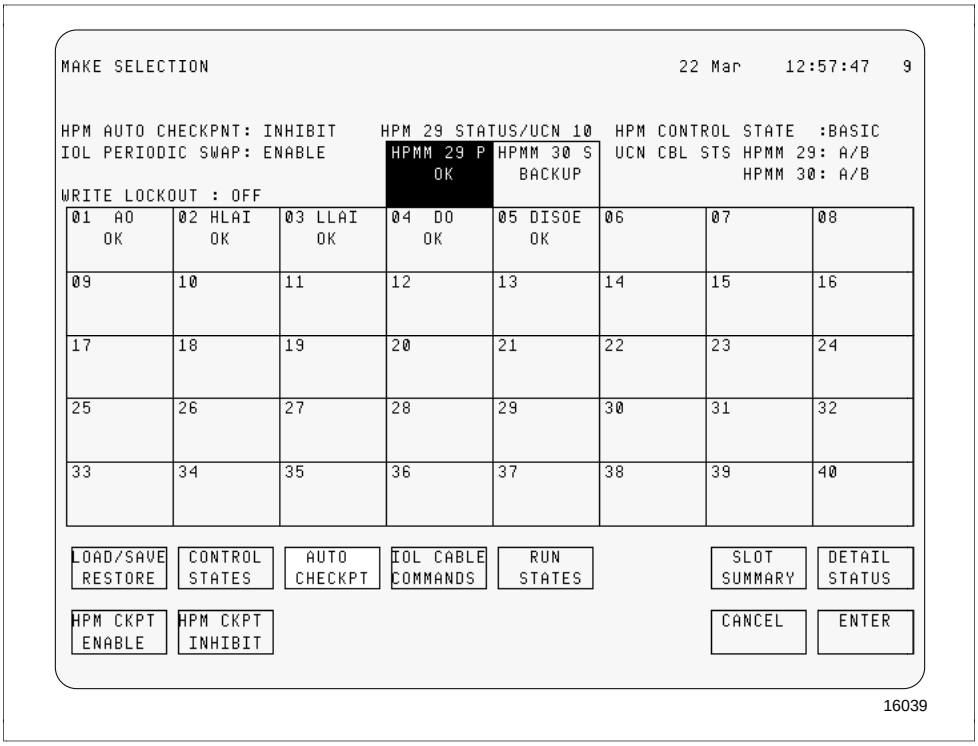
Target	Function
HPM FULL CONTROL	Changes the UCN's control state to FULL. The command is executed by selecting the ENTER target.
HPM BASIC CONTROL	Changes the UCN's control state to BASIC. The command is executed by selecting the ENTER target.
CANCEL	Clears the HPM FULL CONTROL, HPM BASIC CONTROL, and ENTER command targets from the display.
ENTER	Executes the CONTROL STATES function command.

3.4.2.3 AUTO CHECKPT Target

AUTO CHECKPT target

Selection of the **AUTO CHECKPT** command target on the HPM Status display as shown in Figure 3-23 invokes additional targets at the bottom of the display to change the Checkpointing state of the HPM.

Figure 3-23 HPM Status Display – AUTO CHECKPT Target Selected



AUTO CHECKPT display targets

The command targets at the bottom of the display in Figure 3-23 perform the functions defined in Table 3-17.

Table 3-17 HPM Status Display – AUTO CHECKPT Target Selected

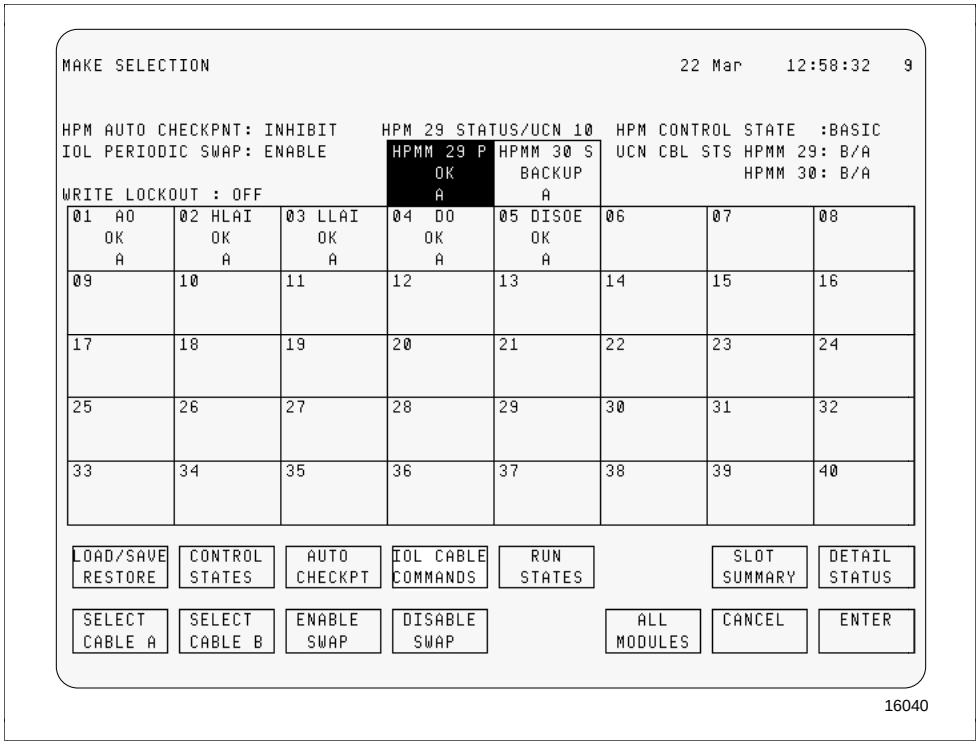
Target	Function
HPM CKPT ENABLE	Enables automatic Checkpointing of the HPM. The command is executed by selecting the ENTER target.
HPM CKPT INHIBIT	Disables automatic Checkpointing of the HPM. The command is executed by selecting the ENTER target.
CANCEL	Clears the HPM CKPT ENABLE, HPM CKPT INHIBIT, and ENTER command targets.
ENTER	Executes the AUTO CHECKPT function command.

3.4.2.4 IOL CABLE COMMANDS Target

IOL CABLE COMMANDS target

Selection of the **IOL CABLE COMMANDS** command target on the HPM Status display as shown in Figure 3-24 invokes additional targets at the bottom of the display to change the selected IOL cable or enable/disable automatic cable swapping.

Figure 3-24 HPM Status Display – IOL CABLE COMMANDS Target Selected



Continued on next page

3.4.2.4 IOL CABLE COMMANDS Target, Continued

IOL CABLE COMMANDS display targets

The command targets at the bottom of the display in Figure 3-24 perform the functions defined in Table 3-18.

Table 3-18 HPM Status Display – IOL CABLE COMMANDS

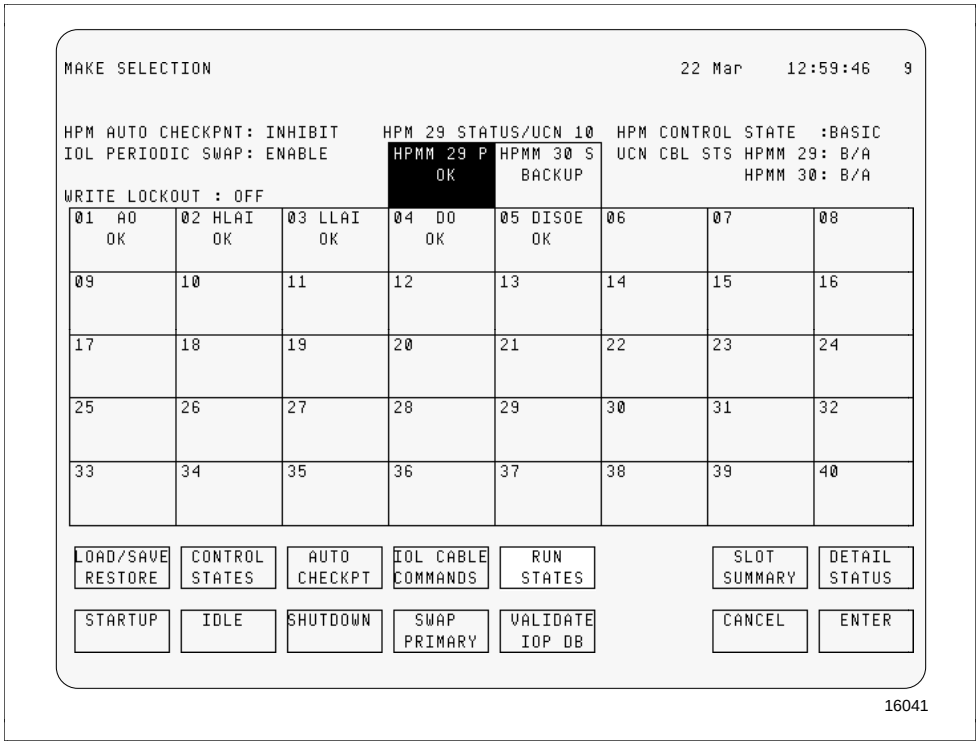
Target	Function
SELECT CABLE A	Activates I/O Link (IOL) cable A. The command is executed by selecting the ENTER target.
SELECT CABLE B	Activates I/O Link (IOL) cable B. The command is executed by selecting the ENTER target.
ENABLE SWAP	Enables periodic swapping of the I/O Link cables. The command is executed by selecting the ENTER target.
DISABLE SWAP	Disables periodic swapping of the I/O Link cables. The command is executed by selecting the ENTER target.
ALL MODULES	Allows both HPMMs and all IOPs to be affected by the cable function command. The command is executed by selecting the ENTER target.
CANCEL	Clears the SELECT CABLE A, SELECT CABLE B, ENABLE SWAP, DISABLE SWAP, ALL MODULES, and ENTER command targets from the display.
ENTER	The ENTER target must be selected for the chosen IOL CABLE COMMANDS function to be executed.

3.4.2.5 RUN STATES Target

RUN STATES target

Selection of the **RUN STATES** command target on the HPM Status display as shown in Figure 3-25 invokes additional targets at the bottom of the display to **STARTUP**, **SHUTDOWN**, **IDLE** or **SWAP** the chosen HPMM or IOP.

Figure 3-25 HPM Status Display – RUN STATES Target Selected



Continued on next page

3.4.2.5 RUN STATES Target, Continued

RUN STATES display targets

The command targets at the bottom of the display in Figure 3-25 perform the functions defined in Table 3-19.

Table 3-19 HPM Status Display – RUN STATES Target Selected

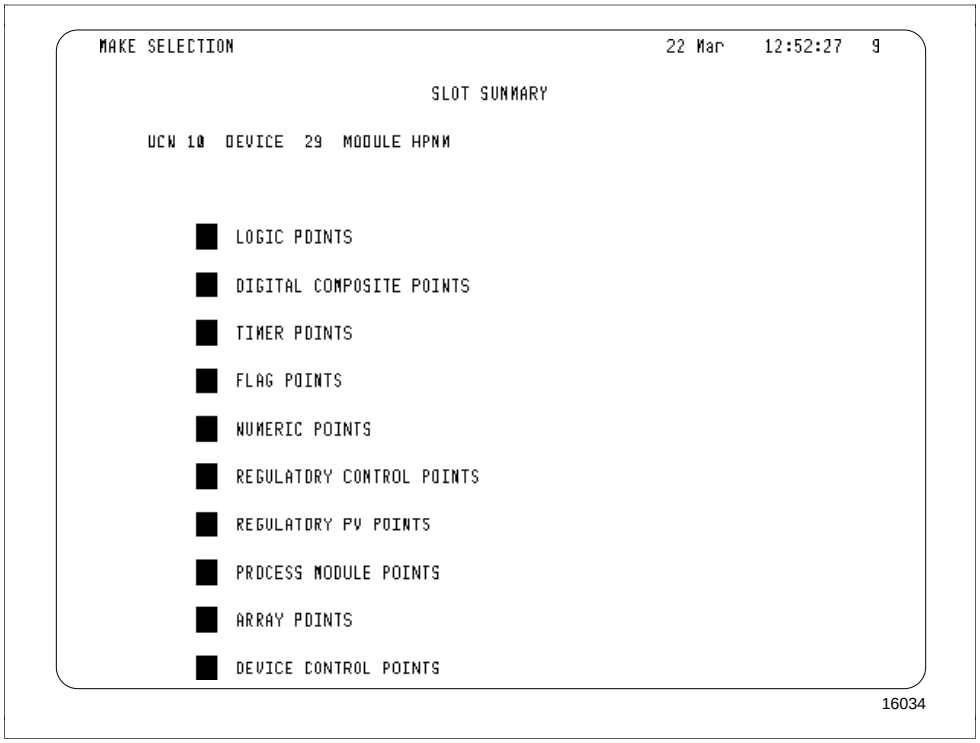
Target	Function
STARTUP	Provides COLD and WARM STARTUP targets for starting the HPMM or IOP that was chosen by its status box. Changes the HPMM or IOP chosen from the Idle state to the OK state if it has a valid database, which is indicated. The HPMM or IOP will then begin processing data. The command is executed by selecting the ENTER target.
IDLE	The chosen HPMM or IOP is changed from the OK state to the Idle state. The command is executed by selecting the ENTER target.
SHUTDOWN	Changes the chosen HPMM from the Idle or Fail state to the Alive or OK state, respectively. To place the HPMM back in service after Shutdown, its personality program and database must be reloaded using the LOAD/SAVE RESTORE target. The command is executed by selecting the ENTER target.
SWAP PRIMARY	Swaps the chosen HPMMs or redundant IOPs. The present primary HPMM or IOP becomes the secondary HPMM or IOP, respectively. The command is executed by selecting the ENTER target.
VALIDATE IOP DB	Accepts the existing database for the chosen IOP as the valid database. The command is executed by selecting the ENTER target.
ALL MODULES	Allows all HPMMs and IOPs to be affected by the STARTUP or IDLE target.
CANCEL	Clears the STARTUP, IDLE, SHUTDOWN, SWAP PRIMARY, VALIDATE IOP DB, ALL MODULES, and ENTER command targets from the display.
ENTER	The ENTER target must be selected for the chosen RUN STATES function to be executed.

3.4.2.6 SLOT SUMMARY Target

SLOT SUMMARY target

Selection of the **SLOT SUMMARY** command target on the HPM Status display as shown in Figure 3-26 invokes the Slot Summary Menu display from which the point type of interest for the chosen HPMM or IOP is selected. The selection provides a Slot Summary display for the point type that displays the contents (point ID, descriptor, and active/inactive state) of the HPMM or IOP that is chosen.

Figure 3-26 HPM Status Display – SLOT SUMMARY Target Selected



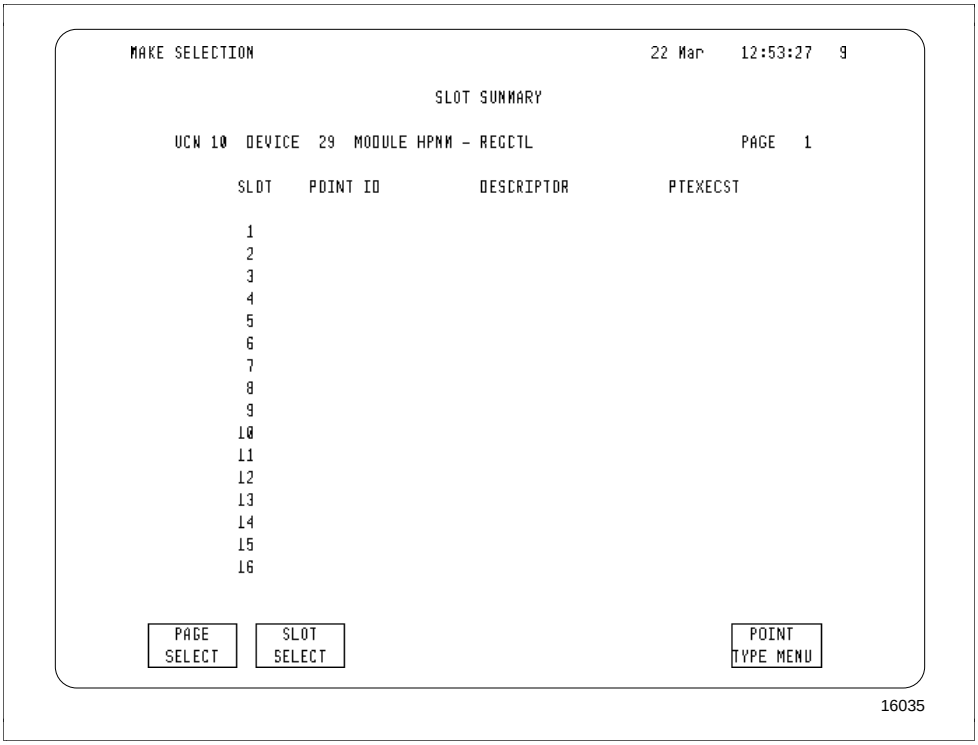
Continued on next page

3.4.2.6 SLOT SUMMARY Target, Continued

REGULATORY CONTROL POINTS target

An example of this is the Process Module Points display as shown in Figure 3-27. Selecting the **REGULATORY CONTROL POINTS** target on the Slot Summary Menu display invokes the display. The Slot Summary display provides access to commands that active/deactivate slots.

Figure 3-27 HPM Status Display – REGULATORY CONTROL POINTS Target Selected



Process Module Points display targets

Three targets are available on the Process Module Points display.

- Selecting the **PAGE SELECT** target produces a **ENTER PAGE NUMBER** response. Enter the page number of interest.
- Selecting the **SLOT SELECT** target produces a **ENTER SLOT NUMBER** response. Enter the slot number of interest.
- The **POINT TYPE MENU** target returns you to the Slot Summary Menu display.

3.4.2.7 DETAIL STATUS Target

DETAIL STATUS target

Selection of the **DETAIL STATUS** command target on the HPM Status display invokes the Detail Status display of the chosen HPMM or IOP as shown in Figures 3-31, 3-32, or 3-54.

3.4.3 NIM Detail Status Displays

Selection procedure

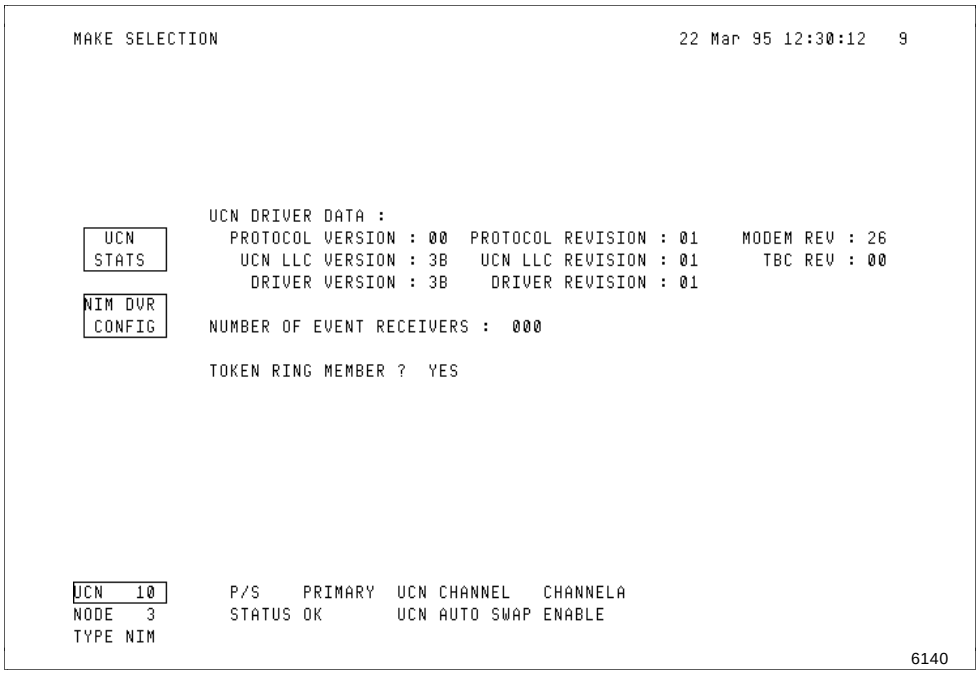
The NIM Detail Status displays consist of two displays, the NIM Driver Configuration display and the NIM Local UCN Statistics display. The initial NIM Detail Status display, which is the NIM Driver Configuration display, is selected by invoking the UCN Status display, choosing the NIM of interest on the display grid, and then selecting the **DETAIL STATUS** target.

The NIM Driver Configuration display can also be invoked by selecting the **NIM DVR CONFIG** target on the NIM Local UCN Statistics display.

NIM Driver Configuration display

The NIM Driver Configuration display is shown in Figure 3-28.

Figure 3-28 NIM Driver Configuration Display



Continued on next page

NIM Driver Configuration display status

Table 3-20 defines the information in the NIM Driver Configuration display.

Table 3-20 NIM Driver Configuration Display Status

Term	Description
PROTOCOL VERSION	The version of the UCN Communications protocol which exists in the NIM UCN Communications Driver.
PROTOCOL REVISION	The revision of the UCN Communications protocol which exists in the NIM UCN Communications Driver.
UCN LLC VERSION	The version of the Logical Link Control layer which exists in the UCN.
UCN LLC REVISION	The revision of the Logical Link Control layer which exists in the UCN.
DRIVER VERSION	The version of the UCN Communications Driver in the NIM.
DRIVER REVISION	The revision of the UCN Communications Driver in the NIM.
NUMBER OF EVENT RECEIVERS	The number of event receivers currently recognized by the UCN Driver.
TOKEN RING NUMBER ?	Is the NIM currently in the UCN token ring? (YES or NO) There are four possible messages that can appear under the TOKEN RING NUMBER ? text. They are: CHANNEL A ABANDONED DUE TO SILENCE CHANNEL B ABANDONED DUE TO SILENCE CHANNEL A ABANDONED DUE TO NOISE CHANNEL B ABANDONED DUE TO NOISE The CHANNEL A and CHANNEL B messages are exclusive to each other.
MODEM REV	The revision of the NIM UCN Communications Driver
TBC REV	The revision of the Token Bus Controller

Continued on next page

3.4.3 NIM Detail Status Displays, Continued

UCN Driver statistics (UCN STATS target)

The NIM maintains a set of UCN Driver statistics that are used to evaluate the condition of the UCN as seen by the NIM. These statistics are requested by selection of the **UCN STATS** target. The statistics are presented in the two pages of the NIM Local UCN Statistics display as shown in Figures 3-29 and 3-30.

NIM and HPMM display differences

The Local UCN Statistics displays for the NIM and HPMM are similar. The HPMM Local UCN Statistics displays are shown in Figures 3-29 and 3-30. The NIM and HPMM Local UCN Statistics displays have the following differences.

- The targets available on the displays are slightly different.
- The HPMM Local UCN Statistics display has a **FILE POS** status.
- The **TYPE** status is different (**HPM** or **NIM**).
- Only the NIM Local UCN Statistics display has Event Receiver statistics.
- The Event Sender statistics error counts on the NIM Local UCN Statistics display are always zero.
- Only the HPMM Local UCN Statistics display has Performance statistics.

Page statistical and status content

Page 1 displays the local statistics for the UCN node, NIM or HPMM, while Page 2 displays UCN Event Sender statistics (HPMM only), UCN Event Receiver statistics (UCN only), Performance statistics (HPMM only), Time Synch status (NIM or HPMM), and Time Synch statistics (NIM or HPMM).

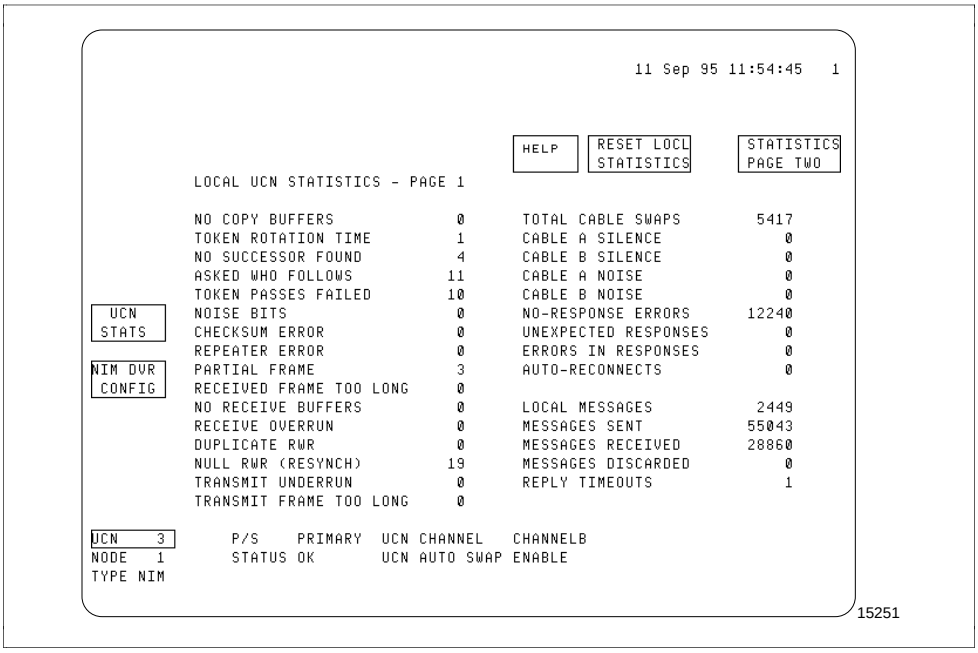
Switching display pages

You can switch between the Page 1 and Page 2 displays by alternately selecting the **STATISTICS PAGE TWO** target on the Page 1 display and the **STATISTICS PAGE ONE** target on the Page 2 display.

Continued on next page

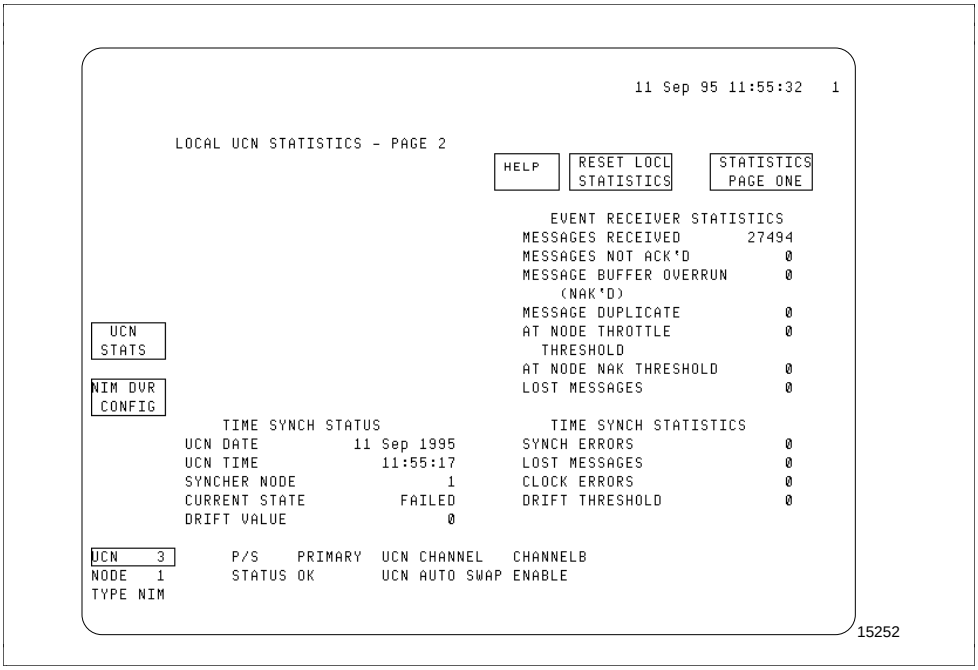
NIM Local UCN Statistics display-page 1

Figure 3-29 NIM Local UCN Statistics Display – Page 1



NIM Local UCN Statistics display-page 2

Figure 3-30 NIM Local UCN Statistics Display – Page 2



Continued on next page

Two pages

The **STATISTICS PAGE TWO** target on the first page display is used to request the second page of statistics. The first page is chosen by selecting the **STATISTICS PAGE ONE** target on the second page display. The **RESET LOCL STATISTICS** target on either page is used to reset the values of all the statistics to zero for diagnostic purposes, not just those on the page being displayed.

Cable noise/silence

Not shown in the figures is a group of four messages pertaining to the detection of noise/silence on the UCN cables. These messages, which appear immediately above the **LOCAL UCN STATISTICS - PAGE 1** or **PAGE 2** heading, can be any combination of the following texts:

- **CABLE A NOISE**
- **CABLE B NOISE**
- **CABLE A SILENCE**
- **CABLE B SILENCE**

Time Sync operation

Normal Time Synch operation is for the Synchronizer NIM, the lowest-address NIM that has an EPNI board and the best LCN clock status, to send a hardware recognized Time Synch message, followed by a matching synchtime message containing the exact time of the Time Synch message transmission. This is done at nominal 6 second intervals.

Four second update

The statistics and messages are updated every four seconds.

HELP target

Refer to Figures 3-29 and 3-30.

The **HELP** target is used to gain greater insight into each statistical entry on the 2-page Local UCN Statistics display. To use it, you simply select the individual entry that you would like more information about, and then select the **HELP** target. The resultant display provides the following information about the statistical entry you selected.

- Description
- Normal Value
- How the system recovers from the failure
- Probable cause of the failure
- Reference to other statistics for correlation

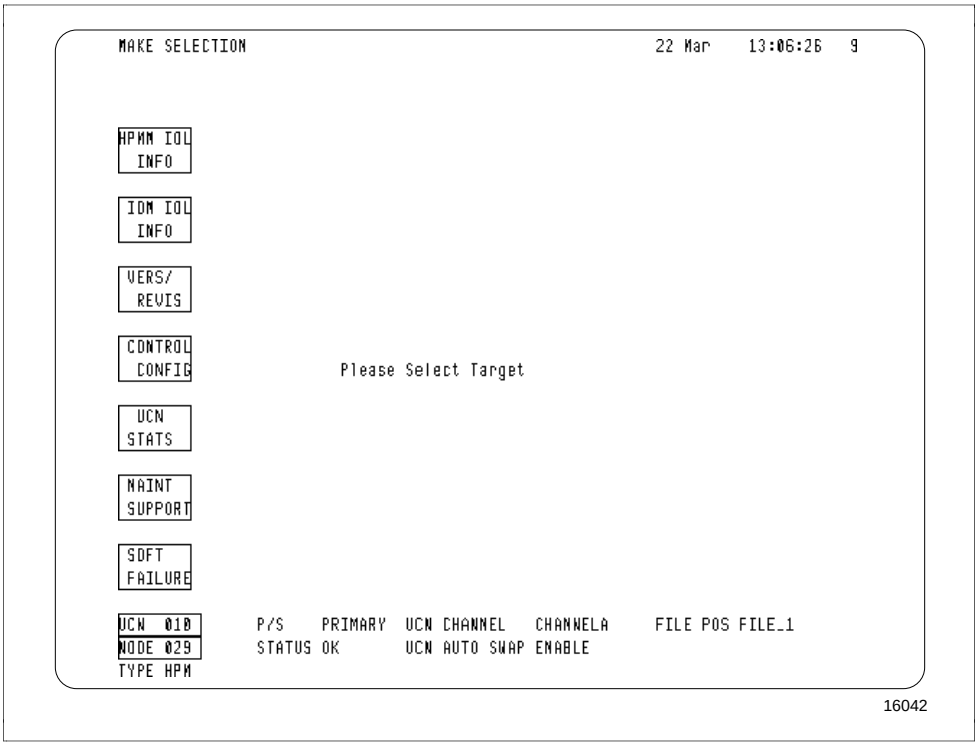
3.4.4 HPMM Detail Status Displays

HPMM Detail Status display selection

The Primary and Secondary HPMM Detail Status displays are shown in Figures 3-31 and 3-32. The primary or secondary display is obtained by choosing the HPM of interest on the UCN Status display, selecting the **DETAIL STATUS** target, choosing the primary or secondary HPMM, and then selecting the **DETAIL STATUS** target.

Primary HPMM Detail Status display

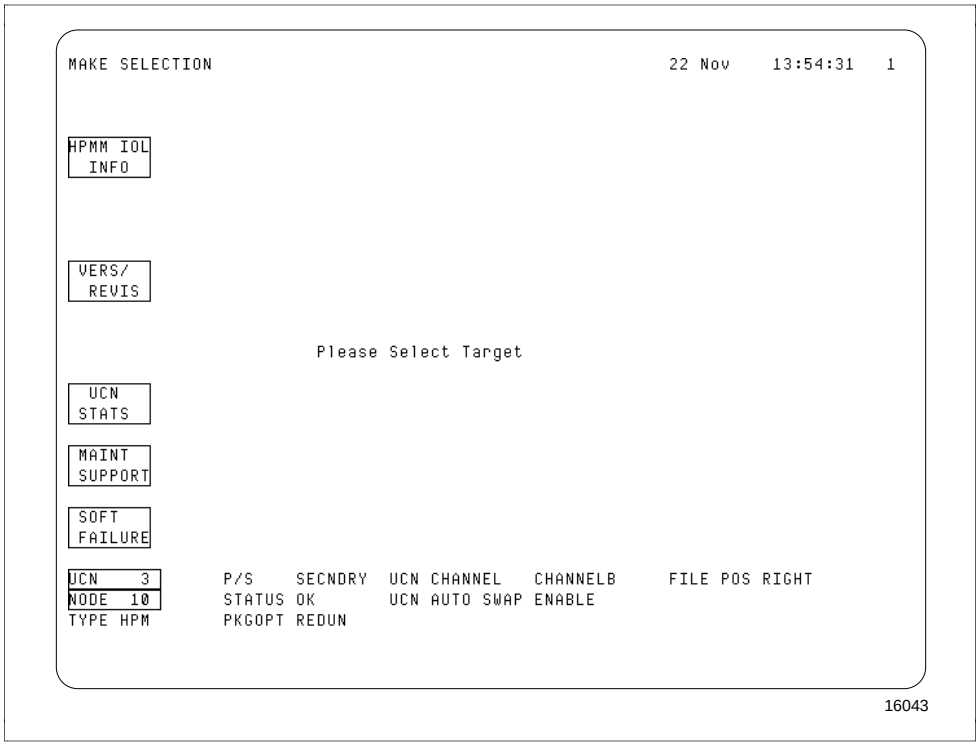
Figure 3-31 Primary HPMM Detail Status Display



Continued on next page

Secondary HPMM Detail Status display

Figure 3-32 Secondary HPMM Detail Status Display



Targets and bottom data fields

The data fields at the bottom of the display and the targets at the left side of the display remain as long as the display is on the console screen.

Continued on next page

Bottom data fields defined

The data at the bottom of the display is defined in Table 3-21.

Table 3-21 HPMM Detail Status Display

Term	Description
UCN	The UCN number
NODE	The node number on the UCN
TYPE	The node type (NIM or HPM)
P/S	The node's current redundancy status (PRIMARY, SECNDRY, or NONREDUN)
STATUS	The current composite status of the node. This is the same as the composite status displayed on the UCN Status display. See the *High-Performance Process Manager Process Operations Manual Process Operations Manual* for responses.
PKGOPT	The configured hardware packaging of the HPMM. REDUN = Nonredundant and redundant 7-Slot HPMM card files REDUN_2F = Nonredundant and redundant 15-Slot HPMM card files
UCN CHANNEL	Current UCN cable active (CHANNEL A or CHANNEL B).
UCN AUTO SWAP	The current UCN cable auto swap status (ENABLE or DISABLE).
FILE POS	The HPMM node's assigned position in the HPM. RIGHT = Right 7-Slot card file LEFT = Left 7-Slot card file FILE_1 = Primary (lower) 15-Slot card file FILE_2 = Secondary (upper) 15-Slot card file.

Four-second update

With the exception of **UCN**, **NODE**, and **TYPE**, the data at the bottom of the display is updated every four seconds.

Target comparison

The targets at the left side of the display are dependent on the node's redundancy status as illustrated by comparison of Figures 3-31 and 3-32. Except for the HPMM I/O Information display, the information selected by the set of secondary HPMM targets is identical to those selected by the corresponding target for a primary HPMM.

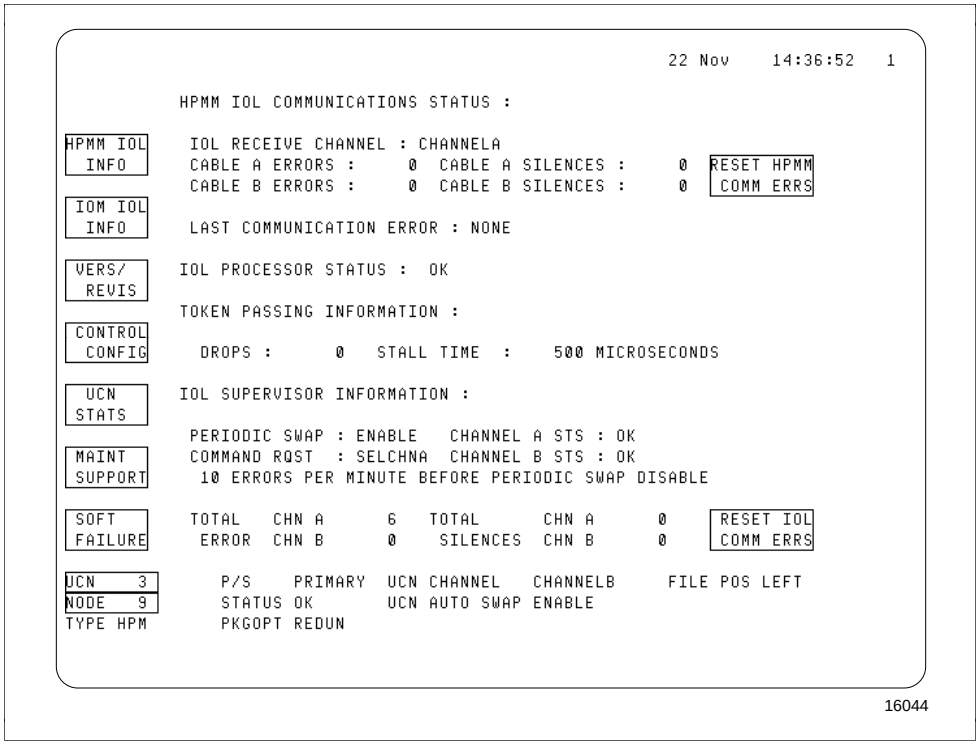
3.4.4.1 HPMM I/O Link Information Displays

HPMM I/O Link Information display

Selection of the **HPMM IOL INFO** target on the HPMM Detail Status display invokes the I/O Link Information display as shown in Figure 3-33. The current status of the HPMM as a node on the I/O Link is displayed, and for the Primary HPMM, it also displays the status of the entire I/O Link as seen by the HPMM Communications processor's I/O Link Supervisor function. As shown in Figure 3-34, only the top portion of the display, the status of the HPMM as a I/O Link address, is displayed for the Secondary HPMM.

Primary HPMM I/O Link Information display

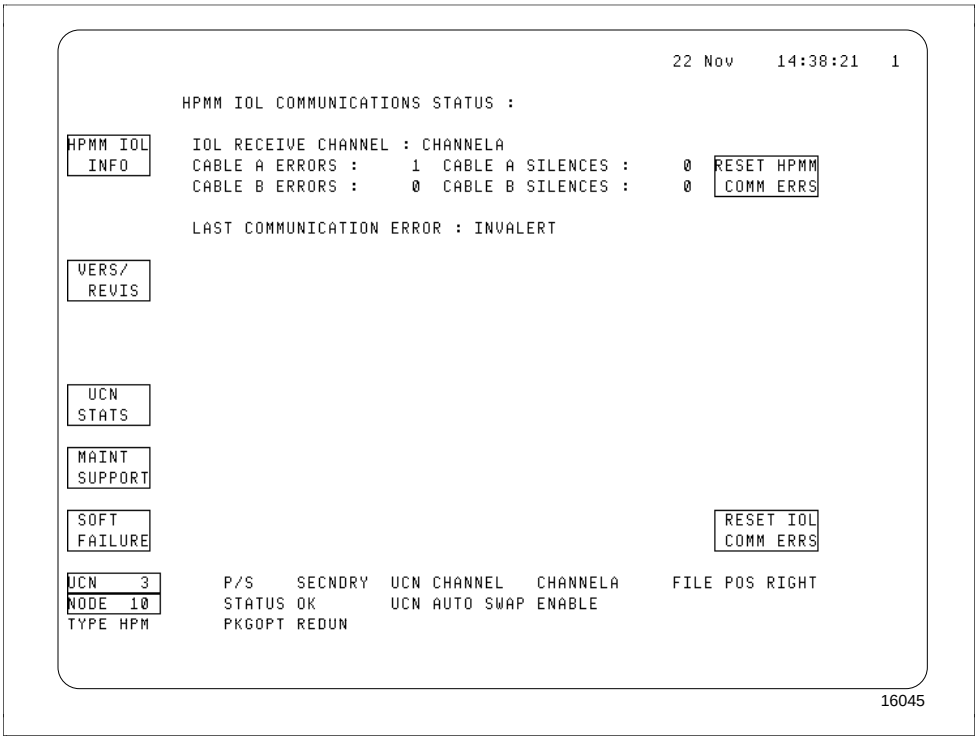
Figure 3-33 Primary HPMM I/O Link Information Display



Continued on next page

Secondary HPMM I/O Link Information display

Figure 3-34 Secondary HPMM I/O Link Information Display



Continued on next page

Four -second update

With the exception of the **STALL TIME** and the allowed number of errors before the periodic UCN cable swap is disabled (see below), the data in the display is updated every four seconds.

HPMM I/O Link status

The status of the HPMM as an I/O Link node is defined in Table 3-22.

Table 3-22 HPMM I/O Link Information Display

Term	Description
IOL RECEIVE CHANNEL	The current I/O Link receive channel (CHANNEL A or CHANNEL B) for the HPMM.
CABLE A ERRORS **CABLE B ERRORS** **CABLE A SILENCES** **CABLE B SILENCES**	Running totals are displayed of the errors/silences detected for each I/O Link cable Interface since the startup of the HPMM or the last reset of the error data. For diagnostic purposes, these totals can be reset to zero by selection of the RESET HPMM COMM ERRS target.
LAST COMMUNICATION ERROR	The last I/O Link error detected by the HPMM. This error is set to NONE by selection of the RESET HPMM COMM ERRS target.
IOL PROCESSOR STATUS	The current status of the I/O Link processor (OK or ERROR).
TOKEN PASSING INFORMATION	DROPS The number of token drops detected by the I/O Link processor. STALL TIME The token stall time (fixed) in microseconds (xxx MICROSECONDS).

Continued on next page

HPMM II/O Link status, continued

Table 3-22 HPMM I/O Link Information Display, Continued

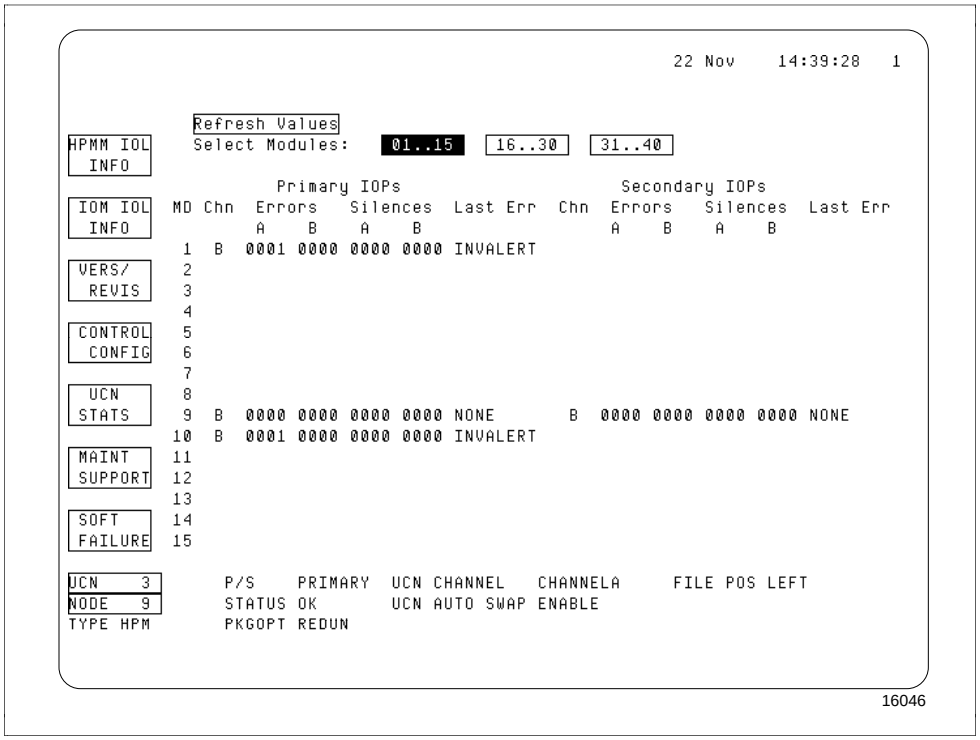
Term	Description	
IOL SUPERVISOR INFORMATION	PERIODIC SWAP	The Enable/Disable status of the periodic swap function (ENABLE or DISABLE).
	COMMAND RQST	A display of the last command executed by the IOS to itself and/or the IOPs.
	CHANNEL A STS	The current condition of the A I/O Link channel (OK or ERROR).
	CHANNEL B STS	The current condition of the A I/O Link channel (OK or ERROR).
	XXX ERRORS PER MINUTE BEFORE PERIODIC SWAP DISABLE	Periodic I/O Link cable swapping will be disabled when the “before periodic swap” number of errors detected on either I/O Link cable exceeds the displayed value. The value is fixed in the I/O Link Driver.
	TOTAL ERROR CHN A CHN B TOTAL SILENCE CHN A CHN B	Displays the total number of errors and silences detected by the IOS for both I/O Link cables for all IOPs and the HPMM. The values in these fields should be the sum of the values given in the IOP I/O Link Information display and the errors shown at the top of this display. The values shown can be reset to zero by selection of the RESET IOL COMM ERRS target. Selection of the target resets the communications errors/silences totals in each of the IOPs, and also resets the current I/O Link errors (LAST ERR) to NONE.

3.4.4.2 IOM I/O Link Information Displays

HPMM IOM I/O Link Information display

The target that produces the HPMM IOM I/O Link Information display and the accompanying three displays is available only for the primary HPMM. One of the three displays is shown in Figure 3-35.

Figure 3-35 IOM I/O Link Information Display



Data tables

The display shows the current I/O Link status for the primary and the secondary (if present) IOP, in the High-Performance Process Manager. Up to 40 IOPs are configurable in the HPM. The information is given in a tabular form. IOPs are arranged in the order of their module number on the I/O Link Interface.

The data table is displayed on three pages. Page 1 displays the data for modules 1-15, page 2 for modules 16-30, and page 3 for modules 31-40. The 01..15, 16..30, or 31..40 target is used to select the desired display. For both the primary and secondary IOP (if it exists), there are seven subcolumns. The subcolumn labels are described in the table that follows. Data for “configured-but-not responding” IOPs appears in red.

The displayed data is snapshot data that is updated every 4 seconds. The **REFRESH VALUES** target can be used to update the displayed data.

Continued on next page

3.4.4.2 IOM I/O Link Information Displays, Continued

DSA data fields

The DSA data fields for the IOM I/O Link nodes are defined in Table 3-23.

Table 3-23 IOM I/O Link Information Display

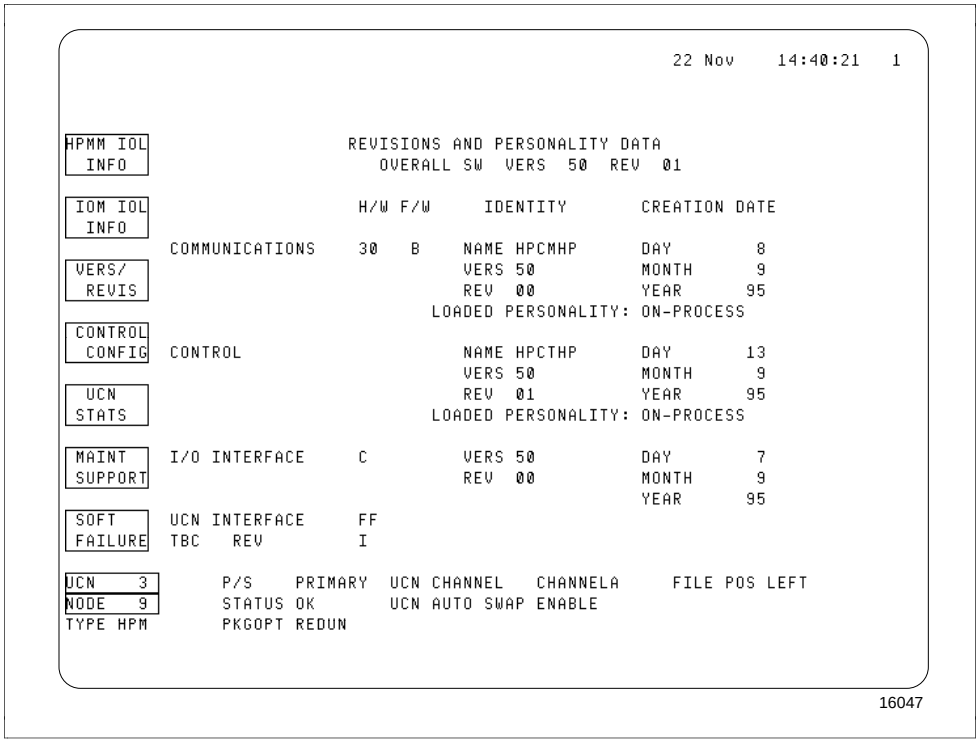
Term	Description
MD	The module number (1-40)
CHN	The current I/O Link receive channel (A or B)
ERRORS A **ERRORS B** **SILENCES A** **SILENCES B**	The total errors/silences detected on the A and B I/O Link cables since the IOP was started or the last reset of the I/O Link errors/silences from the HPMM I/O Link Information display.
LAST ERR	The last I/O Link error detected by the IOP. Reset of the error/silence totals from the HPMM I/O Link Information display sets the error to NONE.

3.4.4.3 HPMM Version/Revision Display

Target selection

The selection of the **VER/REVIS** target on the I/O Link Information display invokes the HPMM Version/Revision display shown in Figure 3-36 which shows the current version/revision/personality information for the hardware and software present in the HPMM.

Figure 3-36 HPMM Version/Revision Display



Continued on next page

3.4.4.3 HPMM Version/Revision Display, Continued

Version and revision data

The information is derived from the hardware boards, firmware ROMs, and the personality data contained in the software. The information is tabular and the column headers are defined in Table 3-24.

Table 3-24 HPMM Version/Revision Display

Term	Description
OVERALL SW VERS REV	Uniquely ties the Communications and Control component software version and revision together.
H/W	The hardware version/revision of the HPMM cards and the HPM UCN Interface module
F/W	The firmware version/revision for the Communications and Control processors
IDENTITY	The NAME, VERSion, and REVision of the software personalities that are currently hosted by the Communications, Control, and I/O Link processors.
CREATION DATE	The DAY, MONTH, and YEAR of the creation of the software personalities that are currently hosted by the Communications, Control, and I/O Link processors.
LOADED PERSONALITY	The present state of the Communications and Control processor personalities

3.4.4.4 HPMM Control Configuration Display

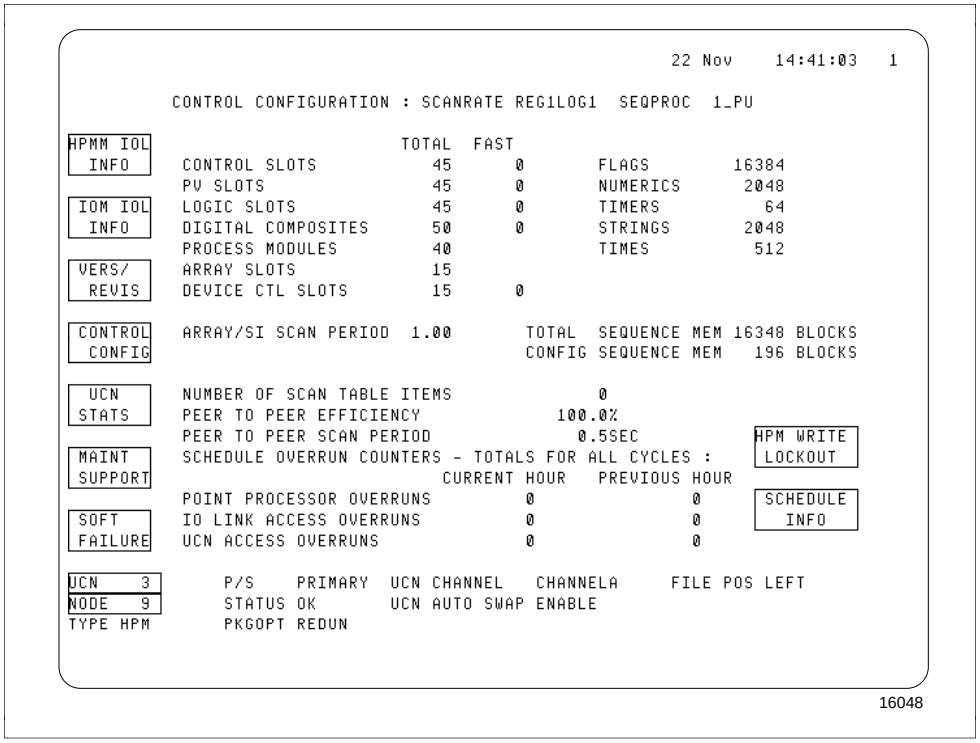
Target selection

Selection of the **CONTROL CONFIG** target on the HPMM Detail Status display invokes the HPMM Control Configuration display for the primary HPMM only. There are two displays associated with the **CONTROL CONFIG** target.

HPMM Control Configuration display

Initial selection of the **CONTROL CONFIG** target produces the HPMM Control Configuration display shown in Figure 3-37. The display has two main sections, Control Configuration and Schedule Overrun Counters.

Figure 3-37 HPMM Control Configuration Display



Continued on next page

3.4.4.4 HPMM Control Configuration Display, Continued

Control Configuration display information

Control Configuration information is found in Table 3-25.

Table 3-25 HPMM Control Configuration Display

Term	Description
SCANRATE	See the *Process Operations Manual*, Section 18, for the displayed states.
SEQPROC	See the *Process Operations Manual*, Section 18, for the displayed states.
TOTAL SEQUENCE MEM	The TOTAL SEQUENCE MEMory available in BLOCKS
CONFIG SEQUENCE MEM	The CONFIGuration SEQUENCE MEMory available in BLOCKS
CONTROL SLOTS	Number of regulatory CONTROL SLOTS and the number configured for FAST scan
PV SLOTS	The total number of regulatory PV SLOTS and the number configured for FAST scan
LOGIC SLOTS	Total number of regulatory LOGIC SLOTS and the number configured for FAST scan
DIGITAL COMPOSITES	The total number of regulatory DIGITAL COMPOSITE slots and the number configured for FAST scan
PROCESS MODULES	The total number of PROCESS MODULES
ARRAY SLOTS	The total number of ARRAY SLOTS
DEVICE CTL SLOTS	The total number of regulatory DEVICE CTL (Control) SLOTS and the number configured for FAST scan
FLAGS	The total number of FLAGS
NUMERICS	The total number of NUMERICS
TIMERS	The total number of TIMERS
STRINGS	The total number of STRINGS
TIMES	The total number of TIMES
ARRAY/SI SCAN PERIOD	The ARRAY/SI (Serial Interface) SCAN PERIOD in seconds
NUMBER SCAN TABLE ITEMS	The number of Scan table items
PEER TO PEER EFFICIENCY	The peer to peer efficiency in percentage.
PEER TO PEER SCAN PERIOD	The peer to peer scan period in seconds.

Continued on next page

Schedule Overrun Counters

The Schedule Overrun Counters portion of the display shows the total overruns for the previous and the current hour for all eight subcycles of the Control processor scan. On the hour, the **CURRENT HOUR** values become the **PREVIOUS HOUR** values and the **CURRENT HOUR** values are reset. The overruns are defined in Table 3-26.

Table 3-26 HPMM Schedule Overrun Counters Statistics

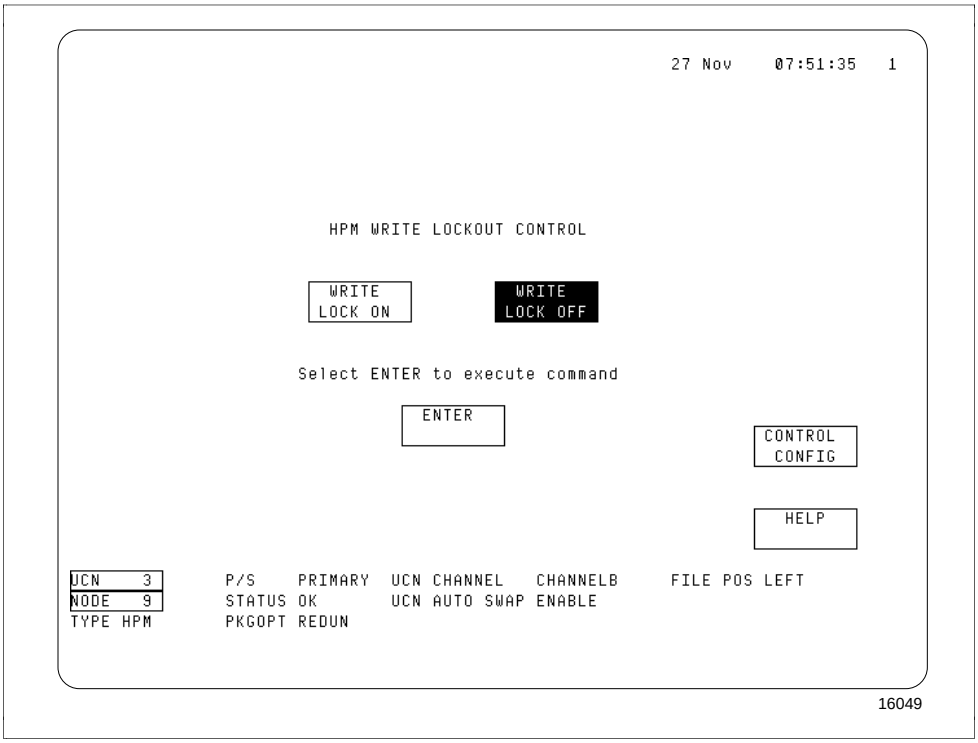
Term	Description
POINT PROCESSOR OVERRUN	The number of times that the processing of all points could not be completed in 1 second.
I/O LINK ACCESS OVERRUNS	The number of timeouts that were encountered during data requests from the IOPs.
UCN ACCESS OVERRUNS	The number of timeouts that were encountered during access of data from HPM, APM, PM, or LM peers.

3.4.4.5 HPM Write Lockout Displays

HPM WRITE LOCKOUT target

Control of HPM Write Lockout can be executed from the HPM Write Lockout Control display. The display is produced by selecting the **HPM WRITE LOCKOUT** target. The display is shown in Figure 3-38.

Figure 3-38 HPM Write Lockout Control Display



WRITE LOCK ON/OFF target selection

The HPM Write Lockout state can be altered only when the HPMM is in the OK or Soft Failure state and the US keylock is in the **ENGINEER** position.

If the proper conditions exist, selecting the **WRITE LOCK ON** target or **WRITE LOCK OFF** target, whichever is appropriate, followed by selecting the **ENTER** target, executes the command.

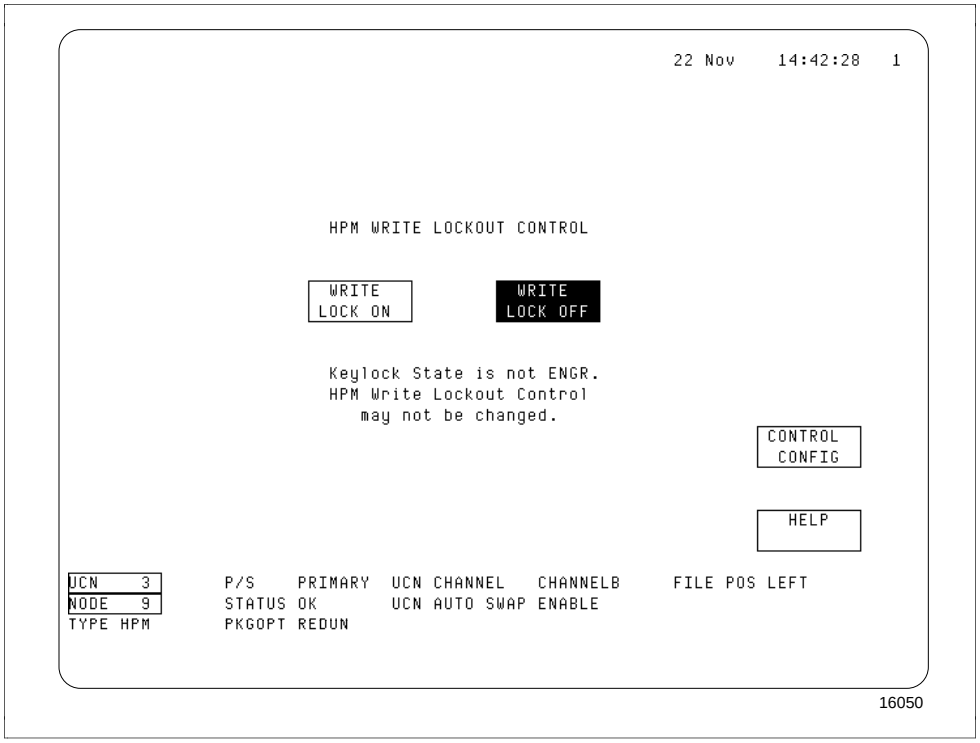
Continued on next page

3.4.4.5 HPM Write Lockout Displays, Continued

US ENGINEER keylock position

Failure to have the US keylock in the ENGINEER position when executing the HPM Write Lockout on/off command results in the HPM Write Lockout Control display shown in Figure 3-39.

Figure 3-39 HPM Write Lockout Control Display – Improper US Keylock Position

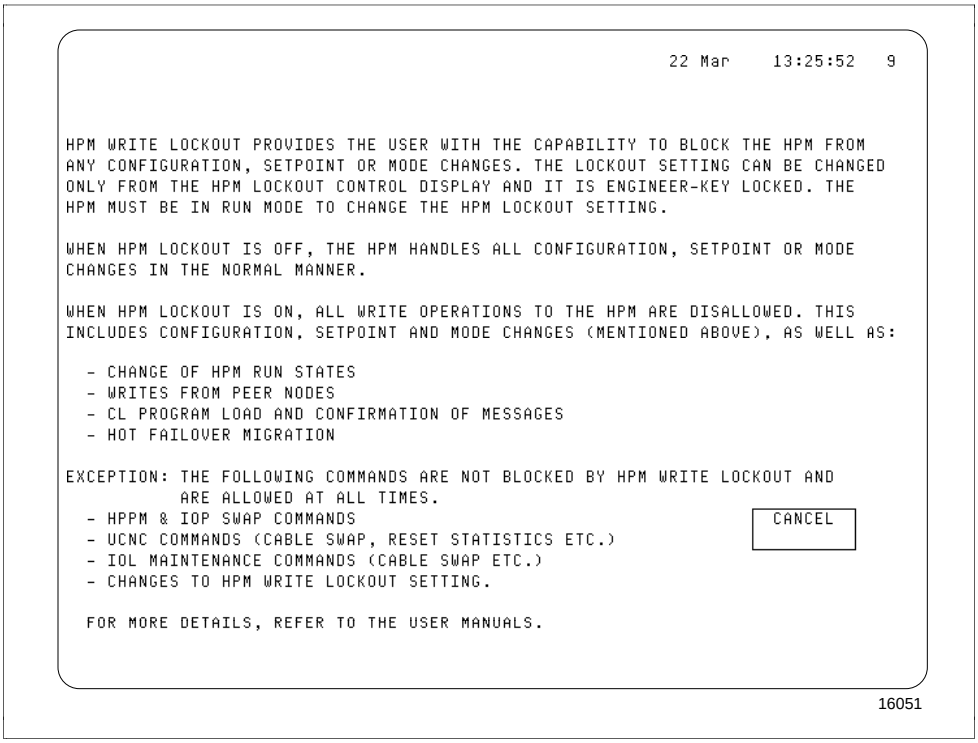


Continued on next page

HELP target selection

Selecting the HELP target on the HPM Write Lockout Control display produces the HPM Write Lockout Control Help display shown in Figure 3-40.

Figure 3-40 HPM Write Lockout Control Help Display

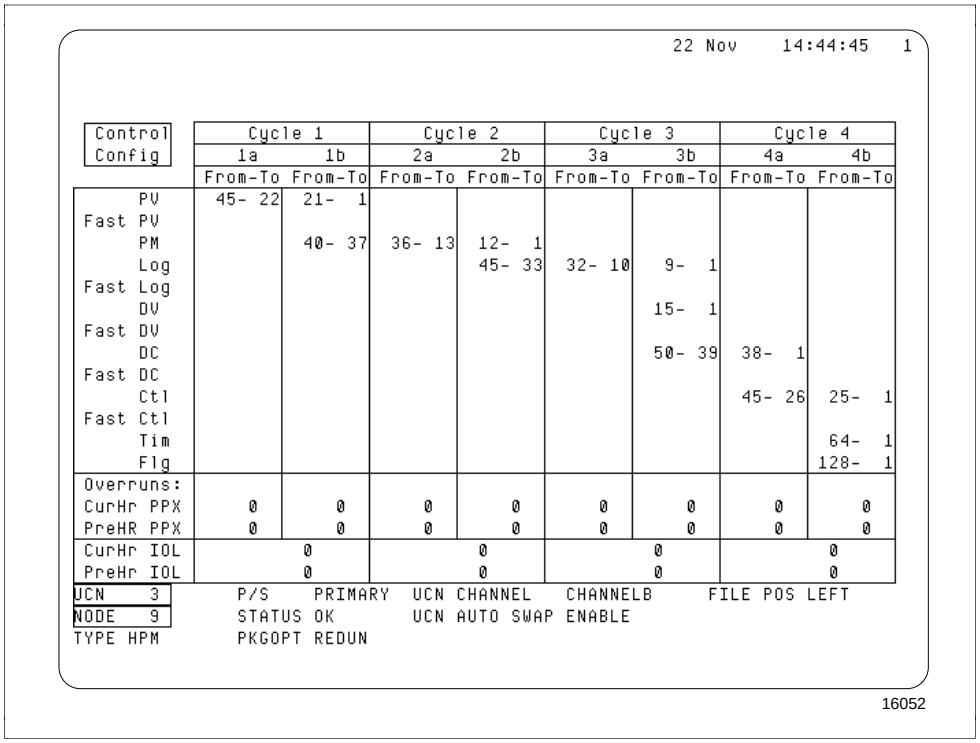


3.4.4.6 HPMM Schedule Information Display

Target selection

A detailed analysis of the assignment of the Control processor points for the eight subcycles of the Control processor scan is available by selecting the **SCHEDULE INFO** target. This invokes the HPMM Schedule Information display shown in Figure 3-41.

Figure 3-41 HPMM Schedule Information Display



Four cycles

The Control processor 1-second point processing scan is divided into four cycles, each of which contains two subcycles. When configuring the Control processor and its associated entities, the user distributes the processing of the various point types among the several subcycles by slot type and slot number. This information is shown in the HPMM Schedule Information display in tabular form, along with the overrun counters for each cycle and subcycle. Inspection of the data in this table enables the user to determine where the assignment of slots is causing overruns and enables correction of the distribution to minimize overloading

Continued on next page

3.4.4.6 HPMM Schedule Information Display, Continued

Slot indices

Each box in the upper part of the table shows which slot indices of each point type are being processed in a given subcycle of the processing scan. For example, in Figure 3-41, PV Slots 25 through 9 are being processed during subcycle 1a, Logic Slots 17 through 1 are being processed during subcycle 2b, and so on. This information is fixed as a result of configuration and is not updated in the display.

Overruns

The overruns in the lower portion of the display are updated every 4 seconds. Point Processing Execution (PPX) overruns are computed for each subcycle. I/O Link (IOL) access overruns are computed for each cycle.

3.4.4.7 HPMM UCN Statistics Displays

Target selection

The displays invoked by selection of the **UCN STATS** target on the HPMM UCN Detail Status display are very similar to the displays described in the NIM Detail Status Displays subsection, 3.4.3. The HPMM UCN statistics and status are maintained by the HPMM's UCN Driver. Use the **HELP** target on the display for descriptions of the statistics and status. Performance statistics descriptions, which are unique to the HPMM UCN Statistics display, are found in Table 3-27. The displays are shown in Figures 3-42 and 3-43.

Table 3-27 Performance Statistics

Statistic	Description
Comm Processor CPU Free	Indicates the Communications processor's free time as a percentage of availability.
Control Processor CPU Free	Indicates the Control processor's free time as a percentage of availability.
I/O Link Bandwidth Free	Indicates the I/O Link Communications Channel's free time as a percentage of availability.

HELP target

Refer to Figures 3-42 and 3-43.

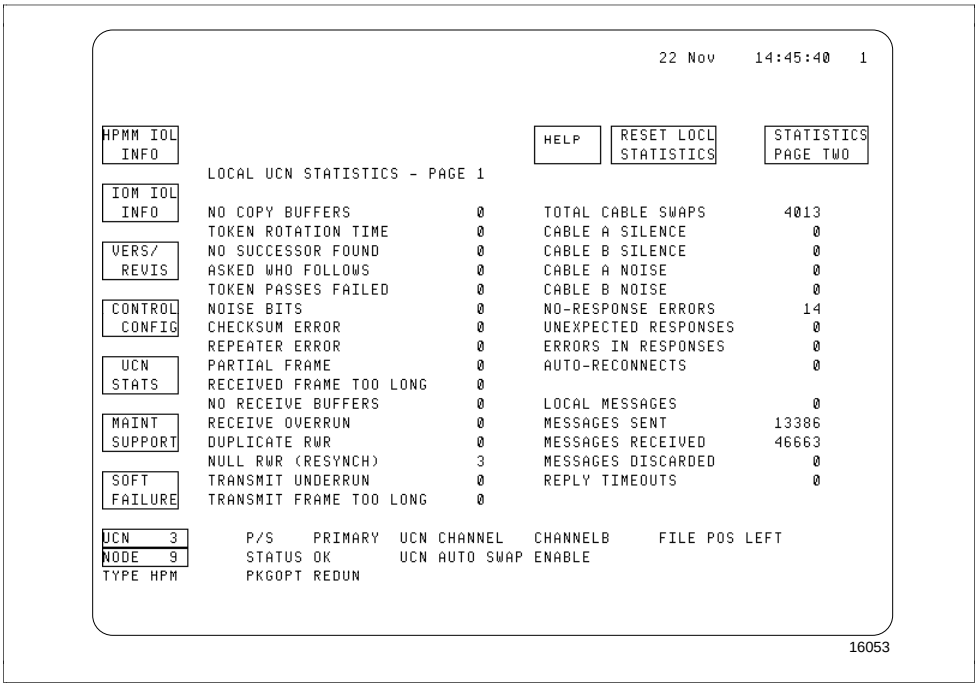
The **HELP** target is used to gain greater insight into each statistical entry on the 2-page HPMM UCN Statistics display. To use it, you simply select the individual entry that you would like more information about, and then select the **HELP** target. The resultant display provides the following information about the statistical entry you selected.

- Description
- Normal Value
- How the system recovers from a failure
- Probable cause of a failure
- Reference to other statistics for correlation

Continued on next page

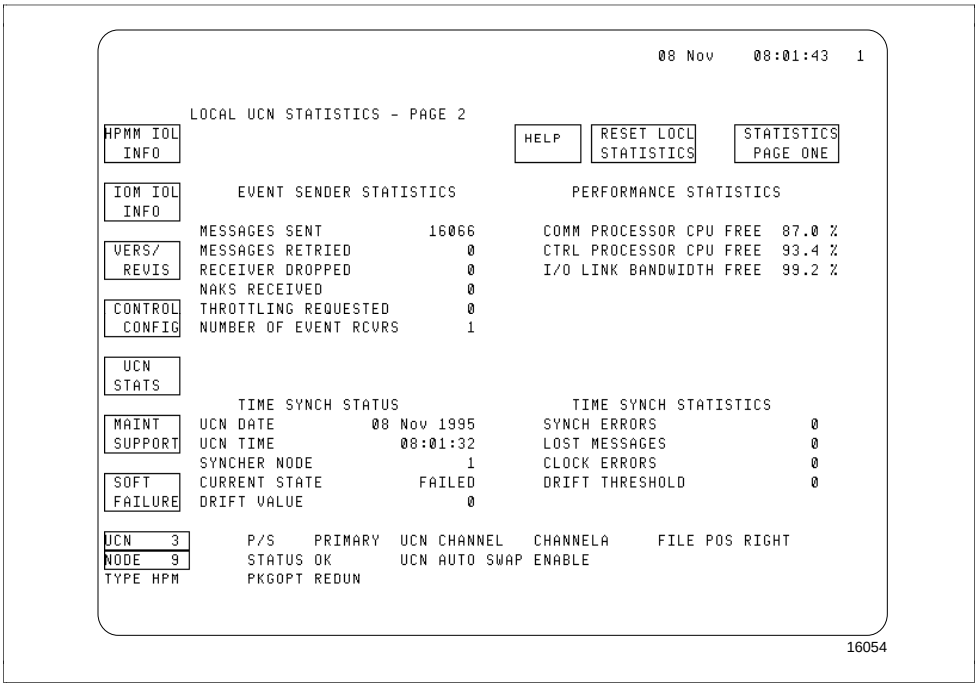
HPMM UCN Statistics display – Page 1

Figure 3-42 HPMM UCN Statistics Display – Page 1



HPMM UCN Statistics display – Page 2

Figure 3-43 HPMM UCN Statistics Display – Page 2



3.4.4.8 HPMM Maintenance Support Displays

Target selection

The **MAINT SUPPORT** target provides access to six displays related to software errors, patches, the current state of the HPMM, and manufacturing information. The displays are shown in Figures 3-44 through Figure 3-49 and contain six secondary targets, **CONTROL ERROR BLK**, **COMMUNCTN ERROR BLK**, **CONTROL PATCHES**, **COMMUNCTN PATCHES**, **NODE STS INFO**, and **MANUFAC INFO**.

Communications Error Block display

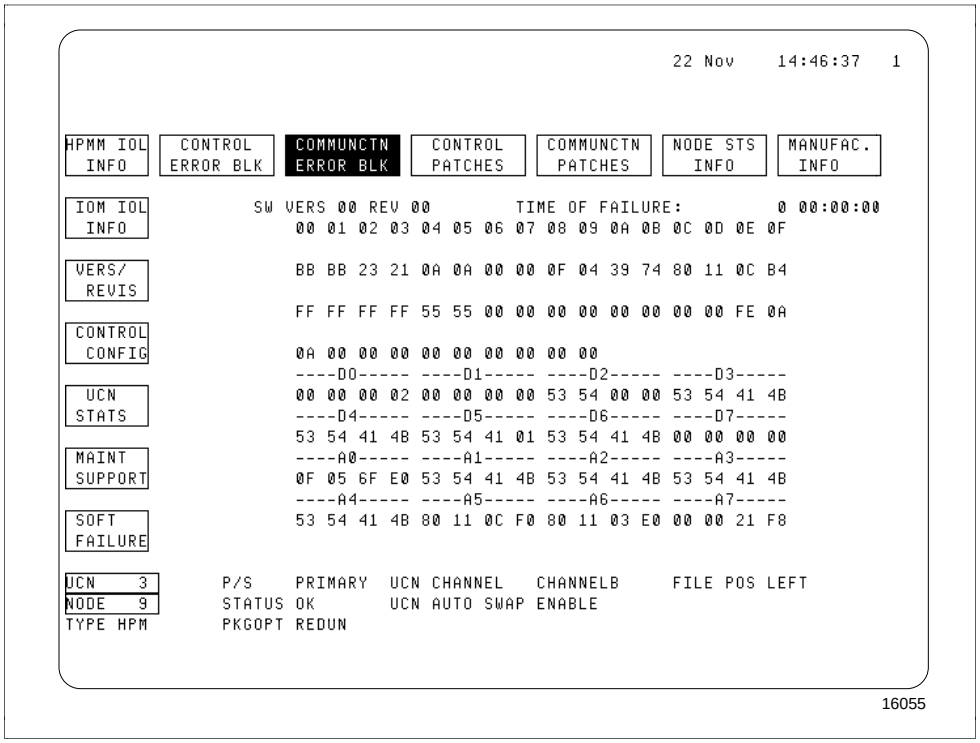
The initial display produced by selection of the **MAINT SUPPORT** target is the Communications Error Block display as shown in Figure 3-44. The display provides the latest error information from the HPMM Communications processor. The error information consists of an error block in LCN error block format and the associated register values.

The Communications software version (**VERS**) and revision (**REV**) is displayed as well as the time of the last failure (**TIME OF FAILURE**).

Error information is not updated while the display is in view. The HPMM Detail Status display must be reselected to view changes in the error data.

Notice the reference to access Hard failure codes in the HPM Service manual. Table 4-2 is located in Section 4 of this manual.

Figure 3-44 HPMM Communications Error Block Display



Continued on next page

Control Error Block display

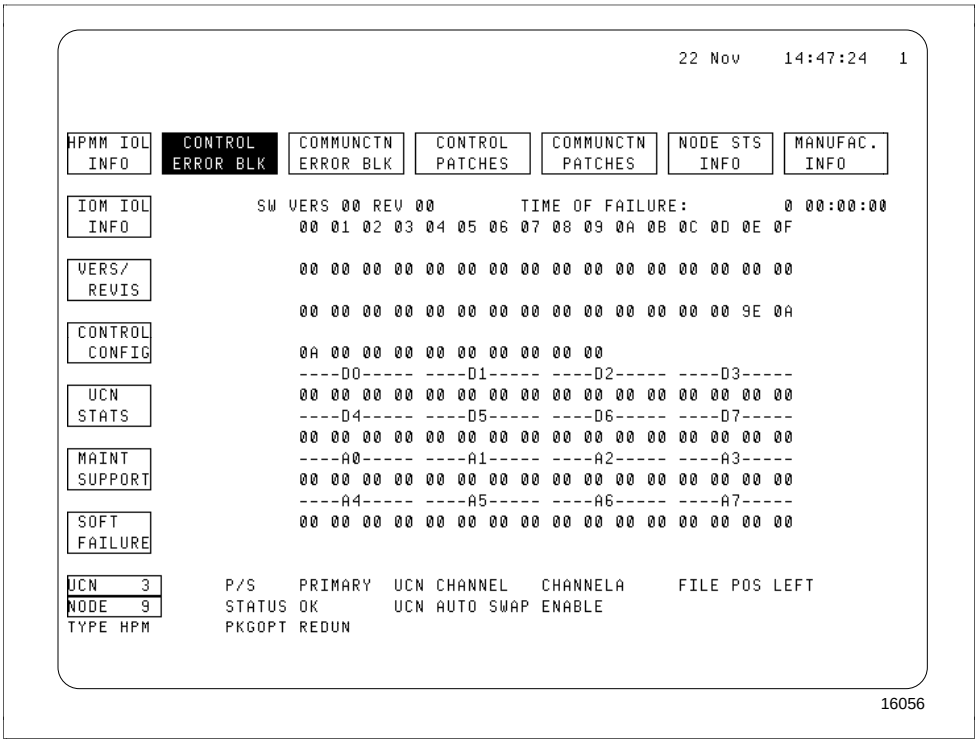
The selection of the **CONTROL ERROR BLK** target invokes the Control Error Block display, providing the latest error information from the HPMM Control processor. The error information consists of an error block in LCN error block format and the associated register values as shown in Figure 3-45. The display is also available by selection of the **CONTROL ERROR BLK** target while in any of the other Maintenance Support displays.

The Control software version (**VERS**) and revision (**REV**) is displayed as well as the time of the last failure (**TIME OF FAILURE**).

Error information is not updated while the display is in view. The HPMM Detail Status display must be reselected to view changes in the error data.

Notice the reference to access Hard failure codes in the HPM Service manual. Table 4-2 is located in Section 4 of this manual.

Figure 3-45 HPMM Control Block Display

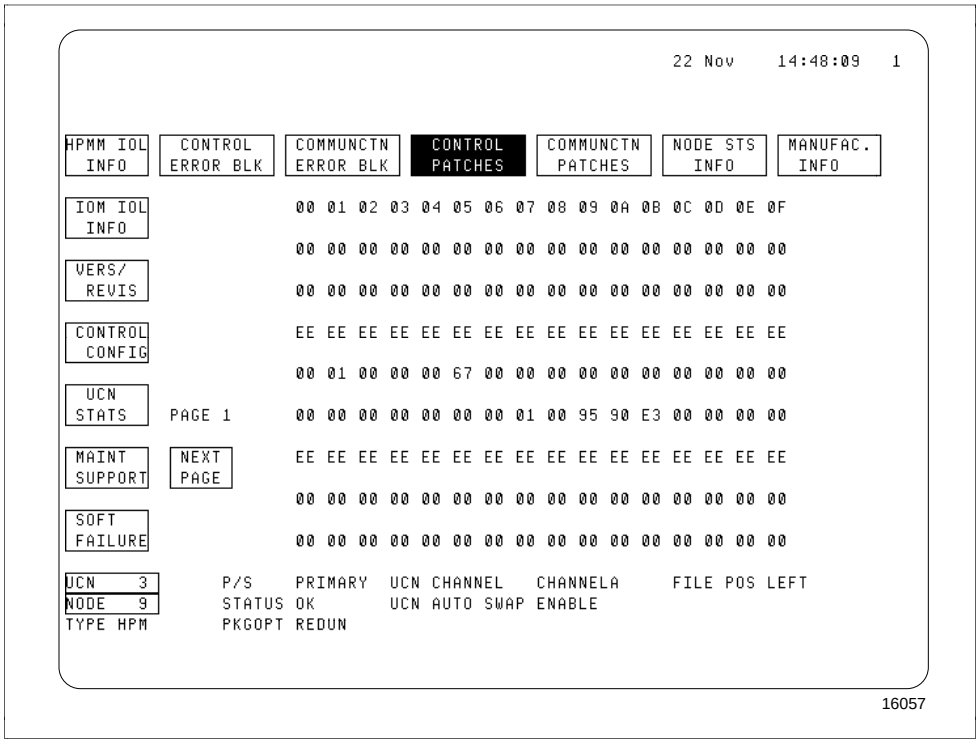


Continued on next page

Control Patches display

The HPMM Control processor maintains a 256-word patch area. This area can be displayed by selection of the **CONTROL PATCHES** target. The Control Patches display is composed of four pages showing 64 words per page. Page 1 is shown in Figure 3-46. To page forward in the display, the user selects the **NEXT PAGE** target. Paging backwards is not permitted. The page forward function has a wraparound feature.

Figure 3-46 HPMM Control Patches Display



ATTENTION

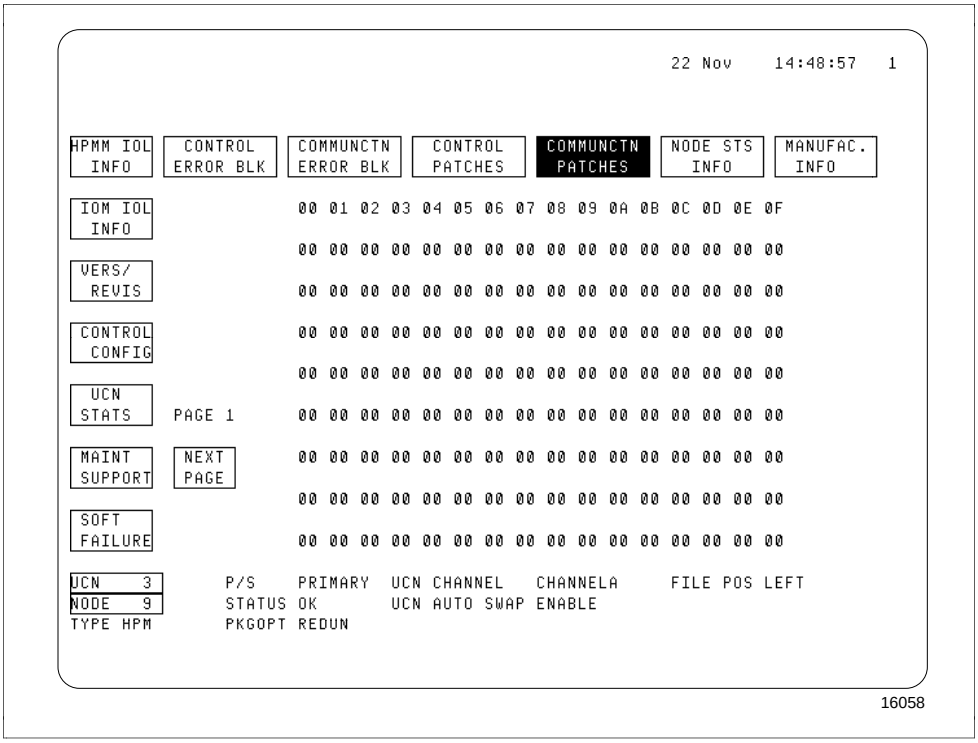
ATTENTION—The Control Patches are used are used for Honeywell maintenance purposes only.

Continued on next page

Communications Patches display

The HPMM Communications processor maintains a 256-word patch area. This area can be displayed by selection of the **COMMUNCTN PATCHES** target. The Communications Patches display is composed of four pages showing 64 words per page. Page 1 is shown in Figure 3-47. To page forward in the display, the user selects the **NEXT PAGE** target. Paging backwards is not permitted. The page forward function has a wraparound feature.

Figure 3-47 HPMM Communications Patches Display



ATTENTION

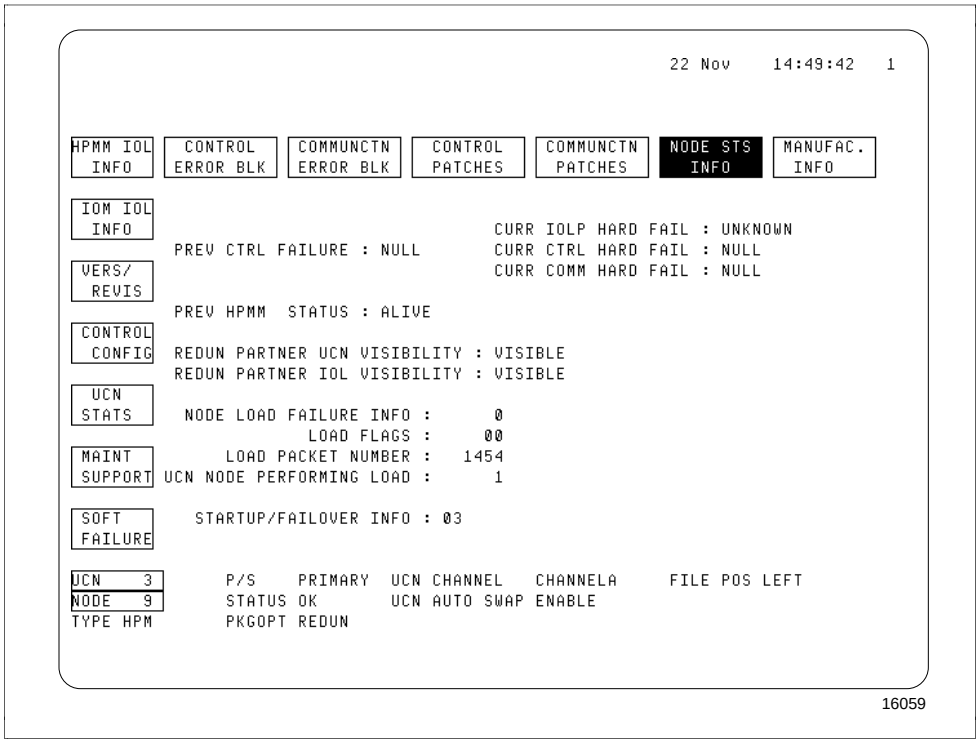
ATTENTION—The Communications Patches are used are used for Honeywell maintenance purposes only.

Continued on next page

HPMM Node Status Information display

The Node Status Information display that is selected by the **NODE STS INFO** target contains miscellaneous information relative to the status of the HPMM. The format of the display is shown in Figure 3-48.

Figure 3-48 HPMM Node Status Information Display



Continued on next page

Data fields definitions

The display data fields are defined in Table 3-28. Data is updated every 4 seconds.

Table 3-28 HPMM Node Status Information Display

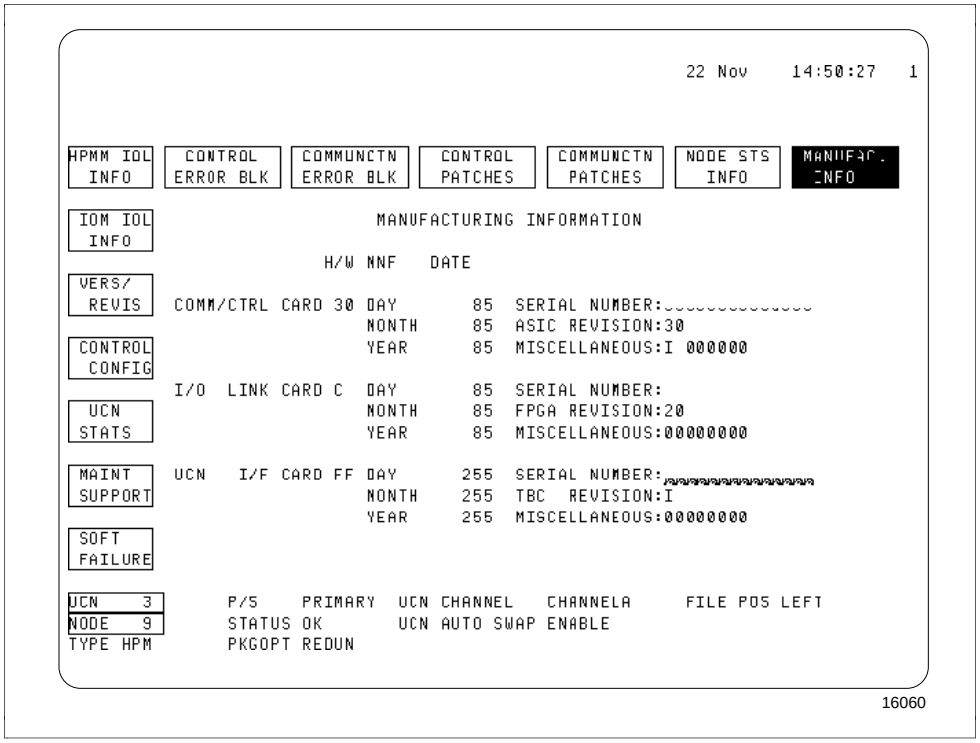
Term	Description
PREV CTRL FAILURE	The Hard failure condition that existed prior to the last restart of the HPMM Control processor. The mnemonic in this field serves as an entry to the Table 4-2 in Section 4 of this document.
CURR IOLP HARD FAIL	The current Hard failure detected by the I/O Link processor. The mnemonic in this field serves as an entry to Table 4-2 in Section 4 of this document.
CURR CTRL HARD FAIL	The current Hard failure detected by the HPMM Control processor. The mnemonic in this field serves as an entry to Table 4-2 in Section 4 of this document.
CURR COMM HARD FAIL	The current Hard failure detected by the HPMM Communications processor. The mnemonic in this field serves as an entry into Table 4-4 in Section 4 of this document.
PREVIOUS HPMM STATUS	The previous status of the HPMM Communications processor. (ALIVE, IDLE, FAIL, OK, POWERON)
REDUN PARTNER UCN VISIBILITY	The redundant HPMM's visibility on the UCN (VISIBLE or NOT VISIBLE).
REDUN PARTNER IOL VISIBILITY	The redundant HPMM's visibility on the I/O Link. (VISIBLE or NOT VISIBLE).
NODE LOAD FAILURE INFO	A code that indicates the reason for the failure of the HPMM load.
LOAD FLAGS	Hexadecimal data that shows the status of the load operation.
LOAD PACKET NUMBER	The current load packet identifier
UCN NODE PERFORMING LOAD	An integer that gives the address of the UCN node performing the load.
STARTUP/FAILOVER INFO	Hexadecimal data that shows the state of the HPMM at startup or failover.

Continued on next page

Manufacturing Information display

The Manufacturing Information display that is selected by the **MANUFAC INFO** target contains miscellaneous information that is relative to the manufacturing diagnostic software. The format of the display is shown in Figure 3-49.

Figure 3-49 Manufacturing Information Display

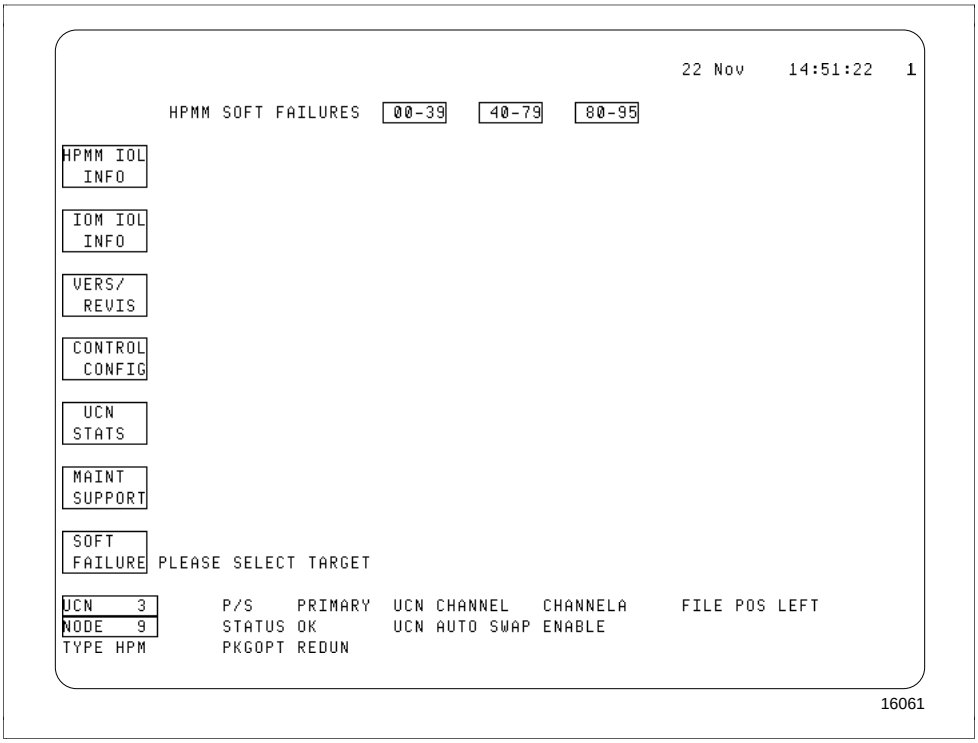


3.4.4.9 HPMM Soft Failure Displays

Target selection

Selection of the **SOFT FAILURE** target on the HPMM Detail Status display provides access to three displays which show Soft failures that can exist in the HPMM. Selecting the **SOFT FAILURE** target produces the HPMM Soft Failure display shown in Figure 3-50.

Figure 3-50 HPMM Soft Failure Display



Failure code descriptions

Descriptions of the failure codes and the possible corrective actions can be found in Table 4-3 in Section 4 in this manual.

Three targets

Each display consists of three targets, **00-39**, **40-79**, and **80-95**, at the top of the display, and a table of Soft failures below the targets. The Soft failures are displayed in two columns. All possible Soft failures are displayed in half intensity text. Those failures that currently exist in the HPMM are highlighted by being shown in reverse video. The operator can step freely through the three displays by selection of the targets at the top of the display.

4-second update

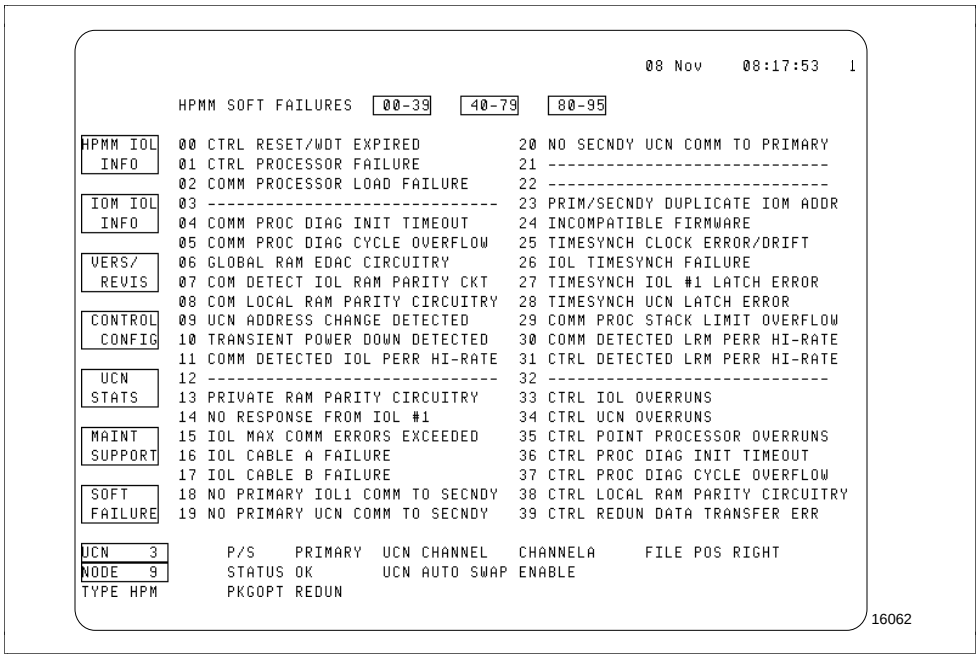
The data is updated every 4 seconds.

Continued on next page

HPMM Soft Failure – 00-39 display

The HPMM Soft Failure display for error codes 00 through 39 is shown in Figure 3-51.

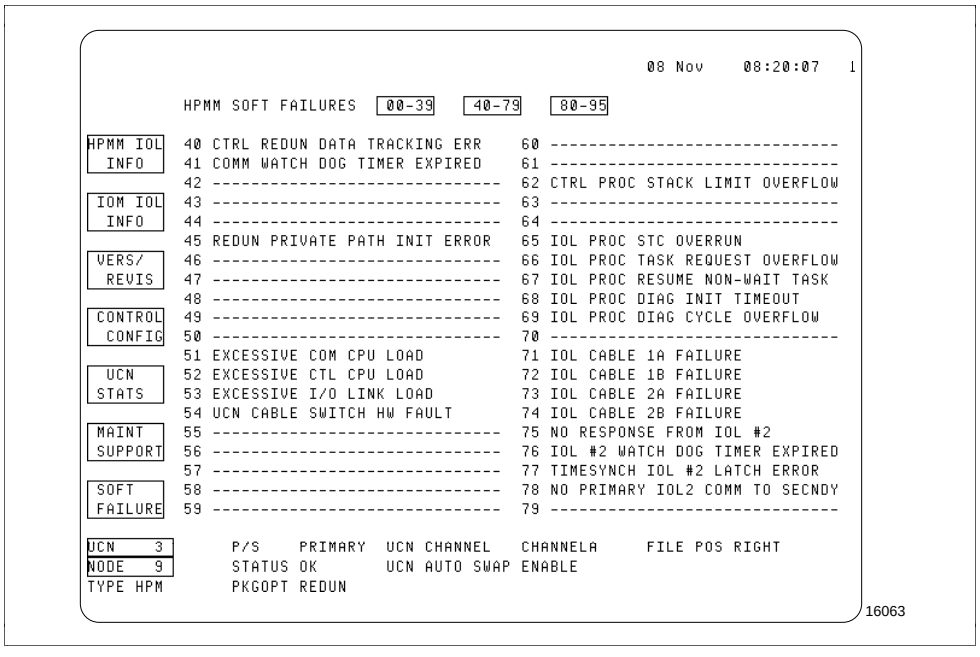
Figure 3-51 HPMM Soft Failure Display – 00-39



HPMM Soft Failure – 40-79 display

The HPMM Soft Failure display for error codes 40 through 79 is shown in Figure 3-52.

Figure 3-52 HPMM Soft Failure Display – 40-79

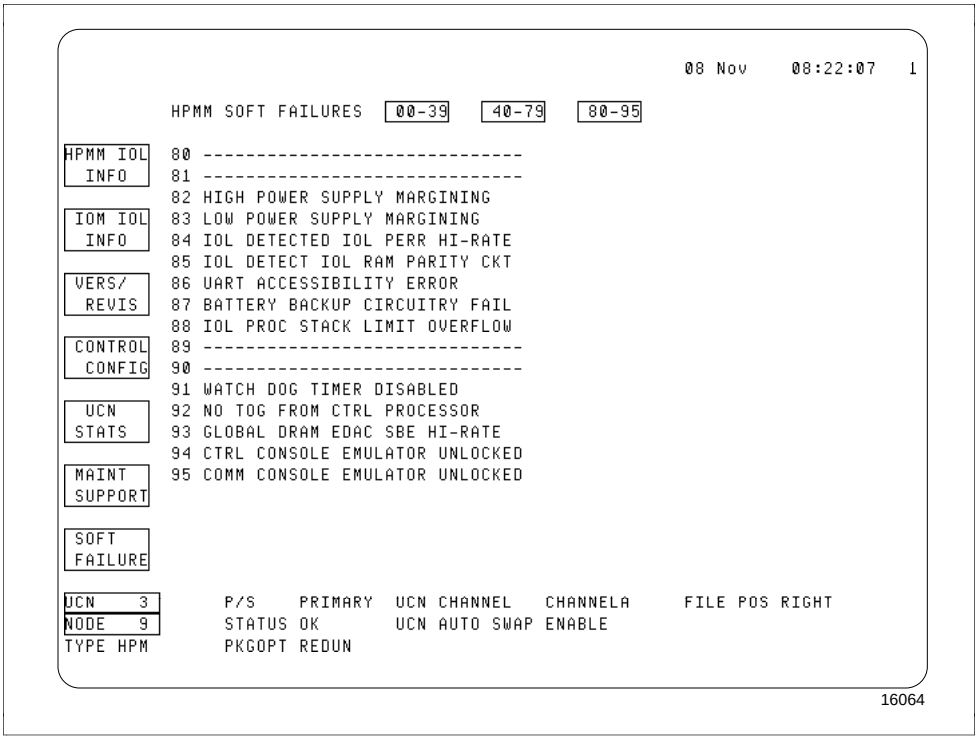


Continued on next page

HPMM Soft Failure – 80-95 display

The HPMM Soft Failure display for error codes 40 through 79 is shown in Figure 3-53.

Figure 3-53 HPMM Soft Failure Display – 80-95

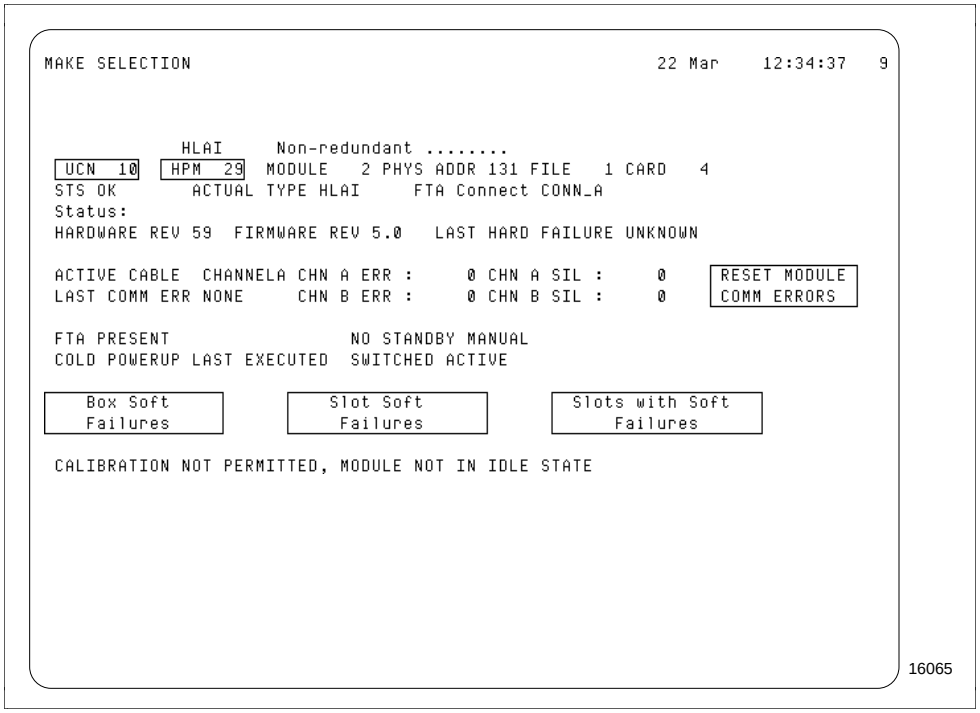


3.4.5 IOP Detail Status Displays

IOP Detail Status display

The IOP Detail Status displays consist of the initial display called the Input/Output Processor (IOP) Detail Status display, and several displays associated with Soft failures. The IOP Detail Status display provides information that is dependent on the IOP type. Figure 3-54 shows the IOP display for a primary High Level Analog Input (HLAI) IOP.

Figure 3-54 HLAI IOP Detail Status Display



Top portion of display

The top portion of the IOP Detail Status display contains the following information.

- The IOP configuration
- Hardware/firmware revisions and the last Hard failure
- I/O Link cable status and statistics
- Status messages
- **PRIMARY** or **SECONDARY IOP STATUS** targets, if redundant
- **SOFT FAILURE** targets

Primary and secondary IOP displays

Switching between the primary and secondary IOP Detail Status displays is provided by the **SECONDARY IOP STATUS** target on the primary display and the **PRIMARY IOP STATUS** target on the secondary display.

Bottom of display

The information at the bottom of the IOP Detail Status display varies. It is dependent on the IOP type. For example, in Figure 3-54, "**CALIBRATION NOT PERMITTED, MODULE NOT IN IDLE**" appears for the HLAI IOP.

Continued on next page

3.4.5 IOP Detail Status Displays, Continued

IOP configuration

The first line of the display indicates the IOP type (**HLAI**, **LLAI**, **DI**, etc.), primary or secondary HPMM (**PRIMARY** or **SECONDARY**) or **Non-redundant**, and whether the IOP is configured as A or B (**IOM_A** or **IOM_B**).

The remaining information in this area is defined in Table 3-29. The status in this area is updated every 4 seconds.

Table 3-29 IOP Detail Status Display – IOP Configuration

Term	Description
UCN	The network number
HPM	The HPM address on the UCN
MODULE	The "soft" (logical) address of the IOP in the HPM configuration (1-40)
PHYS ADDR	The hardware address of the IOP on the I/O Link
FILE	The card file position of the IOP in the HPM
CARD	The slot position of the IOP in the card file
STS	The current status of the IOP (SOFTFAIL, OK, IDLE, IDLESF, NR)
ACTUAL TYPE	The IOP type read from the IOP (HLAI, LLAI, DI, DO, DO_32, LLMux, STIM, PI, SDI, SI, AO, or AO_32).
FTA CONNECT	The connector on the FTA that is in use (CONN_A or CONN_B).
WITH BIAS	Is the acting primary IOP the preferred IOP (YES or NO)?
HARDWARE REV	A hexadecimal byte that shows the current revision of the IOP hardware.
FIRMWARE REV	Two hexadecimal digits in the form "x.x" that shows the current firmware revision.
LAST HARD FAILURE	The last Hard failure detected by the IOP. The mnemonic in this field serves as an entry into Table 4-5 in Section 4 of this manual.
DESCRIPTION	If the IOP is a "High Density" IOP, such as a model MU-PDIY22 IOP, a description of the associated FTA will be included. Two types of FTA can be connected to the IOP (24 V or 240 V)

Continued on next page

I/O Link cable status and statistics

The data in this area is defined in Table 3-30.

The data is updated every four seconds. The area also contains the **RESET MODULE COMM ERRORS** target, selection of which resets the error/silence totals for the IOP, and resets the **LAST COMM ERR** field to **NONE**.

Table 3-30 IOP Detail Status Display – I/O Link Cable Status/Statistics

Term	Description
ACTIVE CABLE	The current I/O Link receive channel (CHANNEL A or CHANNEL B).
LAST COMM ERR	The last I/O Link communications error detected by the IOP
CHN A ERR	The total channel A errors detected by the IOP since startup or the last reset of the cable statistics
CHN B ERR	The total channel B errors detected by the IOP since startup or the last reset of the cable statistics
CHN A SIL	The total channel A silences detected by the IOP since startup or the last reset of the cable statistics
CHN B SIL	The total channel B silences detected by the IOP since startup or the last reset of the cable statistics

Status messages

This area contains status messages that are determined by status bits that are resident in the IOP. The messages are in pairs as defined in Table 3-31. The first message of each pair is the message that is displayed if the status bit is on. The status bits can be considered to be independent of one another, so the message pairs can appear in any combination.

Table 3-31 IOP Detail Status Display – I/O Link Cable Status Messages

Term	Description
FTA PRESENT/NO FTA	The presence or absence of a Field Termination Assembly (FTA) attached to the IOP
WARM START LAST EXECUTED/COLD START EXECUTED	The nature of the last IOP startup. A warm startup means that the IOP's database has been preserved. A cold startup means that the IOP has a default database.
STANDBY MANUAL ENABLED/NO STANDBY MANUAL	The presence or absence of a Standby Manual device
SWITCHED ACTIVE/NO SWITCHED ACTIVE	The presence or absence of a switched active device

Continued on next page

Loss of communications	If the data for the above messages is unavailable due to the loss of communication with the IOP, a message in the form, "**<message data> UNAVAIL**," will appear.
4-second data update	The data is updated every 4 seconds.

3.4.5.1 IOP Box Soft Failures Displays

SOFT FAILURE targets

Three Soft failure targets on the IOP display provide access to IOP Soft failure displays. The three targets are:

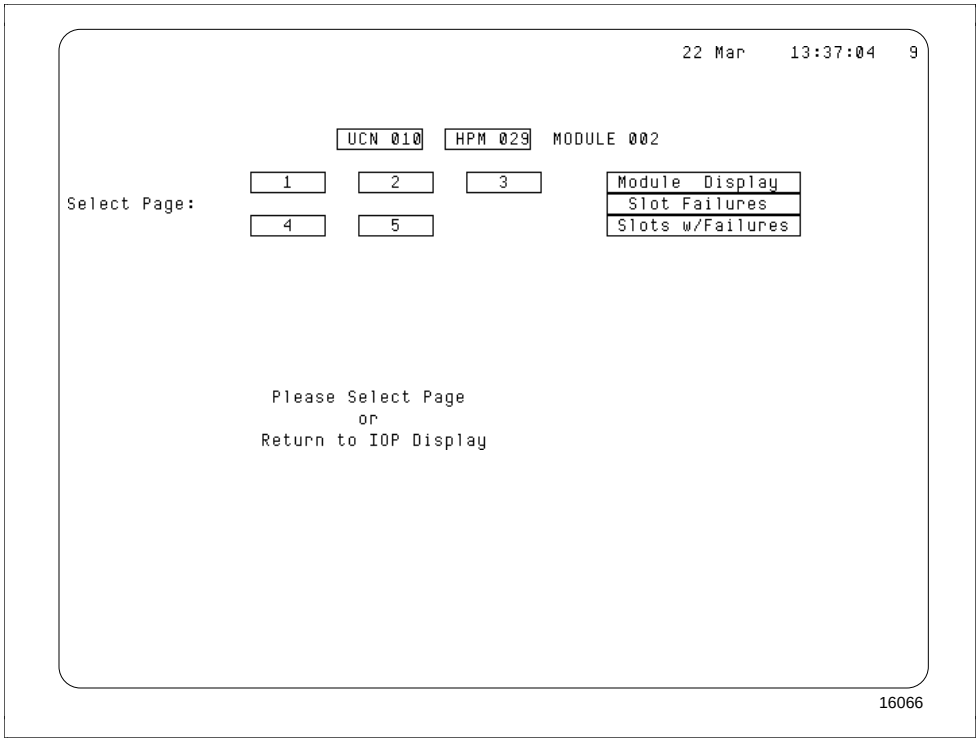
- **BOX SOFT FAILURES**
- **SLOT SOFT FAILURES**
- **SLOTS WITH SOFT FAILURES**

Targets on each display provide the ability to move between the three types of Soft failure displays and the IOP Detail Status display easily.

Target selection

The initial Box Soft Failures display, invoked by selection of the **BOX SOFT FAILURES** target on the IOP Detail Status display, is shown in Figure 3-55. The Box Soft Failures displays consist of five pages as shown in Figures 3-56 through 3-60. Each failure is described, and when the failure is active, an arrow appears pointing to the failure. Table 4-5 in Section 4 in this manual lists the errors and the suggested corrective actions.

Figure 3-55 IOP Box Soft Failures Display

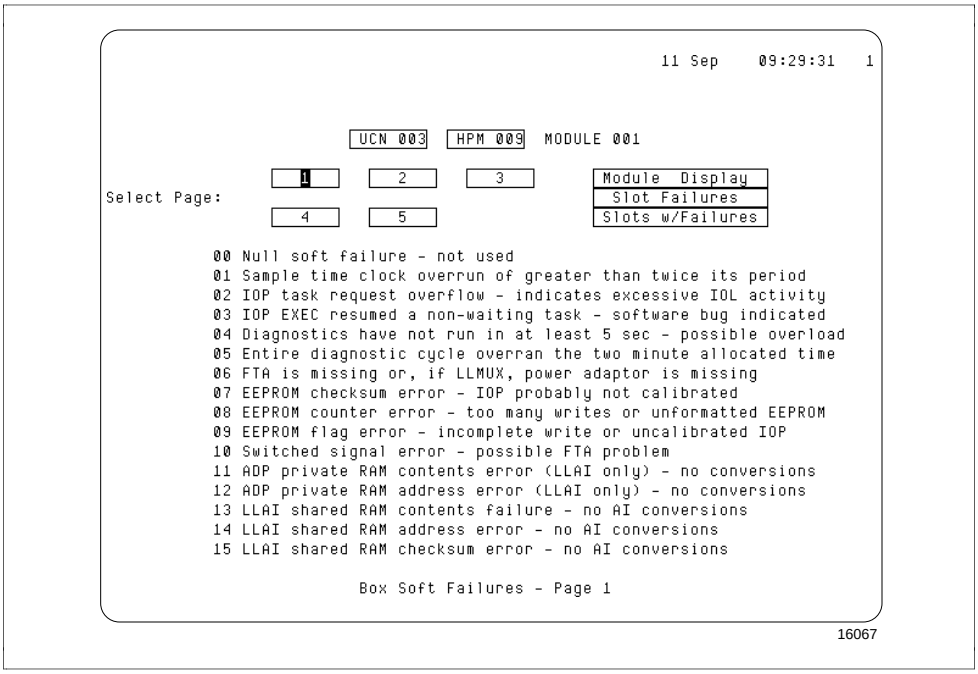


Continued on next page

IOP Box Soft Failures display – Page 1

Page 1 of the IOP Box Soft Failures displays is shown in Figure 3-56.

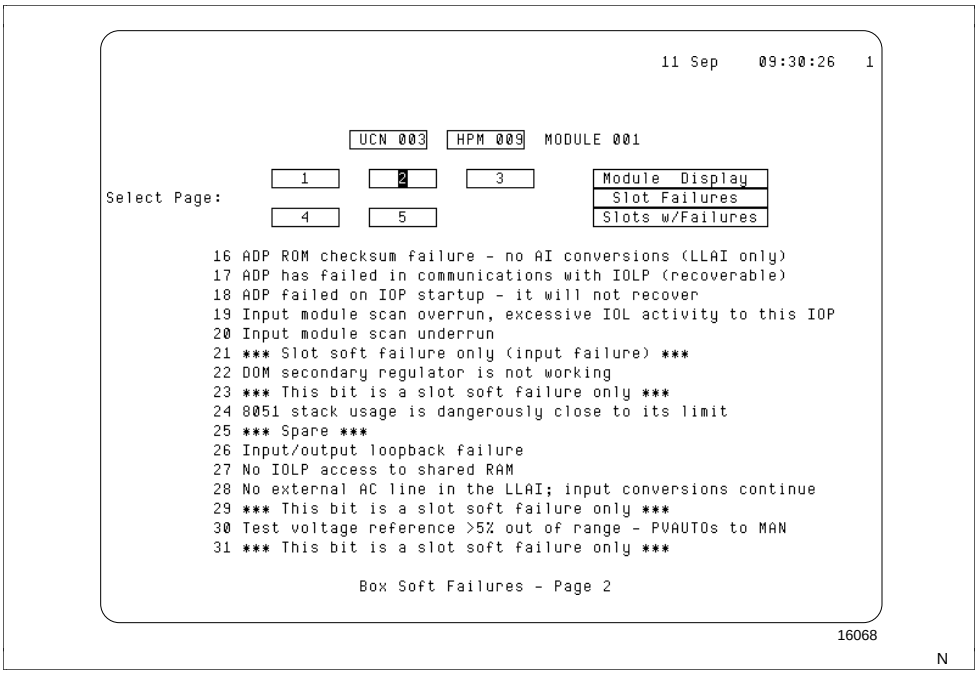
Figure 3-56 IOP Box Soft Failures Display – Page 1



IOP Box Soft Failures display – Page 2

Page 2 of the IOP Box Soft Failures displays is shown in Figure 3-57.

Figure 3-57 IOP Box Soft Failures Display – Page 2

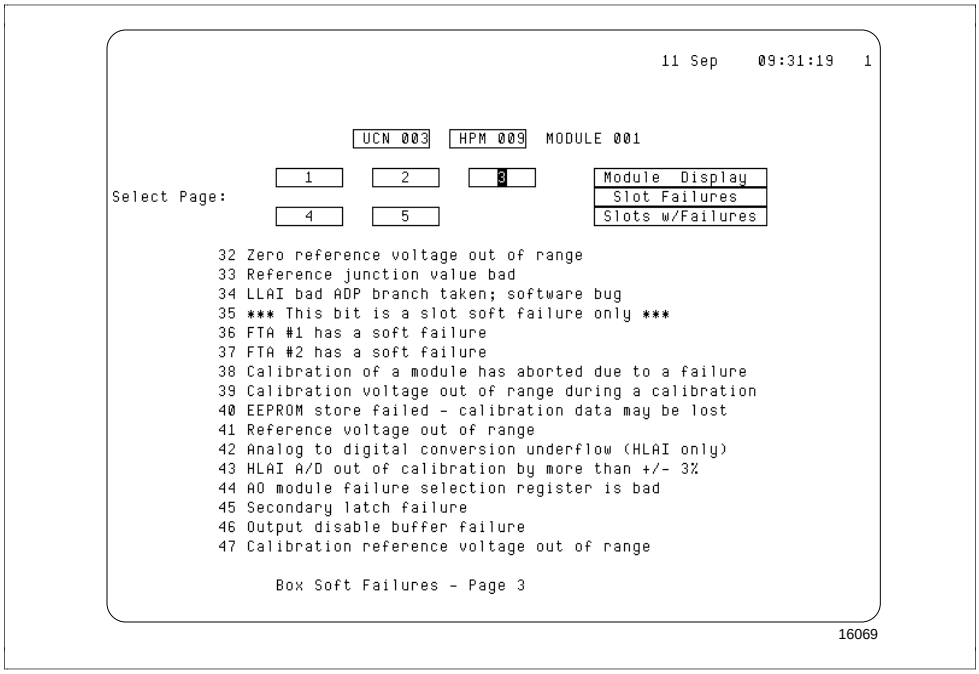


Continued on next page

IOP Box Soft Failures display – Page 3

Page 3 of the IOP Box Soft Failures displays is shown in Figure 3-58.

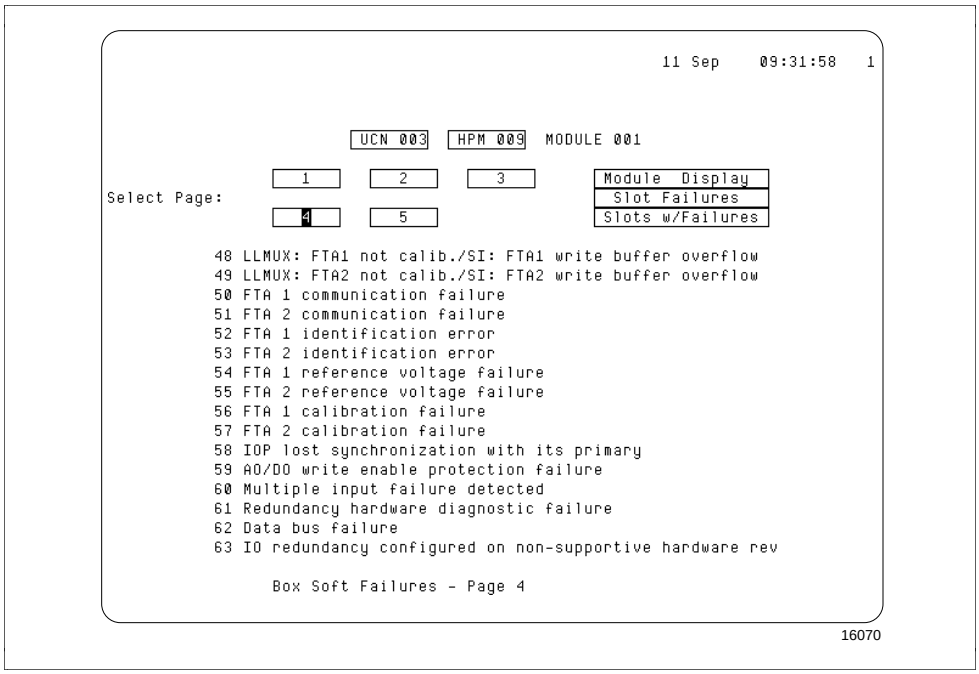
Figure 3-58 IOP Box Soft Failures Display – Page 3



IOP Box Soft Failures display – Page 4

Page 4 of the IOP Box Soft Failures displays is shown in Figure 3-59.

Figure 3-59 IOP Box Soft Failures Display – Page 4

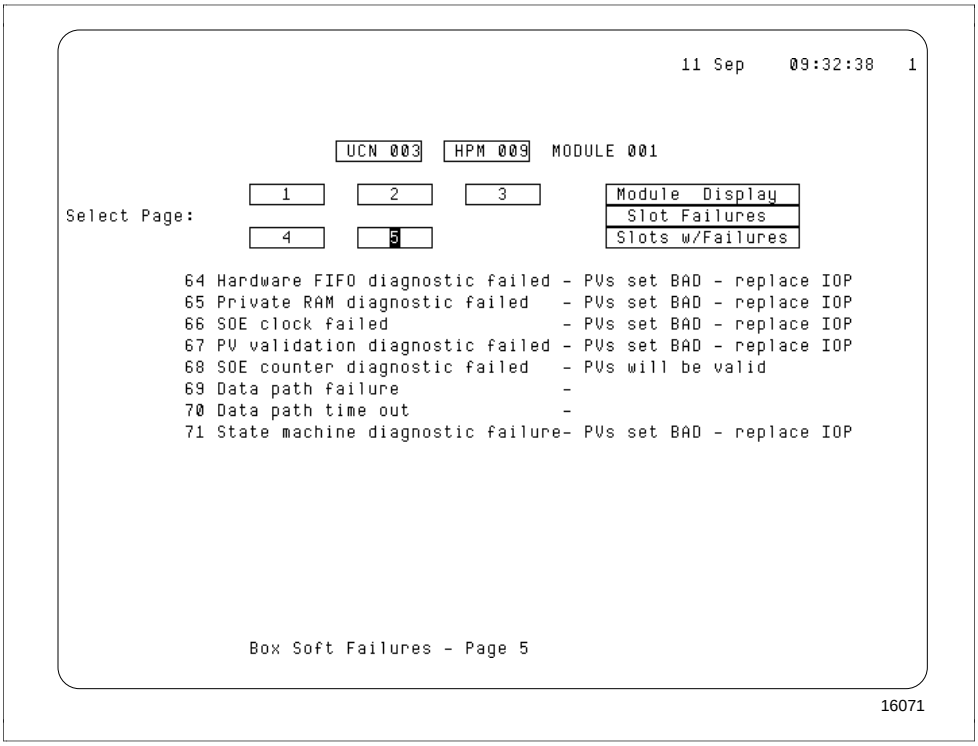


Continued on next page

IOP Box Soft Failures display – Page 5

Page 5 of the IOP Box Soft Failures displays is shown in Figure 3-60.

Figure 3-60 IOP Box Soft Failures Display – Page 5

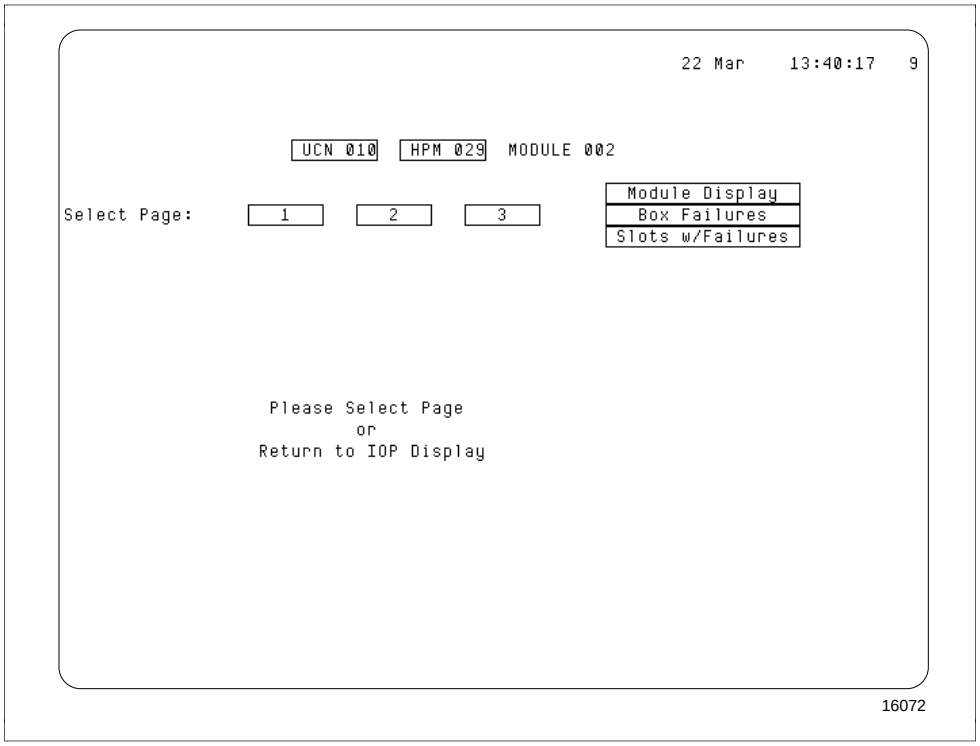


3.4.5.2 IOP Slot Soft Failures Displays

Target selection

The initial IOP Slot Soft Failures display, invoked by selection of the **SLOT SOFT FAILURES** target on the IOP Detail Status display, is shown in Figure 3-61. The display consists of three pages as shown in Figures 3-62 through 3-64. Each failure is described, and when the failure is active, an arrow appears pointing to the failure. Table 4-6 in Section 4 in this manual lists the errors and the suggested corrective actions.

Figure 3-61 IOP Slot Soft Failures Display

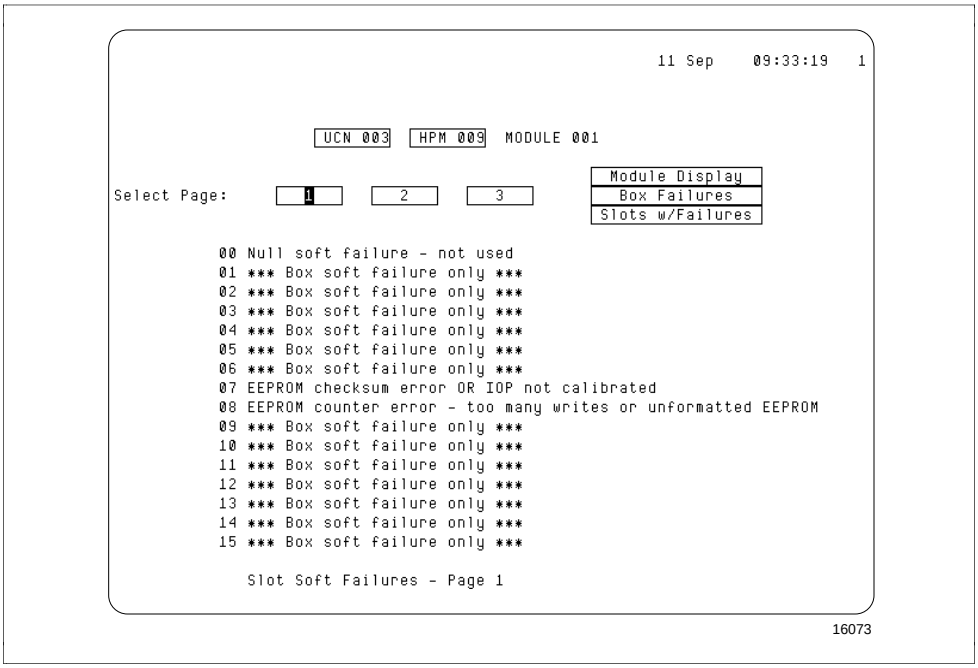


Continued on next page

IOP Slot Soft Failures display – Page 1

Page 1 of the IOP Slot Soft Failures displays is shown in Figure 3-62.

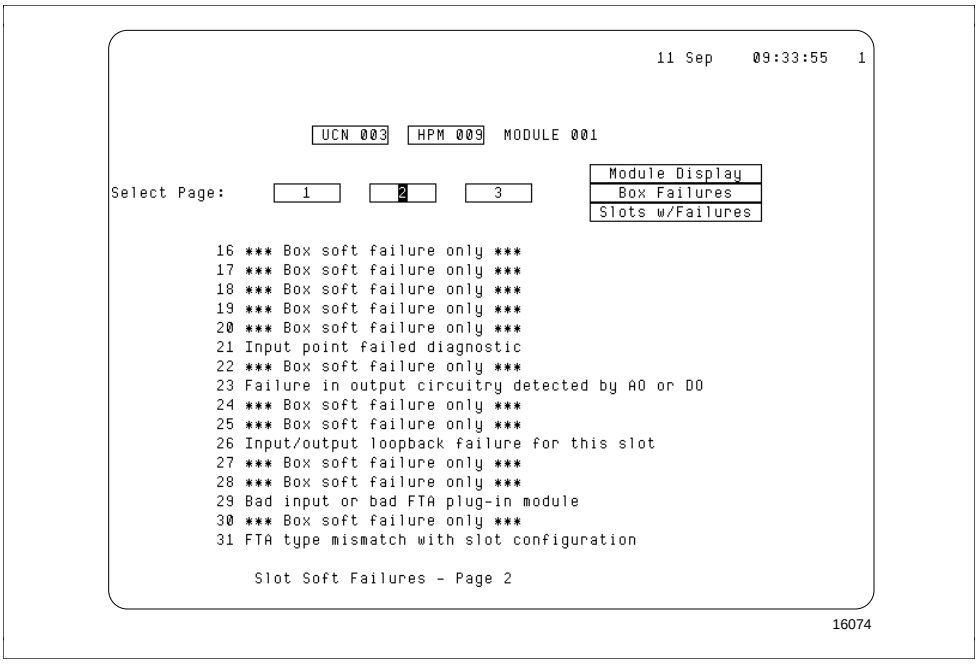
Figure 3-62 IOP Slot Soft Failures Display – Page 1



IOP Slot Soft Failures display – Page 2

Page 2 of the IOP Slot Soft Failures displays is shown in Figure 3-63.

Figure 3-63 IOP Slot Soft Failures Display – Page 2

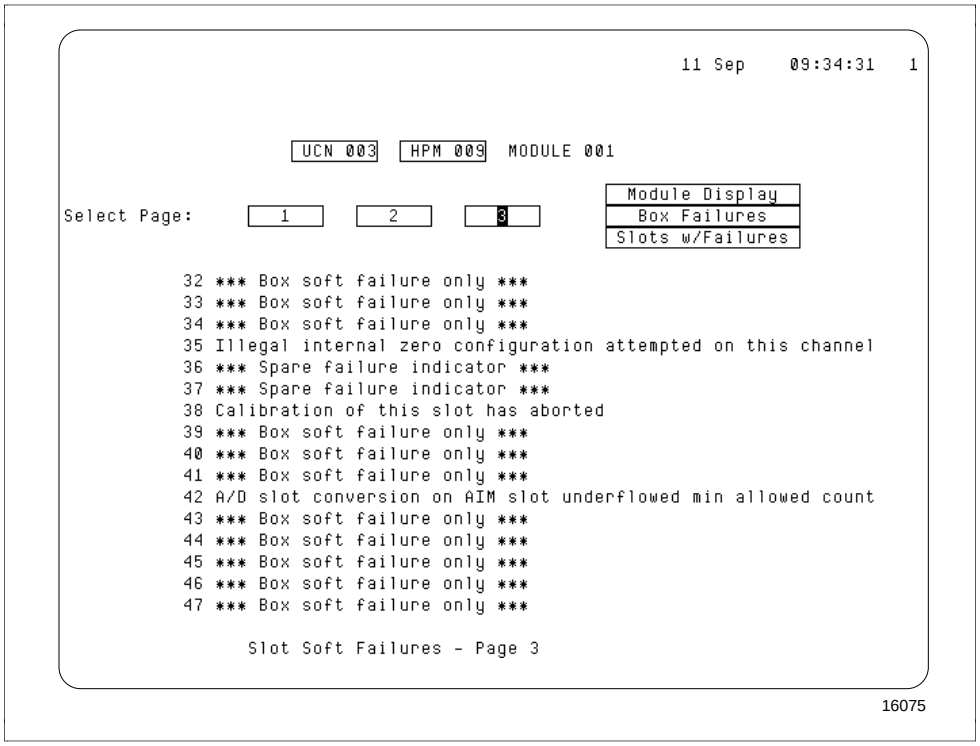


Continued on next page

IOP Slot Soft Failures display – Page 3

Page 3 of the IOP Slot Soft Failures displays is shown in Figure 3-64.

Figure 3-64 IOP Slot Soft Failures Display – Page 3

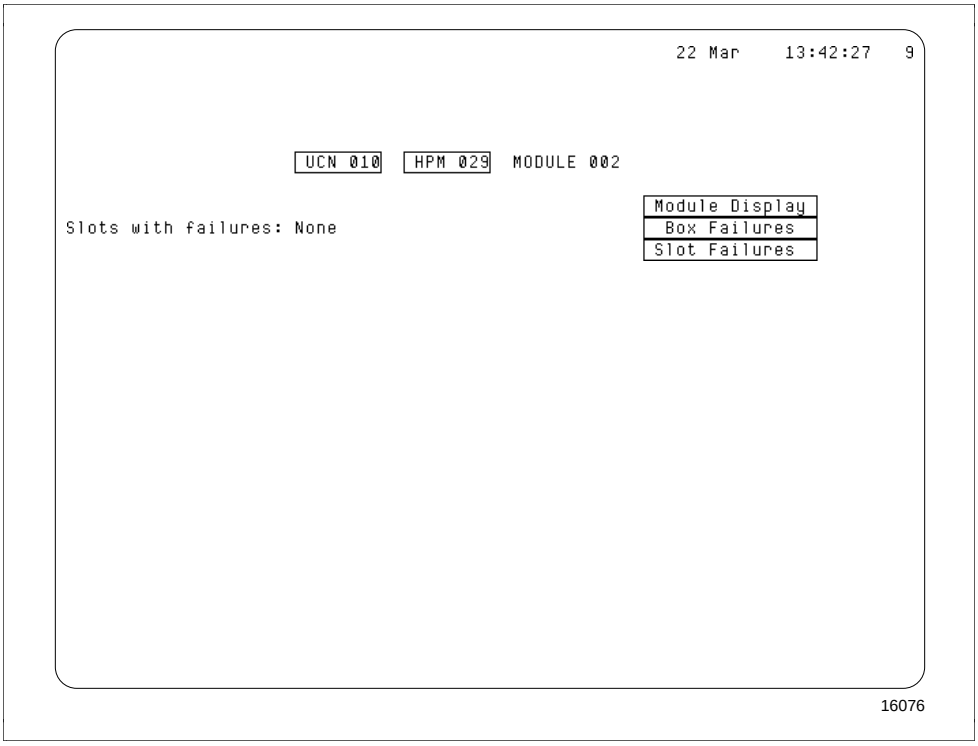


3.4.5.3 IOP Slots with Soft Failures Display

Target selection

The Slots with Soft Failures display, invoked by selection of the **SLOTS WITH SOFT FAILURES** target on the IOP detail Status display, is a single display as shown in Figure 3-65. No failure is displayed as the response **NONE** indicates.

Figure 3-65 IOP Slots with Soft Failures Display



3.4.5.4 HLAI IOP Detail Status Display

IOP calibration

The IOP Detail Status displays for the IOP types that permit calibration of the IOP's A/D or D/A converters (HLAI, LLAI, AO, or LLMux) provide targets to enable/disable the calibration procedure. The calibration procedures are found in Section 8 in this manual.

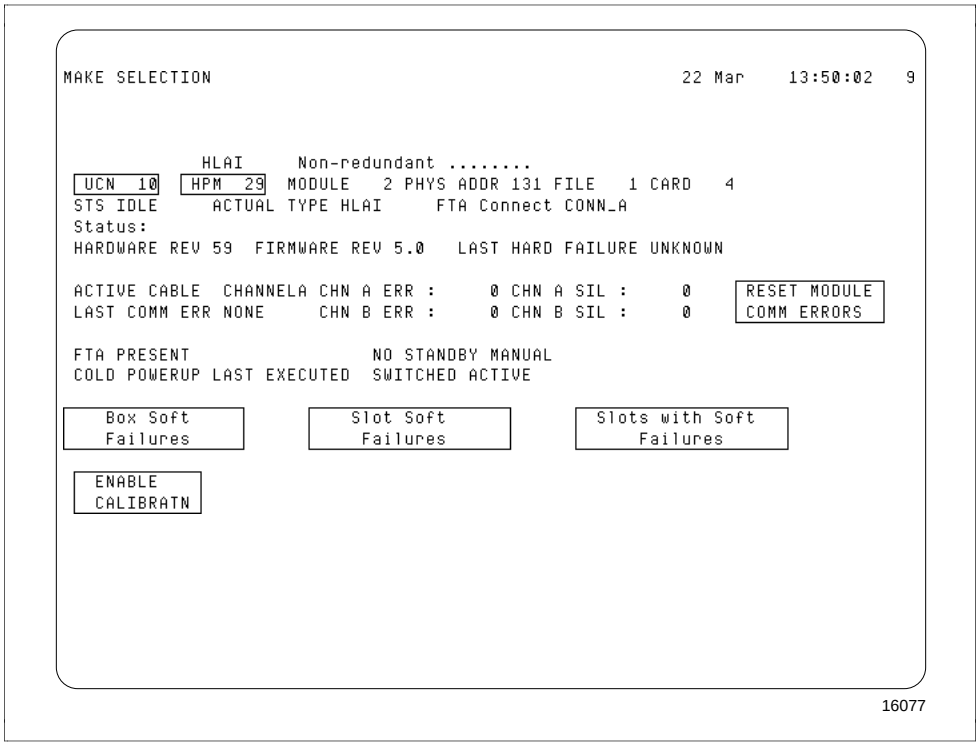
HLAI IOP calibration

The HLAI IOP Detail Status display, as shown in Figure 3-54, is typical of the display for an IOP which is not in an **IDLE** or **IDLESF** (Idle or Idle/Soft Failure) state. Calibration is permitted in only the **IDLE** or **IDLESF** states, as indicated by the "**CALIBRATION NOT PERMITTED, MODULE NOT IN IDLE**" message at the bottom of the display.

ENABLE CALIBRATN target

When the IOP is in the Idle or Idle/Soft Failure state, and not being calibrated, as indicated by a calibration bit resident in the IOP, an **ENABLE CALIBRATN** target appears, indicating that calibration can be initiated as shown in
Figure 3-66.

Figure 3-66 High Level Analog Input IOP Detail Status Display – ENABLE CALIBRATN Target Selected

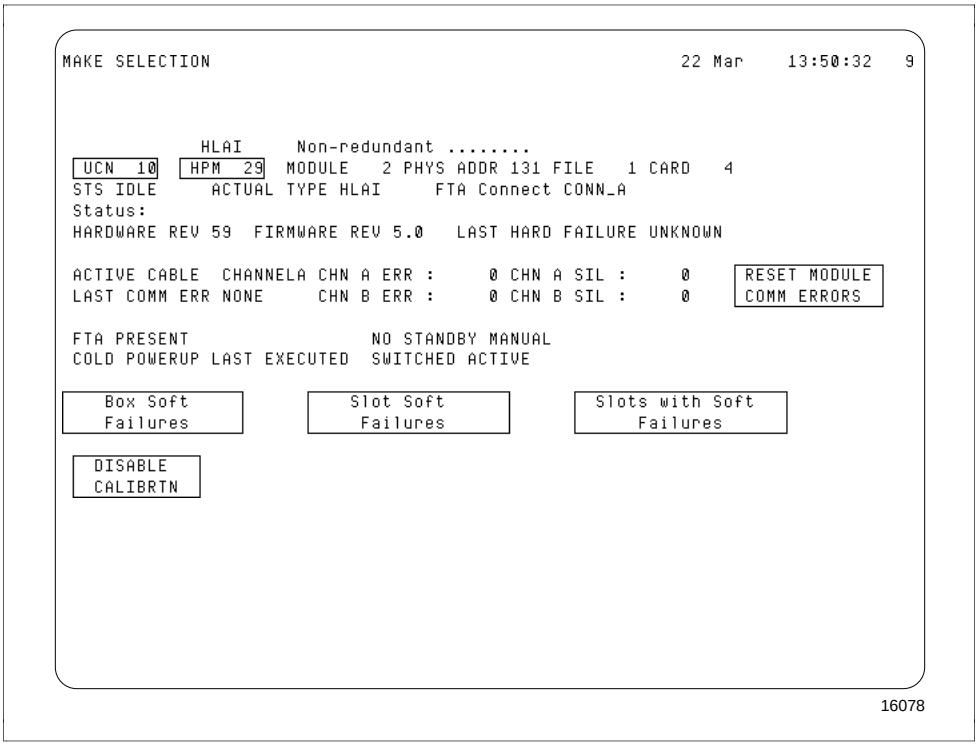


Continued on next page

DISABLE CALIBRATN target

Selection of the **ENABLE CALIBRATN** target sets the calibration bit in the IOP and results in the display that is shown in Figure 3-67. The **DISABLE CALIBRATN** target indicates that calibration is in progress, and that the calibration bit in the IOP can be reset by the operator selecting the **DISABLE CALIBRATN** target.

Figure 3-67 High Level Analog Input IOP Detail Status Display – DISABLE CALIBRATN Target Selected



Calibration bit

The calibration bit can also be reset at the IOP when calibration is complete. Either action will return the IOP to the state that is shown in Figure 3-66.

3.4.5.5 LLAI IOP Detail Status Display

IOP calibration

The LLAI IOP Detail Status display can be used for calibration of the IOP's A/D converters. Targets are provided to enable/disable the calibration procedure. The calibration procedures are found in Section 8 in this manual.

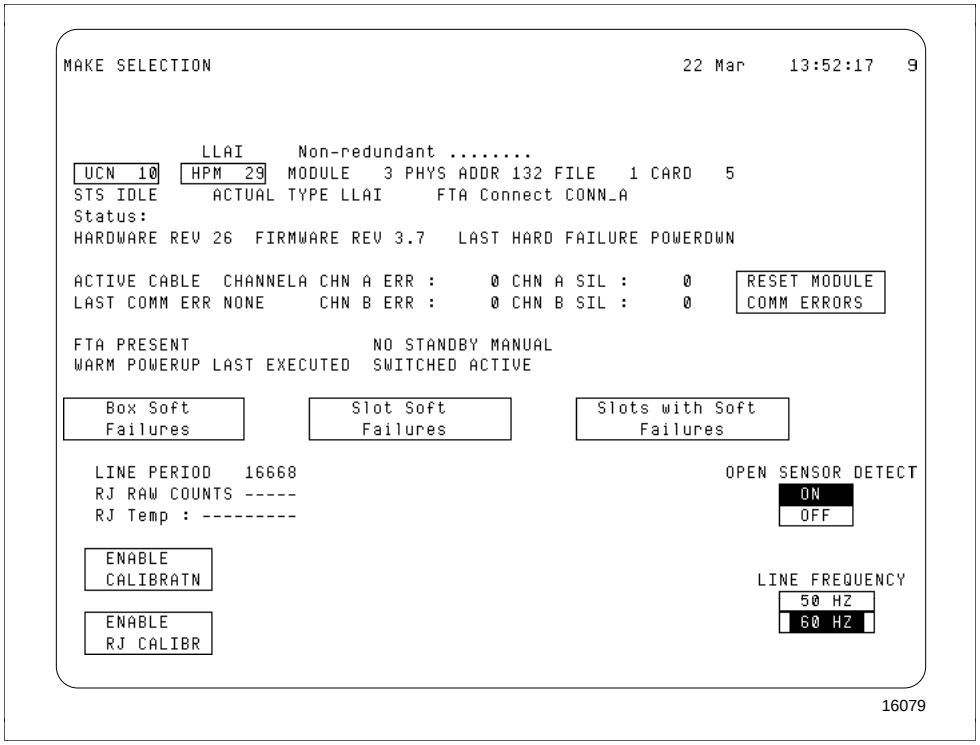
LLAI IOP calibration

There are two types of calibrations possible for the LLAI IOP, A/D Converter calibration and Reference Junction calibration. Figures 3-68 through 3-70 show the calibration targets available for calibration of the LLAI IOP.

ENABLE CALIBRATN and ENABLE RJ CALIBR Targets

Figure 3-68 shows the Low Level Analog Input IOP Detail Status display with the ENABLE CALIBRATN and ENABLE RJ CALIBR targets.

Figure 3-68 Low Level Analog Input IOP Detail Status Display – ENABLE CALIBRATN and ENABLE RJ CALIBR Targets



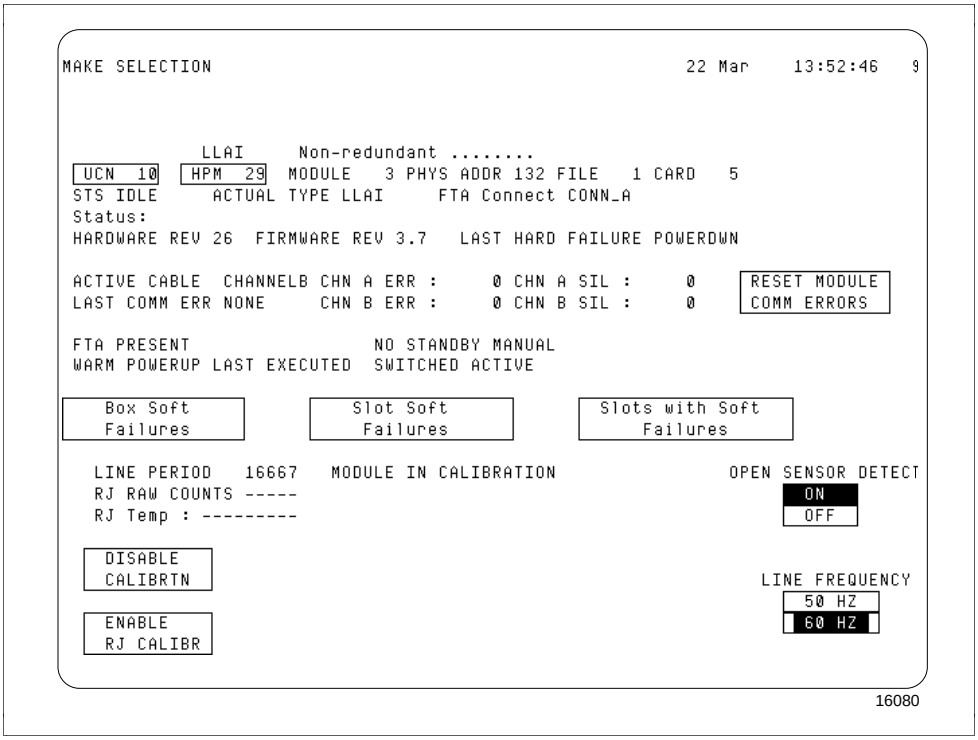
Calibration messages

When either type of calibration is in progress, the message "**MODULE IN CALIBRATION**" or "**RJ IN CALIBRATION**" is displayed to the right of the **LINE PERIOD** data, as shown in Figures 3-69 and 3-70, respectively.

Continued on next page

DISABLE CALIBRATN target

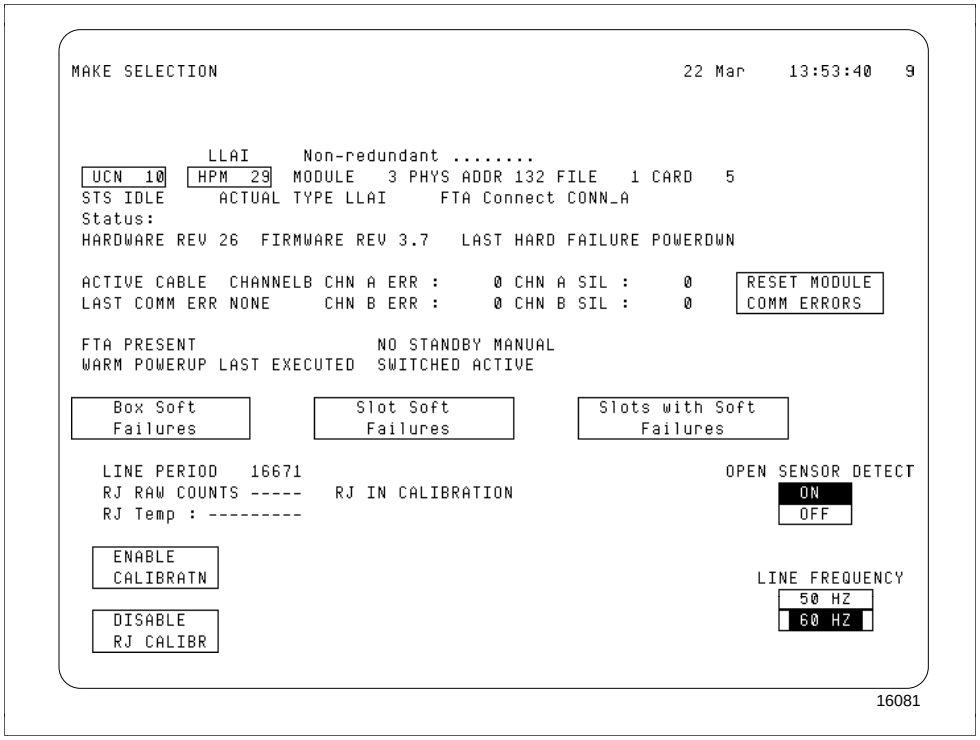
Figure 3-69 Low Level Analog Input IOP Detail Status Display – DISABLE CALIBRATN Target Selected



Continued on next page

DISABLE RJ CALIBR target

Figure 3-70 Low Level Analog Input IOP Detail Status Display – DISABLE RJ CALIBR Target Selected



Continued on next page

3.4.5.5 LLAI IOP Detail Status Display, Continued

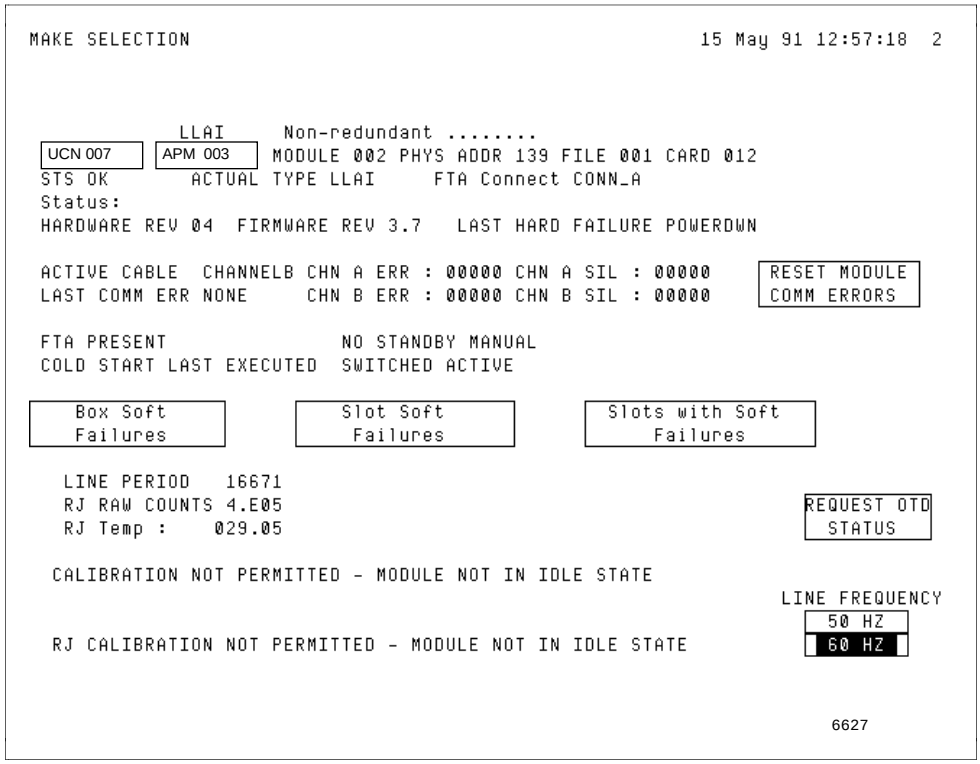
Unique display information

Some of the information provided by an IOP Detail Status display is unique for the type of IOP. The definitions that follow provide information that is unique to the LLAI IOP Detail Status display.

REQUEST OTD STATUS and LINE FREQUENCY targets

The unique portion of the LLAI IOP Detail Status display data and the **REQUEST OTD STATUS** and **LINE FREQUENCY** targets are shown in Figure 3-71.

Figure 3-71 Low Level Analog Input IOP Detail Status Display



Continued on next page

3.4.5.5 LLAI IOP Detail Status Display, Continued

LLAI IOP Detail Status display definitions

The LLAI IOP Detail Status display data and the **REQUEST OTD STATUS** and **LINE FREQUENCY** targets are defined in Table 3-32.

Table 3-32 Low Level Analog Input IOP Detail Status Display

Term	Description
LINE PERIOD	The ac line period in microseconds
RJ RAW COUNTS	The Reference Junction raw count
RJ TEMP	The Reference Junction temperature in degrees centigrade
REQUEST OTD STATUS	When selected, the REQUEST OTD STATUS target, displays the current state of the IOP's Open Thermocouple Detection (OTD) option. If the target is selected, it is replaced with two targets showing the possible OTD states, ON or OFF, with the current state shown in reverse video. If the IOP is in the Idle state, and the Universal Station (US) keyswitch is in the ENGineer position, the state may be changed by selecting the desired target. Any other IOP state or any other keyswitch position will result in an error message.
LINE FREQUENCY	The LINE FREQUENCY target permits selection of 50 Hz or 60 Hz operation. The selection is identified by reverse video.

3.4.5.6 AO IOP Detail Status Display

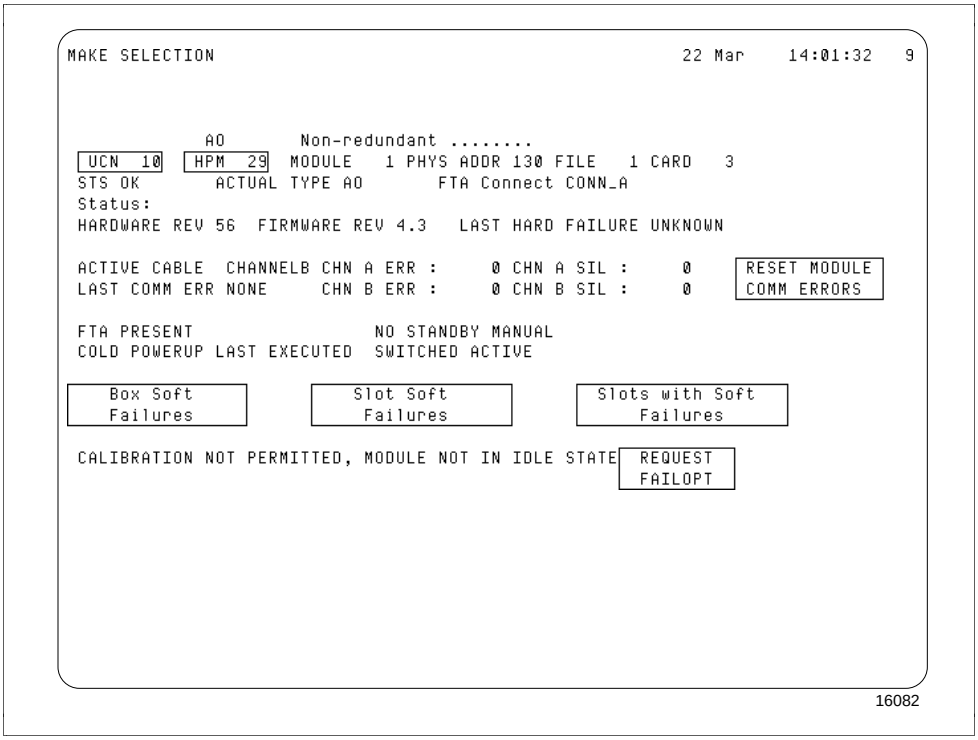
AO IOP Detail Status display

There are two types of Analog Output IOPs and each type accommodates only certain FTA models. Generally, the main difference in the types of AO IOPs is the number of FTA channels that the IOP supports, either 8 or 16 channels. The "High Density" 16-channel IOP display is identified by the term **AO_16** in the first line at the top of the display and after **ACTUAL TYPE** in the third line of the display. The 8-channel IOP display is identified by the term **AO**.

8-channel AO IOP display

Figure 3-72 is an illustration of the 8-channel Analog Output IOP display.

Figure 3-72 8-Channel Analog Output IOP Detail Status Display



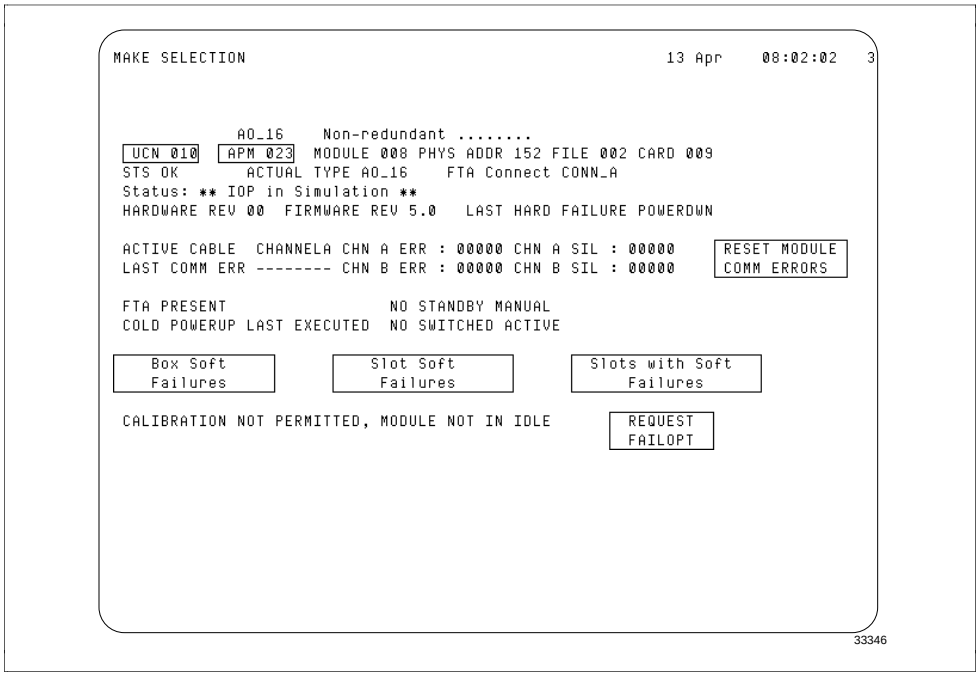
Continued on next page

3.4.5.6 AO IOP Detail Status Display, Continued

16-channel AO IOP display

Figure 3-73 is an illustration of the 16-channel Analog Output IOP display.

Figure 3-73 16-Channel Analog Output IOP Detail Status Display



REQUEST FAILOPT target

Selection of the **REQUEST FAILOPT** target, as shown in Figures 3-72 and 3-73, causes the display to access the current state of the IOP's failure option, parameter **FAILOPT**.

NULL, HOLD, and UNPOWER targets

When the target is selected, it is replaced with three targets showing the possible failure option states, **NULL**, **HOLD** and **UNPOWER**, with the current state in reverse video. If the Universal Station keyswitch is in the **ENG**ineer position, the state may be changed to **HOLD** or **UNPOWER**, by selecting the desired target. Any other IOP state, or any other keyswitch position, or selection of the **NULL** target will result in an error message.

Idle or OK state

If the IOP is in the Idle or OK state and the Universal Station keyswitch is in the **ENG**ineer position, the failure option can be changed to **HOLD** or **UNPOWER**, by selecting the appropriate target. Any other IOP state, any other keyswitch position, or selection of the **NULL** target will result in an error message.

NULL target

The **NULL** failure option can be selected only by placing the IOP in the Idle state, reconstituting the HPM box configuration, selecting the **NULL** failure state, and then reloading.

Continued on next page

3.4.5.6 AO IOP Detail Status Display, Continued

PRIMARY IOP STATUS and SECONDARY IOP STATUS targets

The AO IOP can exist as a redundant configuration. The **SECONDARY IOP STATUS** and **PRIMARY IOP STATUS** targets provide a means of selecting either the primary or secondary IOP displays. Each display has a unique message. The primary display can display the message "**CALIBRATION NOT PERMITTED**, **MODULE NOT IN IDLE**." The secondary display has the message "**SECONDARY IOP**, **CALIBRATION NOT PERMITTED**."

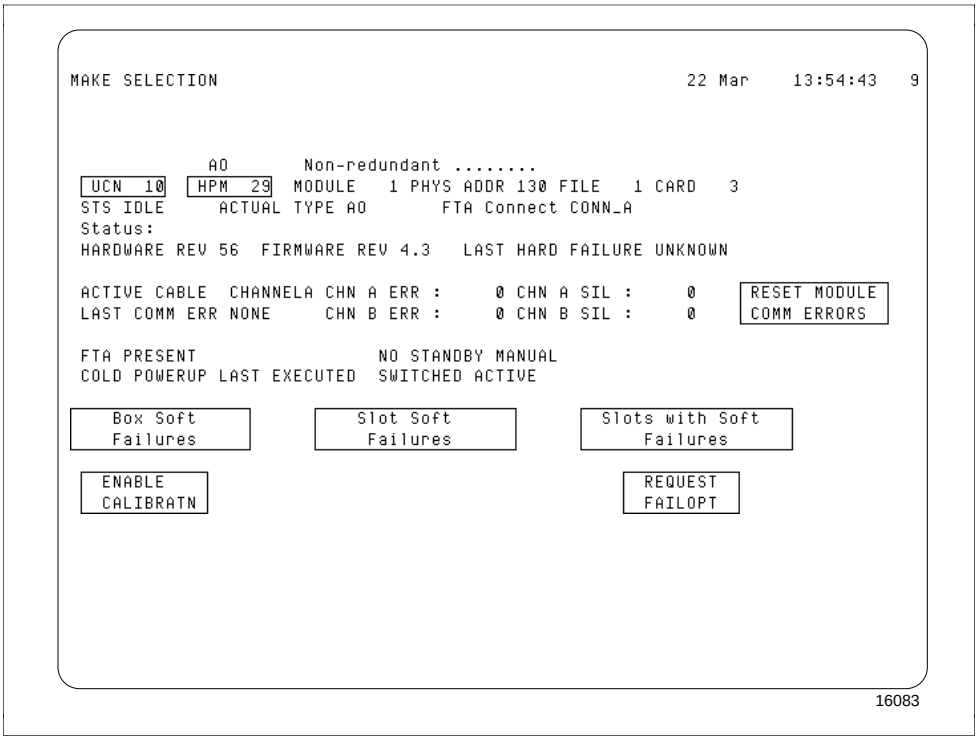
IOP calibration

The AO IOP Detail Status display can be used for calibration of the IOP's D/A converters. Targets are provided to enable/disable the calibration procedure. The calibration procedures are found in Section 8 in this manual.

AO IOP calibration

Figures 3-74 and 3-75 show the targets available for calibration of the Analog Output (AO) IOP. Selecting the **ENABLE CALIBRATN** target initiates the calibration procedure, while selecting the **DISABLE CALIBRATN** target terminates the procedure.

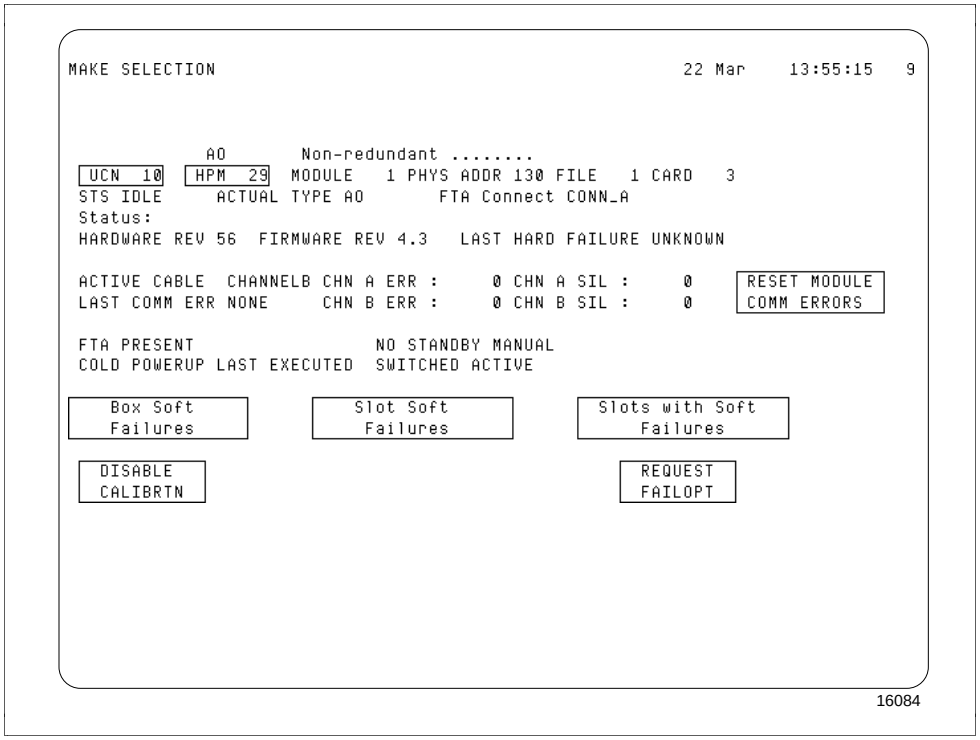
Figure 3-74 Analog Output IOP Detail Status Display – ENABLE CALIBRATN Target Selected



Continued on next page

DISABLE CALIBRATN target

Figure 3-75 Analog Output IOP Detail Status Display – DISABLE CALIBRATN Target Selected



3.4.5.7 LLMux IOP Detail Status Display

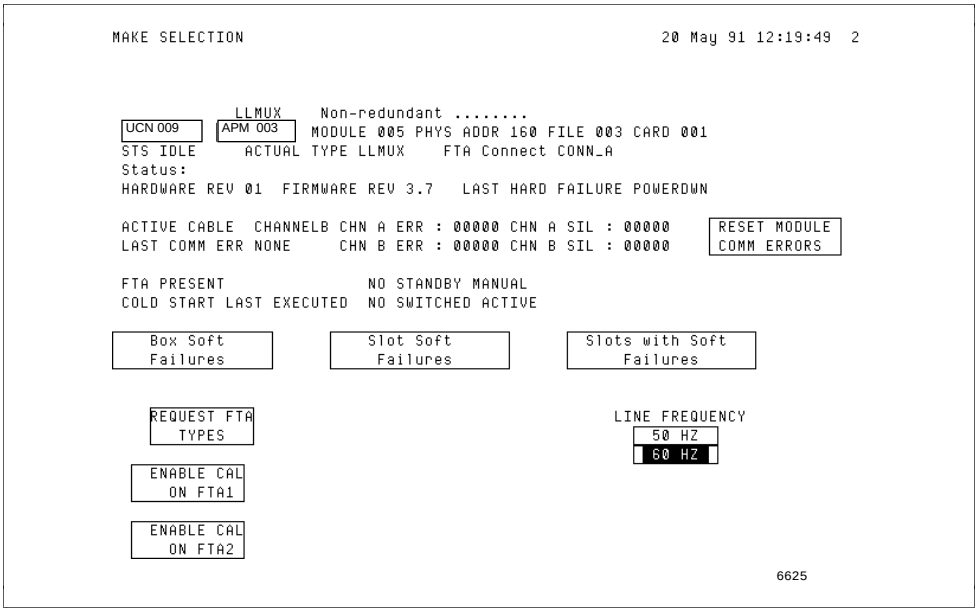
IOP calibration

The LLMux IOP Detail Status display can be used for calibration of the IOP's A/D converters. Targets are provided to enable/disable the calibration procedure. The calibration procedures are found in Section 8 in this manual.

LLMux IOP calibration

Figures 3-76 and 3-77 show the targets available for calibration of the Low Level Multiplexer (LLMux) IOP. Selecting either the **ENABLE CAL ON FTA1** or **ENABLE CAL ON FTA2** target initiates the calibration procedure, while selecting the **DISABLE CAL ON FTA1** or **DISABLE CAL ON FTA2** target terminates the procedure.

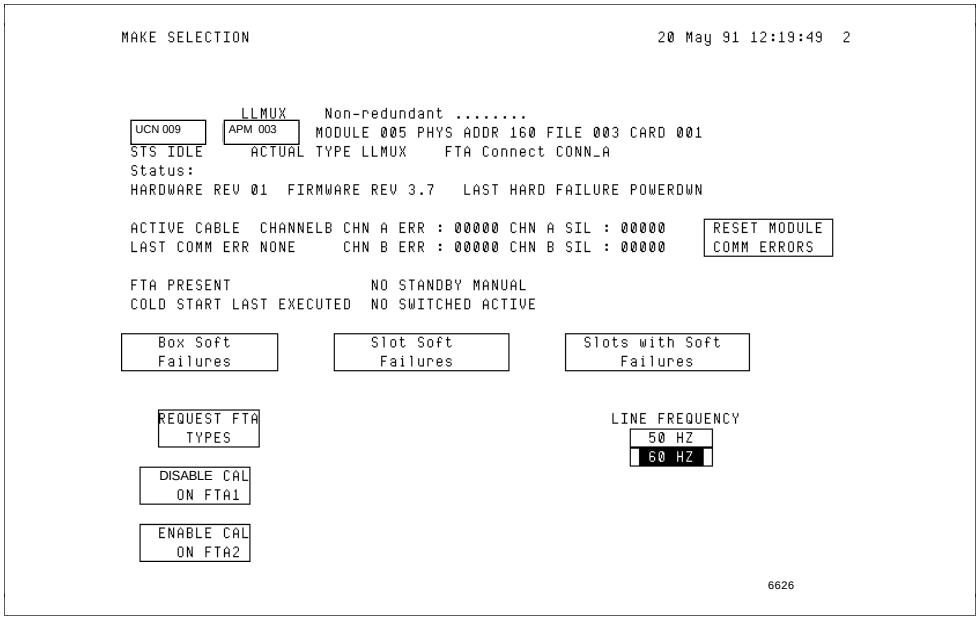
Figure 3-76 LLMux IOP Detail Status Display – ENABLE CAL ON Target Selected



Continued on next page

DISABLE CALIBRATN target

Figure 3-77 LLMux IOP Display – DISABLE CALIBRATN Target Selected



Unique display information

Some of the information provided by an IOP Detail Status display is unique for the type of IOP. The definitions that follow provide information that is unique to the LLMux IOP Detail Status display.

Continued on next page

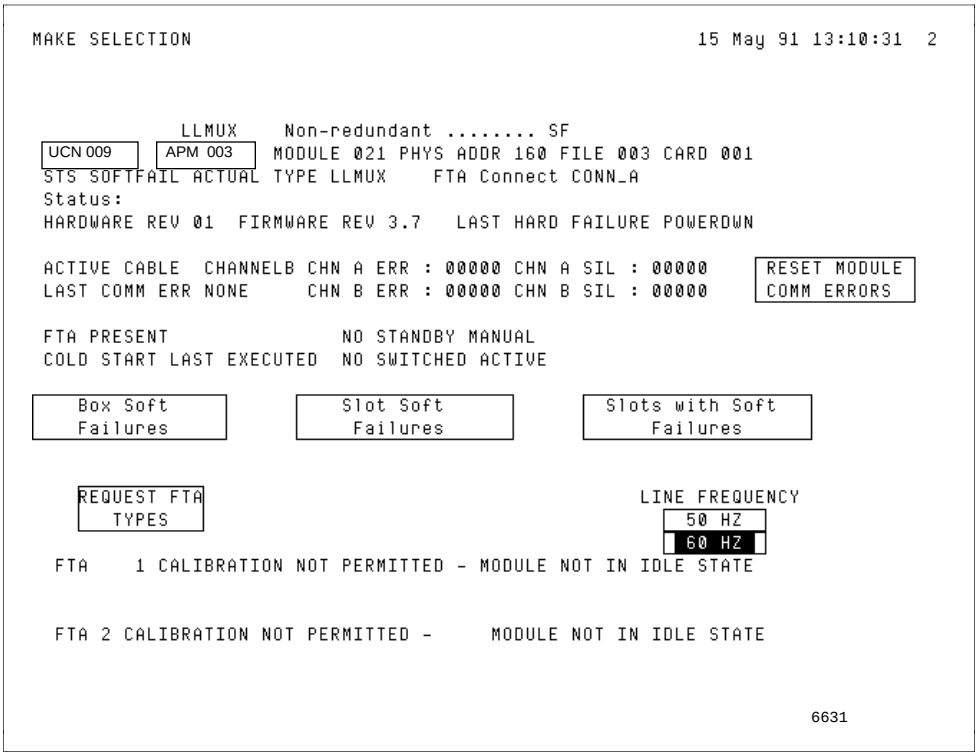
3.4.5.7 LLMux IOP Detail Status Display, Continued

Unique LLMux IOP Detail Status targets

The LLMux IOP Detail Status display has unique data and targets as shown in Figure 3-78. The **REQUEST FTA TYPE** target provides a means of identifying the type of FTA, thermocouple (TC) or Resistive Temperature Device (RTD), that is attached to each Power Adapter channel. Selecting the target produces status displayed as **FTA 1 TYPE** and **FTA 2 TYPE** with the type of FTA attached to each channel.

Another target is the **LINE FREQUENCY** target which permits selection of 50 Hz or 60 Hz operation. The selection is identified by reverse video.

Figure 3-78 Low Level Multiplexer IOP Detail Status Display



Continued on next page

3.4.5.8 DI IOP Detail Status Display

Overview

There are two types of Digital Input IOPs and each type accommodates only certain FTA models. Both types of DI IOPs support 32 FTA channels. The "High Density" 32-channel IOP display is identified by the term **DI24V** in the first line at the top of the display and after **ACTUAL TYPE** in the third line of the display. The other 32-channel IOP display is identified by the term **DI**.

Unique display information

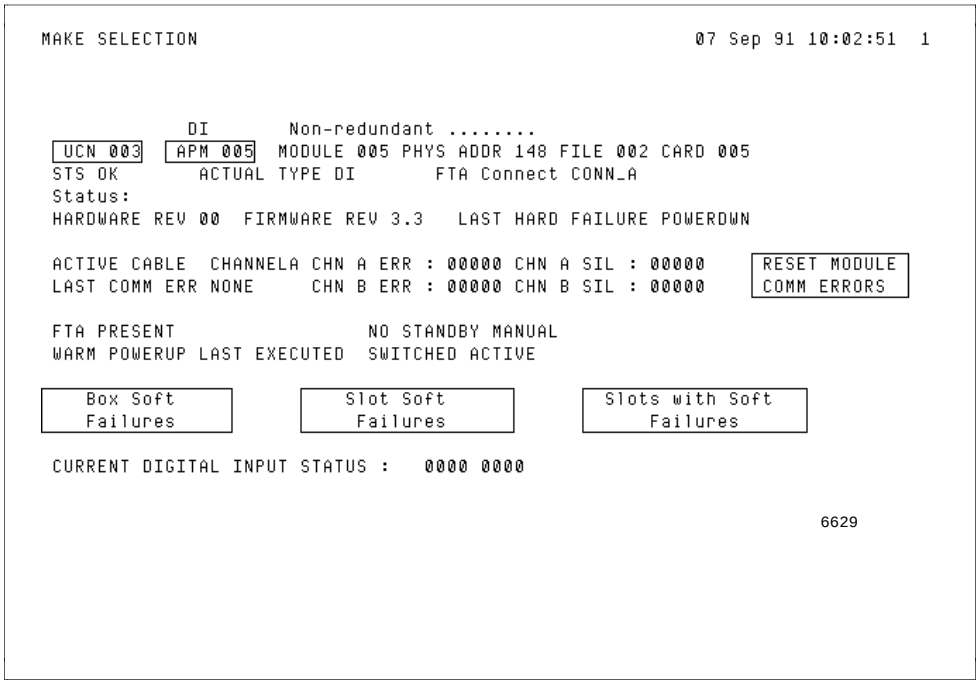
Some of the information provided by an IOP Detail Status display is unique for the type of IOP. The definition that follows provides information that is unique to the DI IOP Detail Status display.

DI IOP Detail Status display

As shown in Figure 3-79, the Digital Input IOP Detail Status display has one unique status.

The **CURRENT DIGITAL INPUT STATUS** data is represented by two hexadecimal words showing the current state of the 32 digital inputs. Input slot 1 is the high order bit in the left-hand word of the data pair.

Figure 3-79 Digital Input IOP Detail Status Display



3.4.5.9 DO IOP Detail Status Display

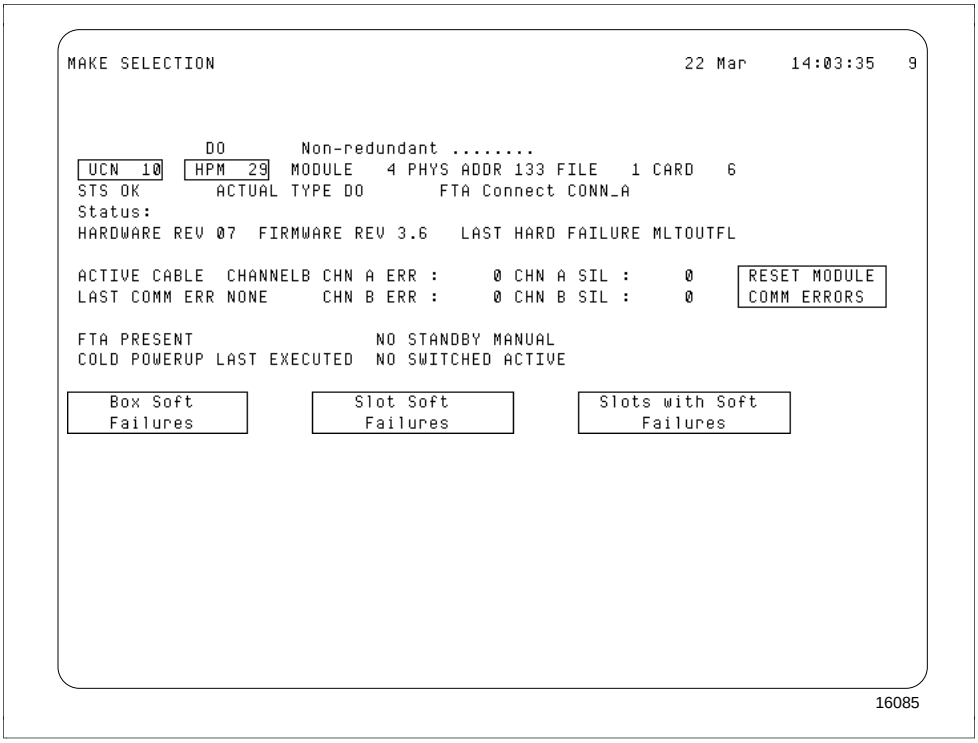
Overview

There are two types of Digital Output IOPs and each type accommodates only certain FTA models. Generally, the main difference in the types of DO IOPs is the number of FTA channels that the IOP supports, either 16 or 32 channels. The “High Density” 32-channel IOP display is identified by the term **DO_32** in the first line at the top of the display and after **ACTUAL TYPE** in the third line of the display. The 16-channel IOP display is identified by the term **DO**.

16-channel DO IOP display

Figure 3-80 is an illustration of the 16-channel Digital Output IOP display.

Figure 3-80 16-Channel Digital Output IOP Detail Status Display



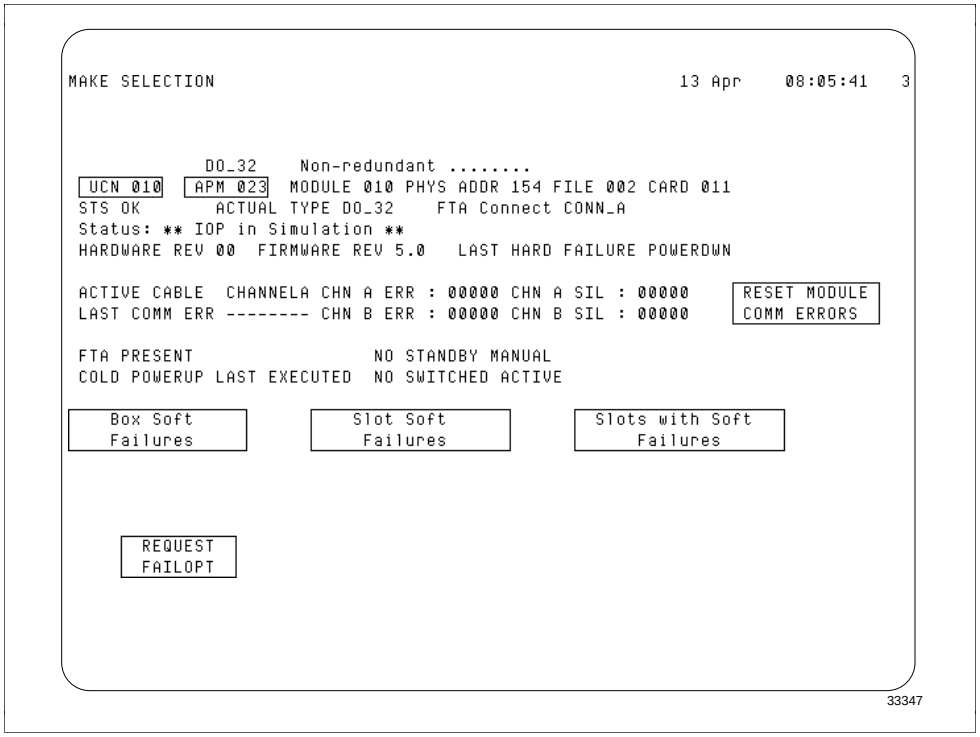
Continued on next page

32-channel DO IOP display

The 32-channel Digital Output IOP display also has an additional display line, the sixth line. The line contains a description of the type of Digital Output FTA that is associated with the IOP. After **IOP DESCRIPTION**, either the term **24V** or **240V** will be displayed. The term **24V** indicates a model MU-TDOY22/62 FTA is connected to the IOP, and the term **240V** indicates a model MU-TDOY22/62 FTA is connected.

Figure 3-81 is an illustration of the 32-channel Digital Output IOP display.

Figure 3-81 32-Channel Digital Output IOP Detail Status Display



Similar to AO IOP display

The Detail Status display for the Digital Output IOP is similar to the display shown for the Analog Output IOP. See the Analog Output IOP display discussion for details.

3.4.5.10 STI/STIM IOP Detail Status Display

Unique display information

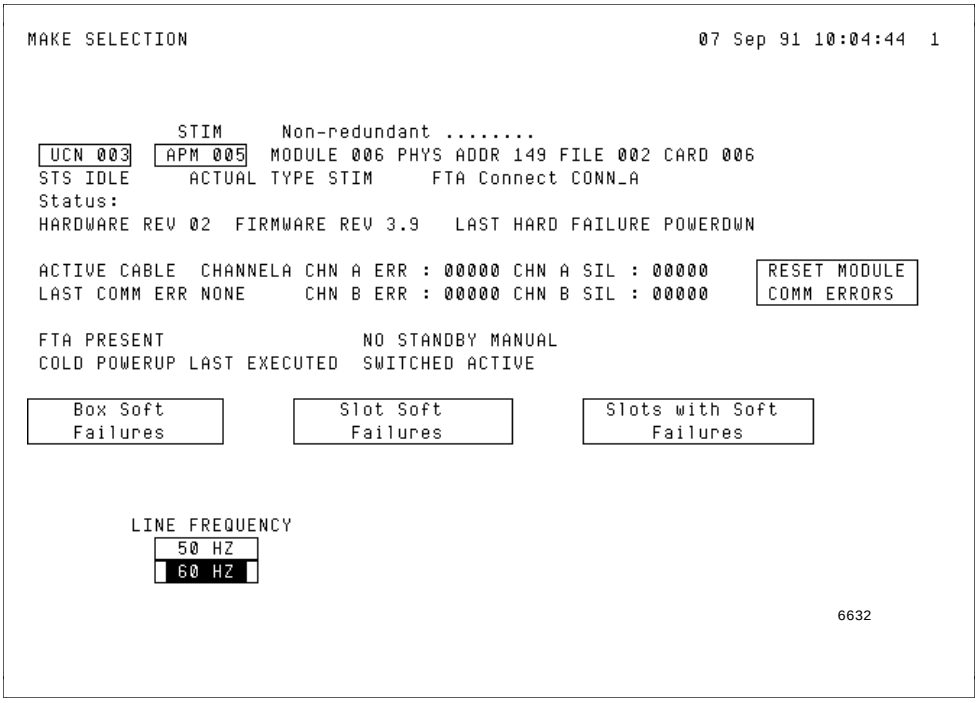
Some of the information provided by an IOP Detail Status display is unique for the type of IOP. The definition that follows provides information that is unique to the STI/STIM IOP Detail Status display.

STIM IOP Detail Status display

The unique data on the Smart Transmitter Interface IOP Detail Status display consists of a single target as shown in Figure 3-82.

The **LINE FREQUENCY** target permits selection of 50 Hz or 60 Hz operation. The selection is identified by reverse video.

Figure 3-82 Smart Transmitter Interface IOP Detail Status Display



3.4.5.11 PI IOP Detail Status Display

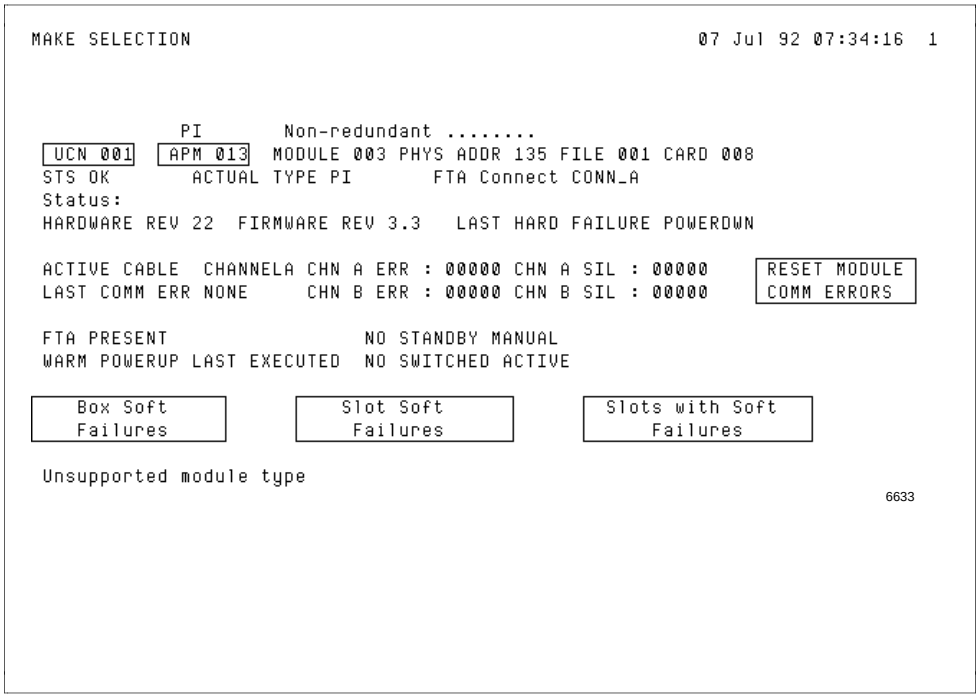
Unique display information

Some of the information provided by an IOP Detail Status display is unique for the type of IOP.

PI IOP Detail Status display

As shown in Figure 3-83, the Pulse Input IOP Detail Status display has no unique status information or targets.

Figure 3-83 Pulse Input IOP Detail Status Display



3.4.5.12 SDI IOP Detail Status Display

Unique display information

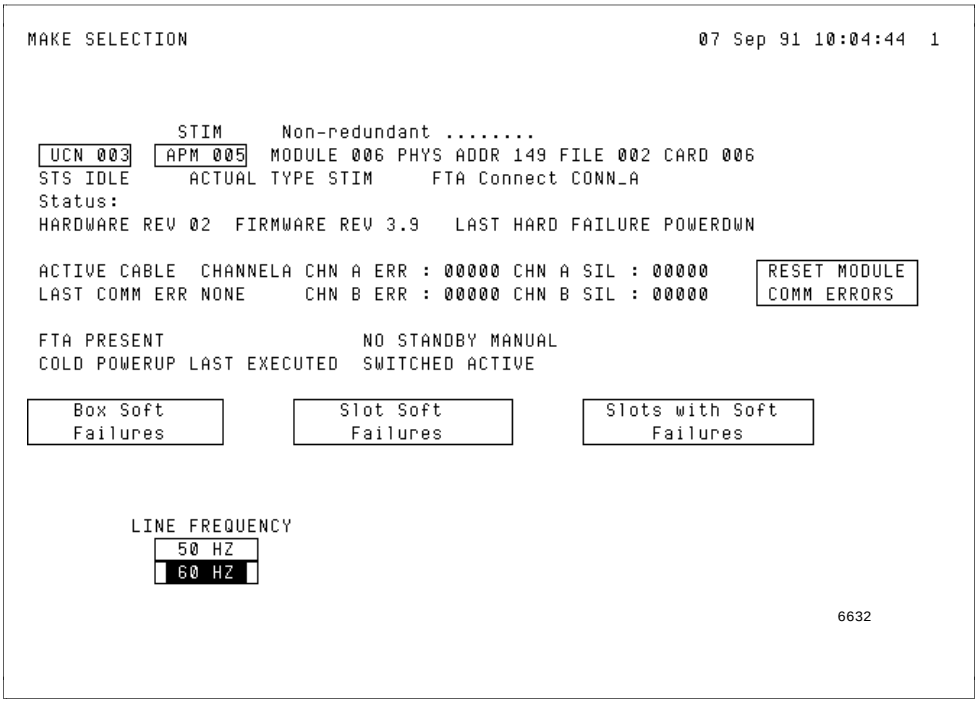
Some of the information provided by an IOP Detail Status display is unique for the type of IOP. The definitions that follow provide information that is unique to the SDI IOP Detail Status display.

SDI IOP Detail Status display

As shown in Figure 3-84, the unique portion of the Serial Device Interface IOP Detail Status display consists of a single target. Its purpose is the same as the Smart Transmitter Interface IOP Detail Status display.

The **LINE FREQUENCY** target permits selection of **50 HZ** or **60 HZ** operation. The selection is identified by reverse video.

Figure 3-84 Serial Device Interface IOP Detail Status Display



3.4.5.13 SI IOP Detail Status Display

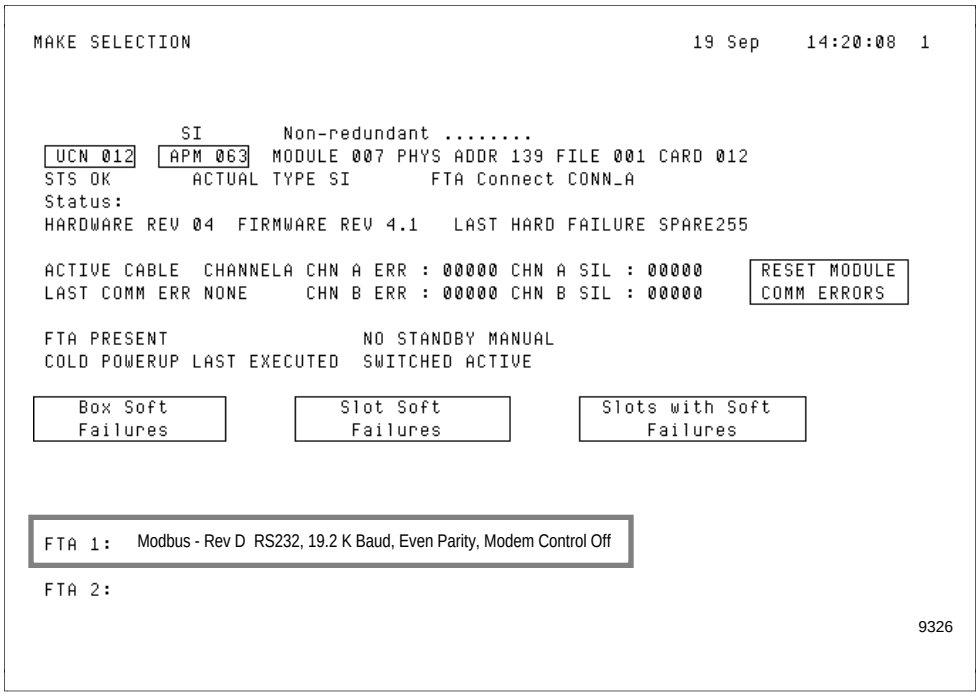
Unique display information

Some of the information provided by an IOP Detail Status display is unique for the type of IOP. The definitions that follow provide information that is unique to the SI IOP Detail Status display.

SI IOP Detail Status display

As shown in Figure 3-85, the unique portion of the Serial Interface IOP Detail Status display consists of **FTA 1** and **FTA 2** status information.

Figure 3-85 Serial Interface IOP Detail Status Display



3.4.5.14 DISOE IOP Detail Status Display

Unique display information

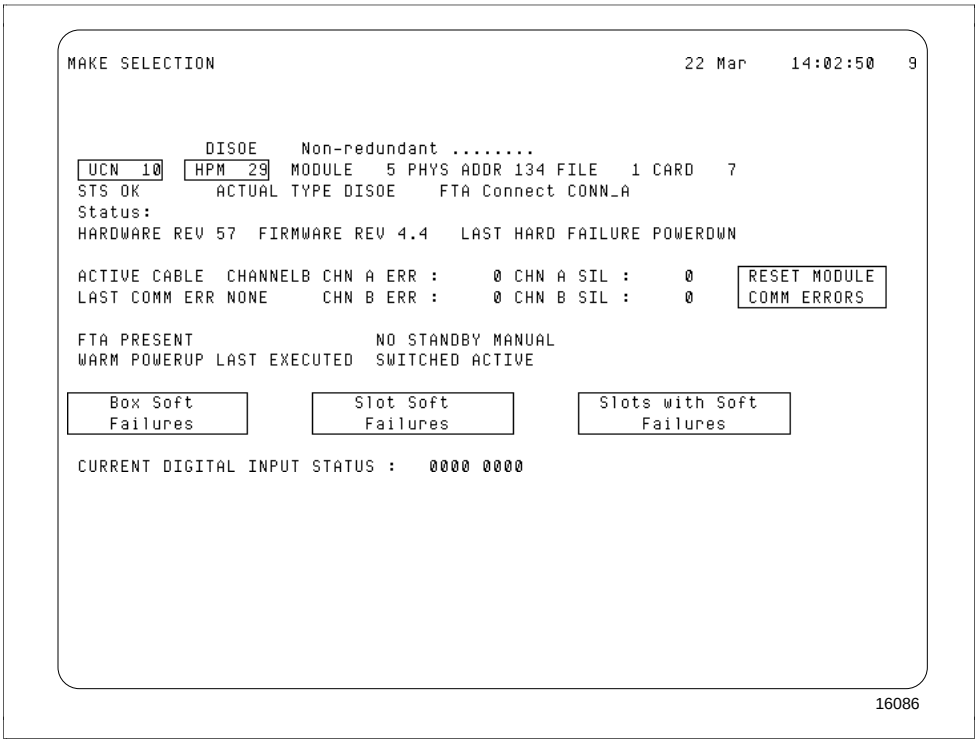
Some of the information provided by an IOP Detail Status display is unique for the type of IOP. The definition that follows provides information that is unique to the DISOE IOP Detail Status display.

DISOE IOP Detail Status display

As shown in Figure 3-86, the Digital Input Sequence of Events IOP Detail Status display has one unique status.

The **CURRENT DIGITAL INPUT STATUS** data is represented by two hexadecimal words showing the current state of the 32 digital inputs. Input slot 1 is the high order bit in the left-hand word of the data pair.

Figure 3-86 Digital Input Sequence of Events IOP Detail Status Display



Section 4 – Fault Isolation

4.1 Overview

Section contents

The topics covered in this section are:

	Topic	See Page
4.1	Overview	231
4.2	Failure Types	232
4.3	Fault Isolation Concepts	235
4.3.1	Troubleshooting Flow Chart	237
4.3.2	HPMM Corrective Actions (Table 4-1)	243
4.3.3	Comm/Control Hard Failure Codes (Table 4-2)	245
4.3.4	HPMM Soft Failure Codes (Table 4-3)	268
4.3.5	I/O Link Hard Failure Codes (Table 4-4)	273
4.3.6	IOP Hard Failure Codes (Table 4-5)	275
4.3.7	IOP Box Soft Failure Codes (Table 4-6)	277
4.3.8	IOP Slot Soft Failure Codes (Table 4-7)	283
4.4	Smart Transmitter Interface	285
4.5	FTA Redundancy Indicators	286
4.6	Redundant Analog Output IOP Failure Diagnosis	287
4.7	Battery Backup Exhaustion	290
4.8	HPMM Card and Module Indicators	290
4.9	HPMM Alphanumeric Display	294
4.9.1	Alphanumeric Display Format	295
4.9.2	Notification Displays	298
4.9.3	Cold HPMM Startup Display Sequences	299
4.9.4	Load Display Sequence	302
4.9.5	Nonredundant HPM Failure Sequences (After Load)	304
4.9.6	RAM Retention Startup Sequence	306
4.9.7	Redundancy Display Sequences	307
4.9.8	HPMM Alphanumeric Display Blanking	311
4.9.9	Listing of Diagnostic Tests	312
4.10	I/O Card Indicators	320
4.11	FTA Indicators	322
4.12	Power System Indicators	324
4.12.1	Standard Power System	324
4.12.2	AC Only Power System	327
4.13	Power System Voltage Checks	328
4.13.1	Standard Power System	328
4.13.2	AC Only Power System	331

CAUTION

CAUTION—The yellow-colored “Voltage Margin” jumper plug that is located in the area behind the bezel door at the front of the High-Performance I/O Link card must always be in the **Normal** (+5 vdc) position during normal operation. The jumper plug must never be removed or moved to the **Low Margin** or **High Margin** position while on-control. An HPMM Soft failure will be reported if it is not in the **Normal** position.

Continued on next page

4.1 Overview, Continued

Purpose

This section provides the information required for HPM fault isolation (troubleshooting). It includes a troubleshooting flow chart that guides the user through isolating faults in the HPM It also provides the user with fault code tables, which include a description of the fault and the recommended corrective action(s) to resolve the problem.

Release 500 software displays

The displays shown in this section are reproductions of console screens created by Release 500 software.

4.2 Failure Types

Two types of failures

There are two general types of failures that can occur in the High-Performance Process Manager, "Hard failures" and "Soft failures."

Hard failure

A Hard failure causes an HPMM or IOP to enter a predefined failure state. While in this failed state, the module cannot perform its normal functions and will be in a reset condition (IOPs) or executing a "failure" program (HPMM).

Soft failure

A Soft failure allows a card to continue operating in its current state (OK or Idle), but its operation is degraded. The level of degraded operation could be insignificant or significant, depending on the nature of the Soft failure. Some Soft failures can automatically clear (clearing is done by the HPMM or IOP without intervention), other Soft failures require manual intervention for resolution.

Hard and Soft failures

Both the Hard and Soft failure types are described below.

HPM failure

An HPM failure indicates that a HPMM Hard failure, as described below, has occurred in an HPM. The HPMM cannot control the process or act as a redundant partner because of the nature of the fault in the HPMM. The four types of Hard failures that cause the HPMM to fail are indicated by a status of **FAIL** in the HPM Box (grid) on the UCN Status display.

Continued on next page

HPMM Hard failure

An HPMM Hard failure forces the HPMM into the **FAIL** state. In this state, the HPMM executes only from its failure executive and acts only as a responder on the UCN. Note that if there is a fault in the High-Performance Comm/Control or the High-Performance I/O Link card in the primary HPMM, and the HPMM is redundant, the faulty HPMM enters the **FAIL** state and the HPM operations switch to the redundant partner HPMM.

If an HPMM does not have a redundant partner and a Hard failure occurs in the control processor on the High-Performance Comm/Control card, the communications processor on the High-Performance Comm/Control card annunciates the appropriate Hard failure code, and the HPMM degrades to the Soft failure state. In this case, no control execution is being performed, but the LCN/UCN view to the IOPs is maintained.

An HPMM Hard failure is indicated by a **FAIL** status on the HPMM Detail Status display. It is also visible as a **Fxxx** state in the HPMM alphanumeric display window. HPMM Hard failure error codes are indicated on the HPMM Detail Status displays for the High-Performance Comm/Control and High-Performance I/O Link card processors. These same Hard failure error codes are also available through the appropriate use of the HPMM alphanumeric display and its associated display switch behind the bezel door at the front of the High-Performance Comm/Control card.

HPM Partial failure

In most cases, an HPM Partial failure indicates that a minor fault has been detected in an HPM, and the HPM continues to control the process. A Partial failure can be caused by an HPMM Soft failure, IOP Hard failure, or an IOP Soft failure as described below. The HPMM Partial failure is indicated by a status of **PARTFAIL**, **PF_IDLE**, **PF_IOIDL**, or **BKUP_PF** on the UCN Status display. The **PF_IDLE** and **PF_IOIDL** Partial failures indicate that a Partial failure was detected while the HPMM, or at least one of the IOPs, is in the idle condition. Some Partial failures may cause failover between redundant HPMMs, while others can cause redundant IOP failover.

HPMM Soft failure

In most cases, an HPMM Soft failure indicates that a minor fault, such as a timeout or overflow condition, has been detected in the internal diagnostics, or that a parity checker has failed. The HPMM Soft failures appear in system event messages and on the HPMM Detail Status display. More detailed information is available when the **SOFT FAILURE** target on the HPMM Maintenance Support display is selected. Note that a Control processor Hard failure on the High-Performance Comm/Control card in a nonredundant HPMM appears as a **SOFTFAIL** on the display, even though this is a major failure and control is interrupted.

Continued on next page

IOP Hard failure

An IOP Hard failure indicates that a Hard failure has occurred in an IOP card. The background (embedded in the operating personality) internal diagnostics in an IOP card are used to test the card's functions and report the status of the IOP, using Hard and Soft failure error codes. When a Hard failure occurs, the IOP card fails (stops operations), and its status becomes **NR** (No Response).

The only possible recovery from this type of failure is to recycle power on the failed IOP by unlocking and lifting/lowering the upper card lever. If the failure still exists, the IOP will fail again.

Restart of an output IOP after a power loss (or manual power recycle) results in analog output channels going to a nonpowered state, and digital output channels are set to off. Reloading of the IOP data base is then required.

IOP Soft failure

An IOP Soft failure indicates that a Soft failure, such as an single slot/channel input/output failure, has been detected in an IOP card by the IOP's internal diagnostics. The IOP Soft failures appear in system event messages and on the IOP Detail Status display.

IOP Soft failures are grouped into two categories. IOP Box Soft failures are failures that affect all slots/channels in the IOP. IOP Slot Soft failures are failures that affect one or more but not all slots/channels in the IOP.

4.3 Fault Isolation Concepts

Introduction

The first step in fault isolation is to determine whether the fault exists in a field device, or in the High-Performance Process Manager. After it has been determined that the fault is in the High-Performance Process Manager, you can begin isolating the fault by using the information provided in this section.

Troubleshooting flowcharts

A flowchart to assist you in isolating off-process and on-process faults to specific High-Performance Process Manager components is shown in Figures 4-1 through 4-6. The flowcharts encourage the following troubleshooting philosophy.

- Use the flowchart to lead you through the available High-Performance Process Manager status and alphanumeric displays so you can identify the type of fault and the associated error code. This is the next step in fault isolation.
- The flowchart will point you to a table in this section that lists and describes the error codes, along with the recommended corrective action(s).
- The recommended corrective action usually identifies the most likely cause of the error condition. In some cases more than one corrective action is given. In these cases, the action listed first is the most probable fix. The remaining actions should be attempted in sequence if the problem is not resolved. If the fault is not eliminated by the recommended corrective action(s), then you should pursue other causes, such as checking for faulty cabling, improper or faulty FTA connections, improper system installation (especially power and grounding), and potential harmful transient conditions, such as Electrostatic Discharge (ESD) or Radio Frequency Interference (RFI).

Recommendations for Operators and Service Technicians

The flowchart shown in Figures 4-1 through 4-6 has been developed for use by both a Universal Station (US) Operator and the Service Technician. The flowchart shows the Operator how to use the displays to locate the error code. When the error code is identified, the Service Technician can begin to further define/resolve the fault by using the error code tables and associated corrective action recommendations.

After a fault has been isolated to a particular High-Performance Process Manager subassembly, refer to Section 7 in this manual for the applicable removal and replacement procedures.

Continued on next page

Troubleshooting table usage

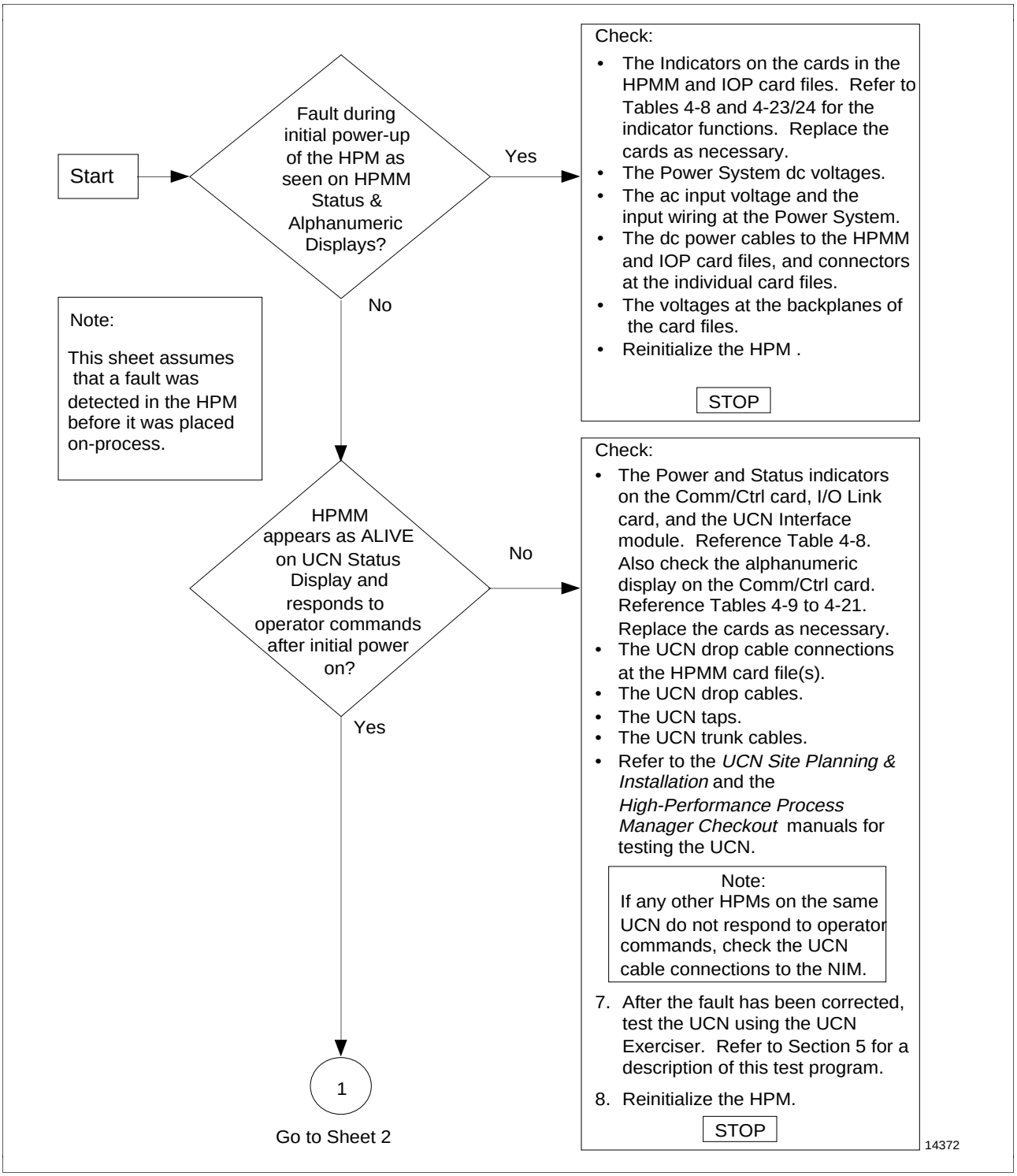
Use the following tables in this section in conjunction with the troubleshooting activities guided by the HPM troubleshooting flow chart. There will be specific references (exit points) to these tables given in the troubleshooting flowchart.

Table Number	Table Title
4-1	Corrective Actions (The corrective actions in this table are called for in Tables 4-2, 4-3, and 4-4.
4-2	Comm/Control Hard Failure Codes (Covers both HPMM Communications and Control processor Hard failures.)
4-3	HPMM Soft Failure Error Codes
4-4	Input/Output Link (IOL) Processor Hard Failure Codes
4-5	IOP Hard Failure Error Codes
4-6	IOP Box Soft Failure Error Codes
4-7	IOP Slot Soft Failure Error Codes
4-8	HPMM Card Indicators
4-9 through 4-21	HPMM Alphanumeric Display Sequences
4-23 through 4-24	IOP Card Indicators
4-25	FTA Indicators

4.3.1 Troubleshooting Flow Chart

Fault isolation flowchart (Sheet 1 of 6)

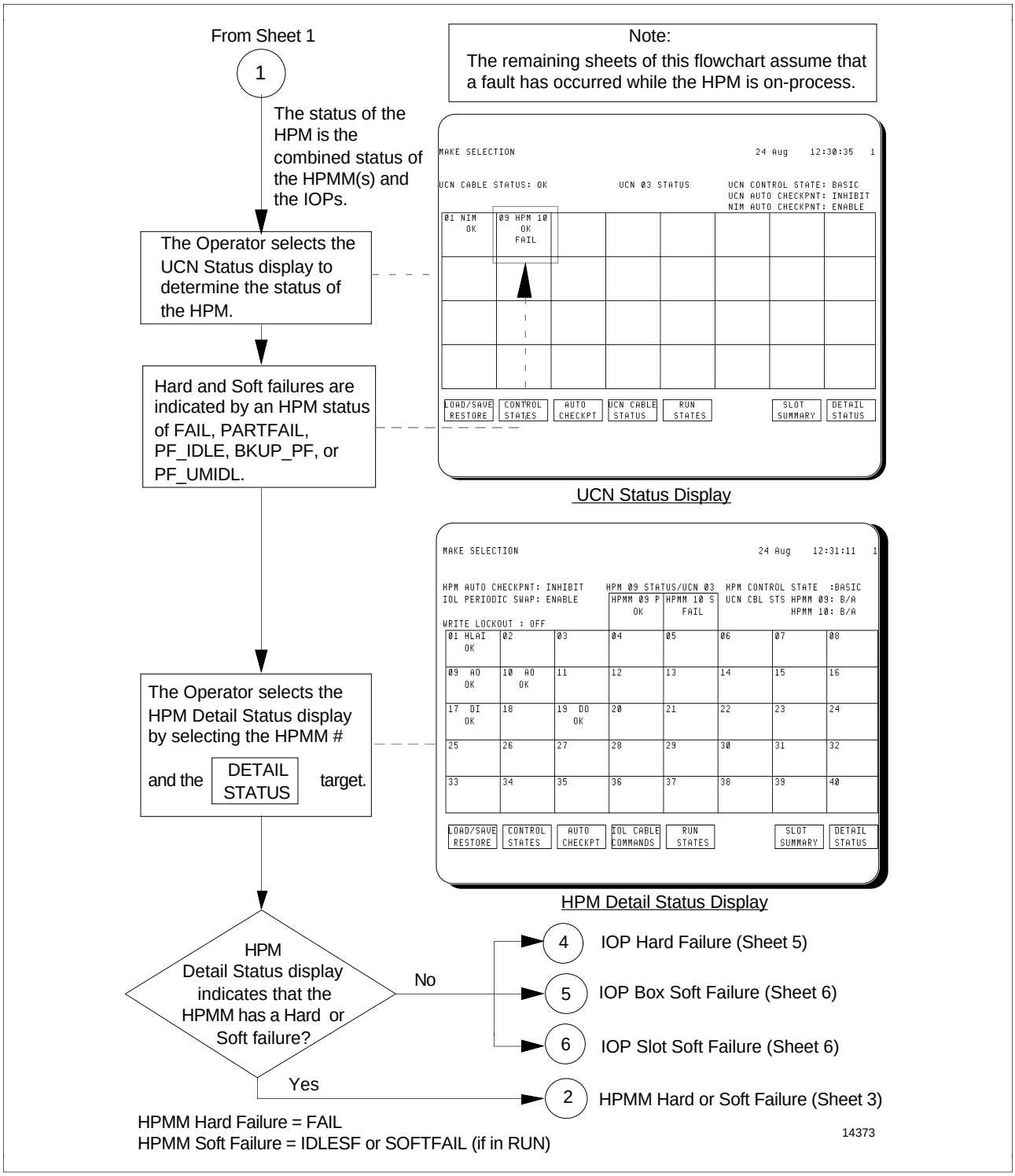
Figure 4-1 HPM Fault Isolation Flowchart (Sheet 1 of 6)



Continued on next page

Fault isolation flowchart (Sheet 2 of 6)

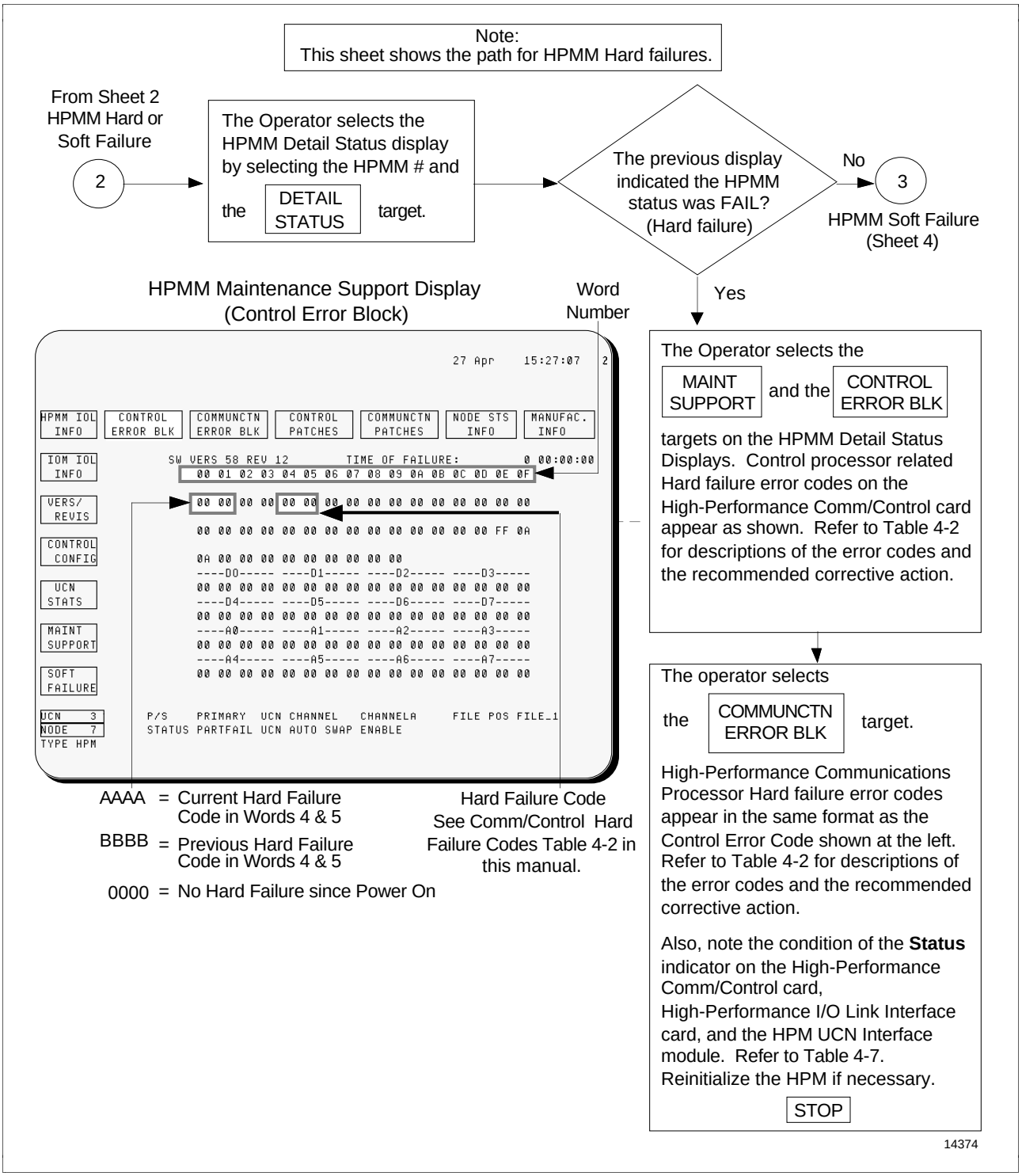
Figure 4-2 HPM Fault Isolation Flowchart (Sheet 2 of 6)



Continued on next page

Fault isolation flowchart
(Sheet 3 of 6)

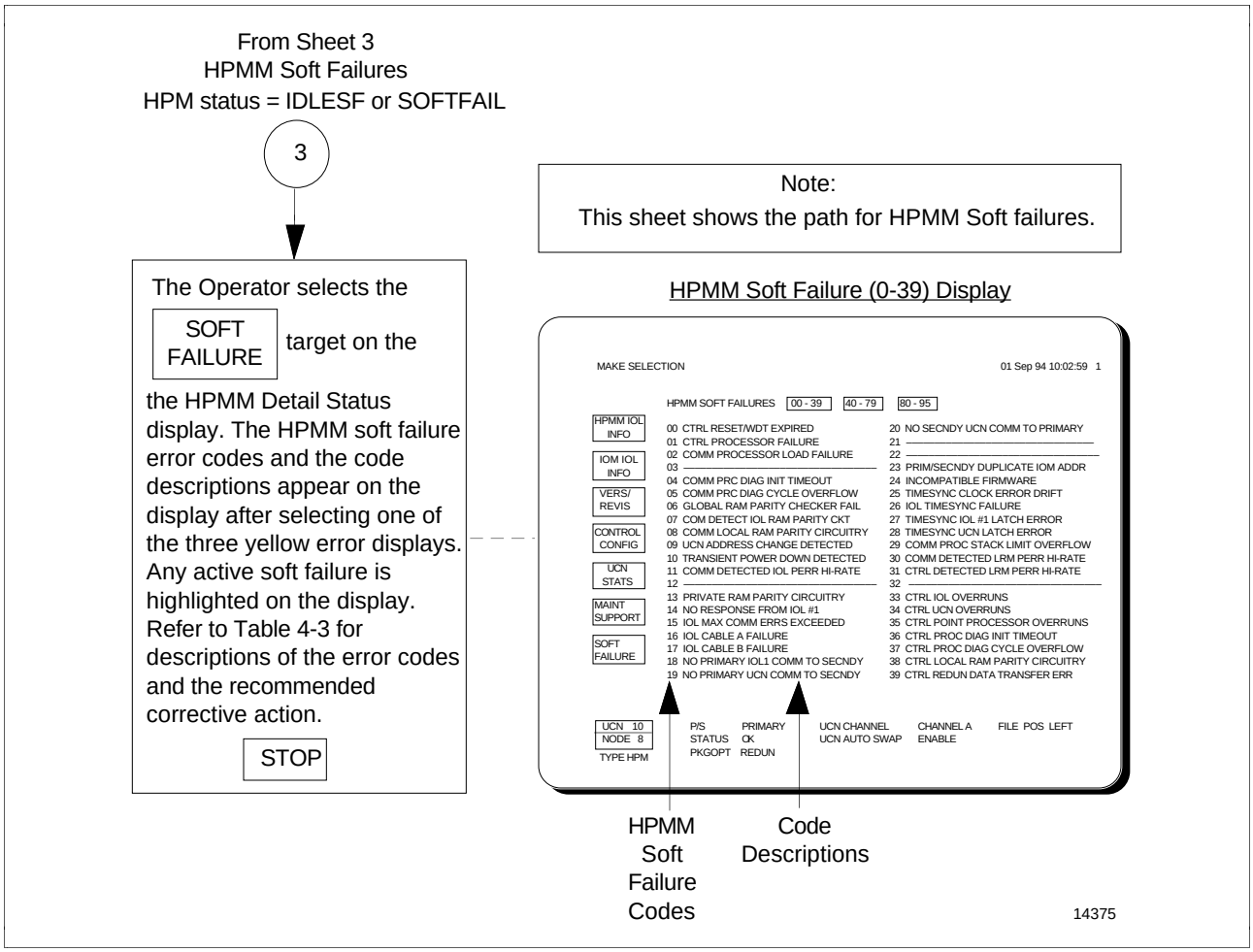
Figure 4-3 HPM Fault Isolation Flowchart (Sheet 3 of 6)



Continued on next page

Fault isolation flowchart
(Sheet 4 of 6)

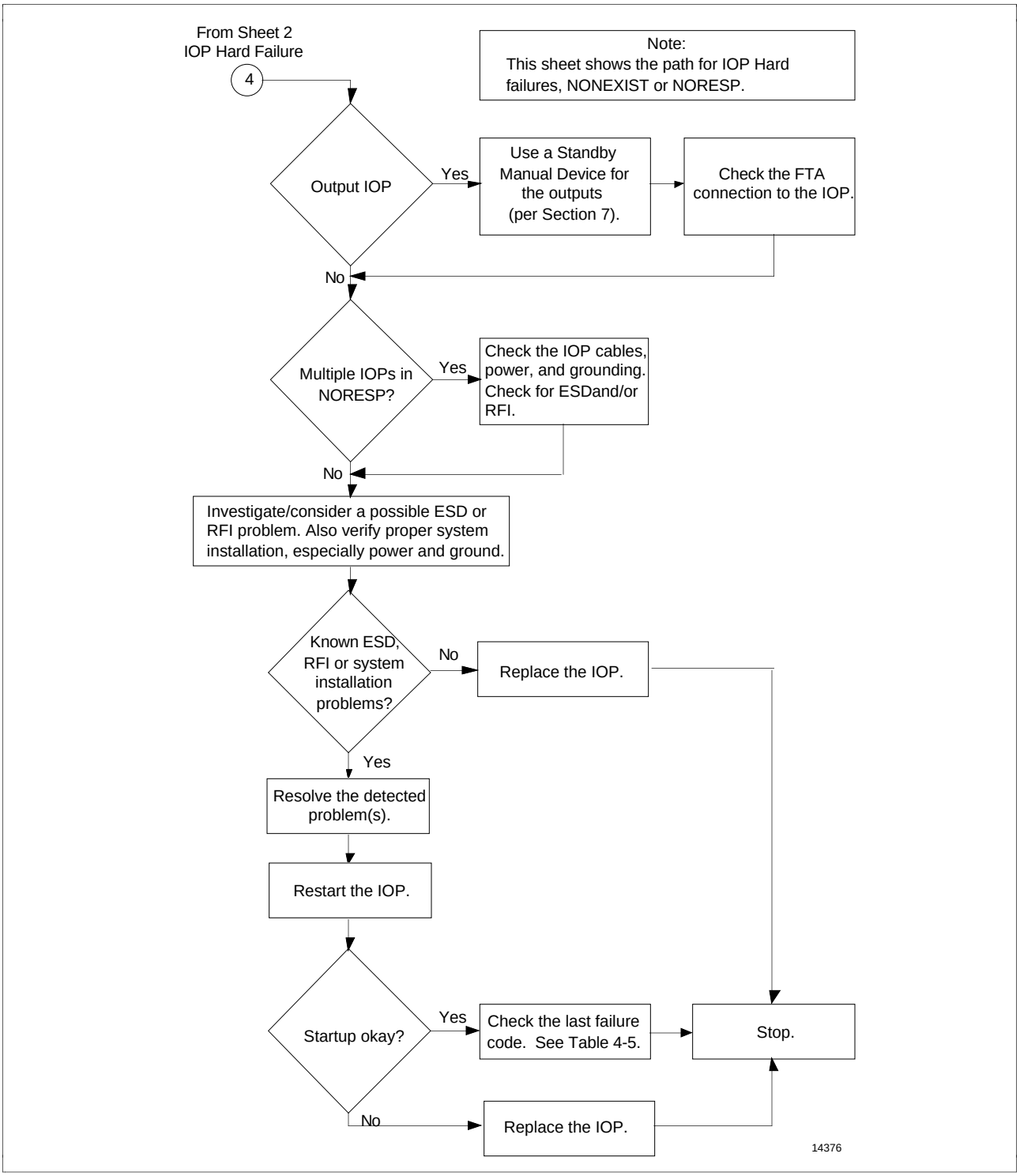
Figure 4-4 HPM Fault Isolation Flowchart (Sheet 4 of 6)



Continued on next page

Fault isolation flowchart (Sheet 5 of 6)

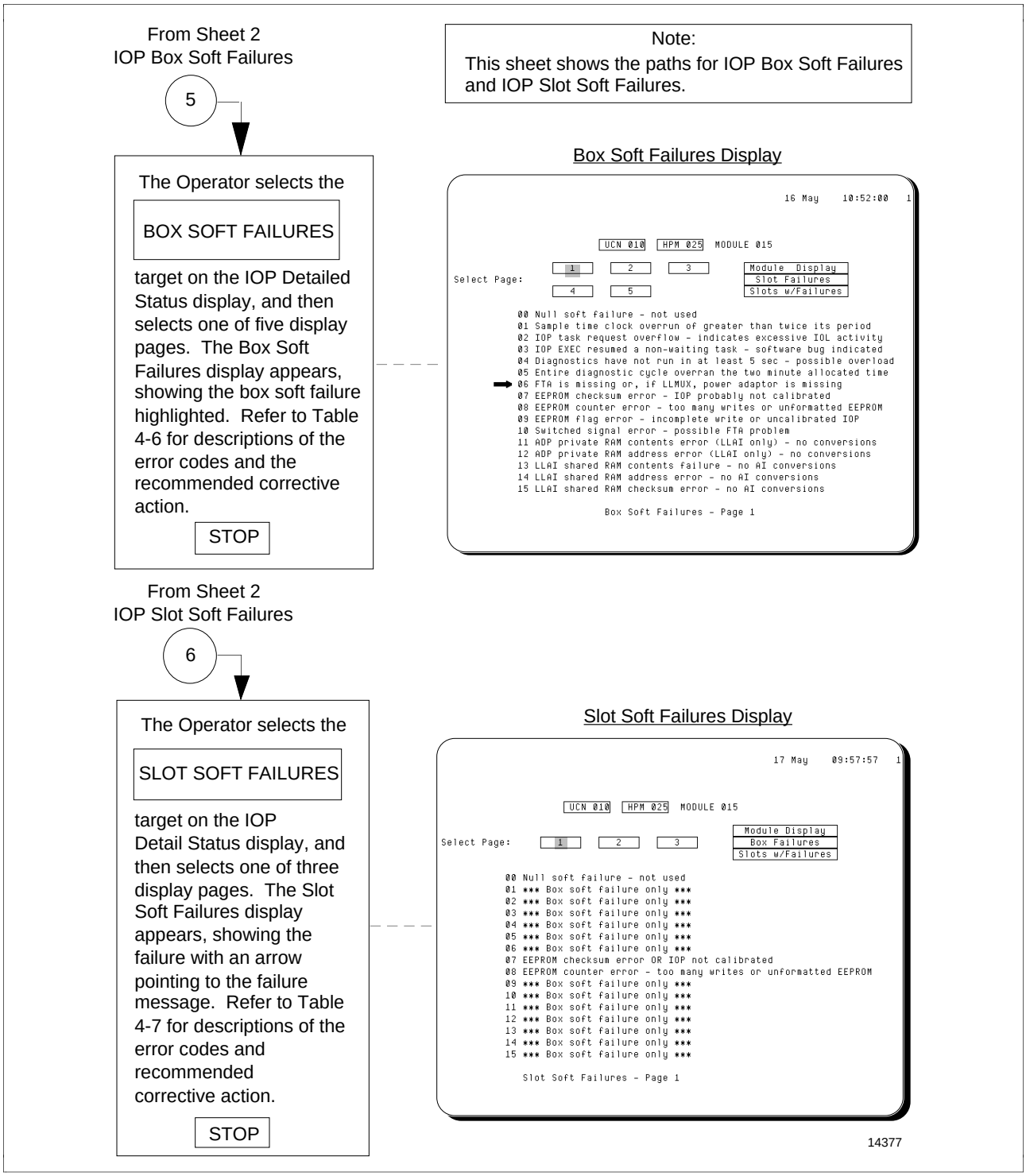
Figure 4-5 HPM Fault Isolation Flowchart (Sheet 5 of 6)



Continued on next page

Fault isolation flowchart
(Sheet 6 of 6)

Figure 4-6 HPM Fault Isolation Flowchart (Sheet 6 of 6)



4.3.2 HPMM Corrective Actions (Table 4-1)

Corrective actions for Tables 4-2, 4-3, and 4-4

Table 4-1 is a list of corrective actions that Tables 4-2, 4-3, and 4-4 reference.

Table 4-1 HPMM Corrective Actions

Number	Corrective Action Description
1	Call TAC for assistance.
2	Reload/restart the HPMM.
3	Check the UCN cables.
4	Check the UCN address and parity jumpers.
5	Check the card file's address and parity jumpers.
6	Replace the High-Performance Comm/Control card.
7	Replace the High-Performance I/O Link card.
8	Replace the HPM UCN Interface module.
9	Check/Replace the redundancy private-path cable.
10	Check/Replace the I/O Link Interface cables.
11	Replace the card file backplane.
12	Replace the Power Supply Module.
13	Ensure the High-Performance I/O Link card Voltage Margin jumper is in the **Normal** position.
14	Check the Control error block.
15	Check the Communications error block.
16	Check for excessive loading of the xPMM (peer-to-peer, heavy event load, large parameter access load from Universal Stations, etc.).
17	Ensure the Console Emulator serial port is secured by issuing the LK command. (Engineering and Factory Test only)
18	Remove the Redundancy cable.
19	Reduce the I/O Link Interface traffic used by the Control processor to recover from the I/O Link Interface overruns.

Continued on next page

I/O Link overruns

The use of AI PV scanning in the HPM improves the utilization of I/O Link resources. However, an HPM can still encounter I/O Link overruns. Continuous I/O Link overruns will result in the generation of an I/O Link overrun Soft failure.

In most cases, an I/O Link overrun indicates that the I/O Link Interface cannot handle the requested amount of traffic. In order to alleviate the I/o Link overrun situation, changes must be made in to the database to reduce or redistribute usage of the I/O Link for non-scan data during the offending cycle(s). I/O Link overrun counters are maintained and displayed for each 1/4 second cycle on the Schedule Information display.

I/O Link overruns corrective actions

Depending upon the application, one or more of the following actions may be appropriate.

- Avoid using IOP resident parameters other than:

  Analog Input scan parameters PV and PVSTS.

  all alarm flags such as BADPVFL, PVHHFL, PVHIFL, PVLOFL, PVLLFL, PVROCPTP and PVROCNTP.

  Digital Input scan parameters PVFL and BADPVFL.

  Digital Output scan parameters SO and INITREQ.
- Change the point mix or scan rate to redistribute or slow down points that read multiple non-scan I/O Link parameters.
- Use Logic points for non-scan I/O input connections that are used by more than one point.
- Delete inactive or non-essential points and non-scan input connections that are used by more than one point.

Contact the Honeywell Technical Assistance Center for additional help if the above recovery actions are not useful.

4.3.3 Comm/Control Hard Failure Codes (Table 4-2)

Comm/Control Hard failure codes

The following Table 4-2 defines the Hard failure codes for both the HPMM Communications and the Control processors. This table spans numerous pages. Some codes are used for both the Communications and Control processors where others are unique to an individual processor. The CPU column in the table indicates Both, Comm, or Control to make the distinction.

Corrective actions are identified by number. The corrective actions are listed in Table 4-1.

Table 4-2 Communications and Control Processor Hard Failure Codes

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0000	Both	NULL	Unknown Error	2
0001	Both	PWRDWN	Power Down Detected	2
0002	Both	LR_PAR	Local RAM parity error	2, 6
0003	Both	LR_LRAM	Unused on HPM Platform	1
0004	Both	LR_CK	Unused on HPM Platform	1
0005	Both	LR_EXC	Unused on HPM Platform	1
0006	Both	LR_HREV		
0007	Both	MM_HREV		
0008	Both	LR_TMR		
0009	Both	LR_PTRN	Local RAM pattern test failure	6
000A	Both	LR_BYTE	Unused on HPM Platform	1
000B	Both	LR_ADCD		
000C	Both	LR_ADDL		
000D	Both	LR_CLRR	Local RAM initialization test failure	6
000E	Both	SPARE20	Unused on HPM Platform	1
000F	Both	SR_PAR		
0010	Both	SR_PTRN		
0011	Both	SR_ADCD		
0012	Both	SR_ADDL		
0013	Both	GR_PAR		
0014	Comm	GR_PTRN	Global RAM pattern test failure	6

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0015	Both	GR_BYTE	Unused on HPM platform	1
0016	Both	GR ADCD	Unused on HPM platform	1
0017	Both	GR_ADDL	Global RAM EDAC circuitry test failure	6
0018	Comm	GR_CLRR	Global RAM initialization test failure	6
0019	Both	31_NR	Unused on HPM Platform	1
001 A	Both	31_ALIV		
001 B	Both	31 _ILTN		
001 C	Both	NMI_UNK		
001 D	Comm	BADUCNN	Bad UCN address/parity jumper setting	4, 6, 11
001 E	Both	NR	No response from other processor	2, 6
001 F	Both	MRFT	Memory reference table build failure	6
0020	Both	NOMTOS	Unused on HPM Platform	1
0021	Comrn	LLC_COMM	UCN LLC communication error	8, 6, 11
0022	Comm	UCNDRV	UCN Driver error	2, 6
0023	Both	RD_HREV	Unused on HPM Platform	1
0024	Both	SW_ERROR		
0025	Both	MD_HREV		
0026	Both	DA_PTRN		
0027	Both	DA_BYTE		
0028	Both	DA ADCD		
0029	Both	DA_ADDL		
002A	Both	DA_CLRR		
002B	Both	RD_SNPS		
002C	Both	RD_BSLK		
002D	Comm	TB_CMTO	UTBC command timeout	8, 6

Continued on next page

4.3.3 Comm/Control Hard Failure codes (Table 4-2), Continued

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
002E	Comm	TB_IF	UTBC interface test failure	6
002F	Comm	TB_LPBK	UTBC internal loopback test failure	6
0030	Comm	TB_RXI	UTBC RX internal loopback test failure	6
0031	Comm	TB_TXI	UTBC TX internal loopback test failure	6
0032	Comm	TB_RXE	UTBC RX external loopback test failure	8, 6, 11
0033	Comm	TB_TXE	UTBC TX external loopback test failure	8, 6, 11
0034	Comm	TB_MDFL	Modem failure or command timeout	8, 6, 11
0035	Comm	TB_INT	UTBC interrupt test failure	6
0036	Comm	TB_LSS	UTBC line switch & silence detect	8, 6, 11
0037	Comm	TB_TBCR	UTBC minimum revision test failure	6
0038	Comm	TB_TCLK	UTBC timesynch clock test failure	6
0039	Comm	TB_MJBR	Modem jabber test failure	8, 6, 11
003A	Comm	TB_MDCD	UTBC message decoder test failure	6
003B	Comm	TB_UM51	UM51 auxiliary latch test failure	7, 6
003C	Comm	ROM_CKS	ROM checksum comparison failure	6
003D	Both	FACTMOD	Unused on HPM Platform	1
003E	Both	ASIC_REG	ASIC Register accessibility test failure	6
003F	Both	FV_EXC	Force and verify exception test failure	6
0040	Comm	PR_PCHK	UTBC Private RAM parity circuitry test failure	6
0041	Comm	PR_PTRN	UTBC Private RAM pattern test failure	6
0042	Comm	PR_BW	UTBC Private RAM byte/word decode failure	6
0043	Comm	GR_BWL	Global RAM byte/word/long decode failure	6
0044	Both	LR_PCHK	Local RAM parity circuitry test failure	6
0045	Both	LR_BWL	Local RAM byte/word/long decode failure	6
0046	Comm	GB_PCHK	Global Bus parity circuitry test failure	7, 6, 11

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0047	Comm	IOL_BWL	IOL RAM byte/word/long decode failure	7
0048	Comm	IOL_PTRN	IOL RAM pattern test failure	7
0049	Comm	IOL_CLRR	IOL RAM initialization test failure	7
004A	Both	PRC_TYPE	Incorrect processor type	6
004B	Control	TRKRAM	Tracking mechanism test	6
004C	Both	TIMER	Timer comparison failure	6
004D	Comm	FLASH	Flash ROM read/write test failure	6
004E	Both	BE_EMBE	BERR - EDAC multiple bit error	6
004F	Both	BE_GLBP	BERR - Global Bus parity error	7, 6, 11
0050	Both	BE_OPTB	BERR - Option Card Bus Error	7, 6
0051	Both	BE_GLBT	BERR - Global Bus timeout	7, 6, 11
0052	Both	BE_ILLD	BERR - ASIC register data error	6
0053	Both	BE_ILLA	BERR - ASIC register illegal address error	2, 6
0054	Comm	ROM_WRT	BERR - Write to ROM	2, 6, 1
0055	Comm	PR_PAR	BERR - UTBC Private RAM parity error	2, 6, 1
0056	Both	CRASH	Software invoked crash	2, 6, 1
0057	Both	BAD_EXC	Bad or unexpected exception	2, 6, 1
0058	Both	WDT_TMO	Watchdog timer timeout	2, 6, 1
0059	Both	DMA_EXC	Unexpected DMA Channel interrupt	2, 6
005A	Both	CTL_EXC	Unexpected Control-to-Comm interrupt	2, 6
005B	Both	FRC_EXC	Unexpected FRC compare interrupt	2, 6
005C	Both	COM_PER	Unexpected Comm periodic interrupt	2, 6
005D	Both	CTL_PER	Unexpected Control periodic interrupt	2, 6
005E	Both	COM_EXC	Unexpected Comm-to-Control interrupt	2, 6
005F	Both	TRK_OVF	Unexpected tracking overflow interrupt	2, 6

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0060	Both	RDN_TBC	Unexpected RTBC interrupt	2, 6
0061	Both	UCN_TBC	Unexpected UTBC interrupt	2, 6
0062	Both	COM_UART	Unexpected Comm UART interrupt	2, 6
0063	Both	CTL_UART	Unexpected Control UART interrupt	2, 6
0064	Both	OPT_EXC	Unexpected Option Card interrupt	7, 6,11, 1
0065	Comm	PR_CLRR	UTBC Private RAM initialization test failure	6
0066	Comm	BADFILE	Bad File address/parity jumper setting	5, 6, 11
0067	Comm	BADSLOT	Bad Slot address/parity setting	6, 11
0068	Comm	IOL_PCHK	I/O Link RAM parity circuitry test failure	7, 6, 1
0069	Comm	IOL_ITMO	I/O Link timeout during transition to Idle	7, 6, 1
006A	Comm	IOL_IDLE	I/O Link failed to transition to Idle	7, 6, 1
006B	Comm	OL_RTMO	I/O Link timeout during transition to Run	7, 6, 1
006C	Comm	IOL_RUN	I/O Link failed to transition to Run	7, 6, 1
006D	Both	REFRESH	Global DRAM refresh circuitry failure	6, 1
006E	Both	PI_CKSM	Bad software personality checksum	2, 6, 1
006F	Both	BE_UNKN	Access to non-existent memory error	2, 6, 1
0070	Both	BERR_SRC	Unacknowledged BERR Source bits set	2, 6, 1
0071	Comm	EE_COM	Comm/Control serial EEPROM write test failure	6
0072	Comm	EE_IOL	I/O Link card serial EEPROM write test failure	7, 6, 11
0073	Comm	EE_UCN	UCN I/F card serial EEPROM write test failure	8, 6, 11
0074	Control	RT_IF	RTBC host interface test failure	6, 1
0075	Control	RT_LPBK	RTBC internal loopback test failure	9, 6, 1
0076	Control	RT_RXI	RTBC RX internal loopback test failure	9, 6, 1
0077	Control	RT_TXI	RTBC TX internal loopback test failure	9, 6, 1
0078	Control	RT_INT	RTBC interrupt test failure	6, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0079	Control	RT_UNRN	Unused on HPM Platform	1
007A	Control	RT_BERR	RTBC bus/address error	2, 6, 1
007B	Control	RT_FD	RTBC corrupted frame descriptor	2, 1
007C	Control	RT_OVRN	RTBC overrun error	2, 6, 1
007D	Control	RT_BDPE	RTBC Buffer Descriptor pool empty	2, 1
007E	Control	RT_FDPE	RTBC Frame Descriptor pool empty	2, 1
007F	Comm	CHGFILE	File address/parity jumpers have changed	5, 6, 11, 1
0080	Comm	CHGSLOT	Slot address/parity has changed	6, 11, 1
0081	Both	RSTCTL	Unused on HPM Platform	1
0082	Comm	Fl_COM	Fault insertion Comm crash	1
0083	Control	Fl_CTL	Fault insertion Control crash	1
0084	Control	Fl_PTRN	Fault insertion pattern comparison failure	1
0085	Both	UART_ACC	UART access error	2, 6
0086	Both	NO_HB	The other processor (Communications or Control) has no heatbeat.	2,6
0087 to 00FF	Both	Undefined	Reserved for future Hard failure codes.	1
0100 to 01FF	Comm	CRASH	UCN Token Bus Controller command timeout. These errors occur if the UTBC does not complete a non-modem related command.	6,1
0200 to 02FF	Comm	CRASH	Physical/MAC command to UTBC timeout. These errors occur if the UTBC does not complete a modem related command.	8, 6, 11, 1
0300	Comm	CRASH	Modem A failed to ACK reset in initialization	8, 6, 11, 1
0301	Comm	CRASH	Modem B failed to ACK reset in initialization	8, 6, 11, 1
0302	Comm	CRASH	Modem A failed to ACK reset in jabber test	8, 6, 11, 1
0303	Comm	CRASH	Modem B failed to ACK reset in jabber test	8, 6, 11, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0304	Comm	CRASH	Corrupted TX counter	2, 1
0305	Comm	CRASH	No free FD for TX to test	2, 1
0306	Comm	CRASH	No free FD for TX for resynch	2, 1
0307	Comm	CRASH	No free FD for TX for message	2, 1
0308	Comm	CRASH	Modem failed to ACK Enable Channel A command	8, 6, 11, 1
0309	Comm	CRASH	Modem failed to ACK Enable Channel B command	8, 6, 11, 1
030A	Comm	CRASH	Modem A failed to ACK in on-line command	8, 6, 11, 1
030B	Comm	CRASH	Modem B failed to ACK in on-line command	8, 6, 11, 1
030C	Comm	CRASH	Modem A failed to ACK in off-line command	8, 6, 11, 1
030D	Comm	CRASH	Modem B failed to ACK in off-line command	8, 6, 11, 1
030E	Comm	CRASH	UTBC bus/address error	2, 6, 1
030F	Comm	CRASH	UTBC faulty transmitter	6, 8, 1
0310	Comm	CRASH	Unexpected frame 6 (was expecting a response but received something else addressed to it).	4, 3, 2, 1
0311	Comm	CRASH	Unexpected frame 10 (was soliciting a new successor and heard another node transmit; this may be a duplicate token problem).	4,3,2,1
0312	Comm	CRASH	UTBC double bus/address error	2, 6, 1
0313	Comm	CRASH	Duplicate UCN node address	4, 1
0314	Comm	CRASH	Modem A error (jabber)	8, 6, 11, 1
0315	Comm	CRASH	Modem B error (jabber)	8, 6, 11, 1
0316	Comm	CRASH	UCN transmit hang	2, 8, 6,1
0317	Comm	CRASH	Unimplemented LLC transmit operation (Means IOCB address in FD was 0.)	2, 1
0318	Comm	CRASH	Bad immediate response FD address in RIOCB	2, 1
0319	Comm	CRASH	No FD for RDR	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
031A	Comm	CRASH	No BD in FD on RDR SAP update	2, 1
031B	Comm	CRASH	Bad RDR FD pointer on close SAP	2, 1
031C	Comm	CRASH	Bad link to BD	2, 1
031D to 03FF	Comm	CRASH	Reserved for future LLC crash codes	1
0400	Comm	CRASH	Null error	2, 1
0401	Comm	CRASH	Failed self-test	8, 6, 11, 1
0402	Comm	CRASH	Unused on HPM Platform	1
0403	Comm	CRASH	Unused on HPM Platform	1
0404	Comm	CRASH	Illogical operational status	2, 1
0405	Comm	CRASH	Command register incorrectly busy	2, 1
0406	Comm	CRASH	Unused on HPM Platform	1
0407	Comm	CRASH	Unused on HPM Platform	1
0408	Comm	CRASH	Unused on HPM Platform	1
0409	Comm	CRASH	Command queue full	2, 1
040A	Comm	CRASH	Unused on HPM Platform	1
040B	Comm	CRASH	Illegal command	2, 1
040C	Comm	CRASH	Unused on HPM Platform	1
040D	Comm	CRASH	IOCB format error	2, 1
040E	Comm	CRASH	Unused on HPM Platform	1
040F	Comm	CRASH	Unused on HPM Platform	1
0410	Comm	CRASH	Unused on HPM Platform	1
0411	Comm	CRASH	Unexpected IOCB chain stop complete	2, 1
0412	Comm	CRASH	Unexpected end of IOCB chain	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0413 to 041B	Comrn	CRASH	Unused on HPM Platform	1
041C	Comm	CRASH	Remove reply list error (not found).	2, 1
041D	Comm	CRASH	Unused on HPM Platform	1
041E	Comm	CRASH	Write Tx buffer pointer FIFO full	2, 1
041F	Comm	CRASH	LLC returned zero pointer as valid	2, 1
0420	Comm	CRASH	Unused on HPM Platform	1
0421	Comm	CRASH	Put to channel - already in chain.	2, 1
0422	Comm	CRASH	Attempt to double unblock Type 3 node.	2, 1
0423	Comm	CRASH	Test switch was set.	2, 1
0424	Comm	CRASH	Reserved	1
0425	Comm	CRASH	Reserved	1
0426	Comm	CRASH	Duplicate network address error	4, 1
0427	Comm	CRASH	STUN command from network	2, 8, 6, 1
0428	Comm	CRASH	Transmit hang	2, 8, 6, 1
0429	Comm	CRASH	Configure timeout/Transmit hang	2, 8, 6, 1
042A	Comm	CRASH	Unused on HPM Platform	1
042B	Comm	CRASH	Not enough task channels available.	2, 1
042C	Comm	CRASH	Unused on HPM Platform	1
042D	Comm	CRASH	RX buffer already assigned	2, 1
042E	Comm	CRASH	RX buffer was not assigned	2, 1
042F	Comm	CRASH	Reply-mask/request type mismatch	2, 1
0430	Comm	CRASH	Error in assignment to driver	2, 1
0431	Comm	CRASH	Unexpected channel not open; not result of bad network message	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0432	Comm	CRASH	Unused on HPM Platform	1
0433	Comm	CRASH	Unused on HPM Platform	1
0434	Comm	CRASH	Unused on HPM Platform	1
0435	Comm	CRASH	Unused on HPM Platform	1
0436	Comm	CRASH	LLC detected jabber	2, 8, 6, 1
0437	Comm	CRASH	LLC detected faulty transmitter	2, 3, 8, 6, 1
0438	Comm	CRASH	LLC called COMM_FAIL routine	2, 8, 6, 1
0439	Comm	CRASH	Unrecoverable IOCB error	2, 1
043A	Comm	CRASH	Timesynch stuck in diagnostic mode	2, 6, 1
043B	Comm	CRASH	Timesynch clock stopped	2, 6, 1
043C to 04FF	Comm	CRASH	Reserved for future UCNC driver crash codes.	1
0500	Comm	CRASH	Event Distributor returned bad MTOS status waiting for its LEF to be set.	2, 1
0501	Comm	CRASH	Event Distributor returned bad MTOS status resetting its LEF.	2, 1
0502	Comm	CRASH	Illogical PN$Add_MMS_Request return status to Event Distributor.	2, 1
0503	Comm	CRASH	Event Distributor encountered illegal event record.	2, 1
0504	Comm	CRASH	MTOS error, could not change priority of given event producer task.	2, 1
0505	Comm	CRASH	Bad event packet detected.	2, 1
0506	Comm	CRASH	MTOS error, could not return event producer task to its inherent priority.	2, 1
0507	Comm	CRASH	Collector task did not correctly schedule a timed resetting of timesynch timer LEF.	2, 1
0508	Comm	CRASH	MTOS error, could not set LEF of Event Distributor task.	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0509	Comm	CRASH	MTOS error, could not resume Event Distributor task.	2, 1
050A	Comm	CRASH	Resource error on UM$SEND_IOL call that initiates collection of given SIOM ECL.	2, 1
050B	Comm	CRASH	Collector task could not reset its own LEF.	2, 1
050C	Comm	CRASH	Collector task did not correctly schedule a timed resetting of its own LEF.	2, 1
050D	Comm	CRASH	Collector task did not correctly wait for setting of its own LEF.	2, 1
050E	Comm	CRASH	Could not raise Event Collector task's priority to that above IOL I/F task.	2, 1
050F	Comm	CRASH	Did not receive a resume from IOL I/F task in 30 seconds for completion of collection on at least one IOM ECL.	2, 1
0510	Comm	CRASH	Could not return Event Collector task to its inherent priority.	2, 1
0511	Comm	CRASH	Resource error on UM$SEND_IOL call for collection of SIOM ECL summary bytes.	2, 1
0512	Comm	CRASH	Illogical condition, could not find corresponding collection status connection record.	2, 1
0513	Comm	CRASH	Invalid SIOM Point/System bracket event	2, 1
0514	Comm	CRASH	Invalid SIOM Recovery bracket event	2, 1
0515	Comm	CRASH	Invalid PROCESS ALARM event from AIM module	2, 1
0516	Comm	CRASH	Invalid SIOM STATE CHANGE event	2, 1
0517	Comm	CRASH	Invalid SIOM event type	2, 1
0518	Comm	CRASH	Resource error on UM$SEND_IOL call for update of SIOM ECL remove pointer	2, 1
0519	Comm	CRASH	Could not change Event Collector task's priority.	2, 1
051A	Comm	CRASH	Did not receive a resume from IOL I/F task within 30 seconds for completion of SIOM ECL Summary byte collection.	2, 1

Continued on next page

4.3.3 Comm/Control Hard Failure codes (Table 4-2), Continued

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
051B	Comm	CRASH	Could not return Event Collector task to its inherent priority.	2, 1
051C	Comm	CRASH	Illogical condition, received an OK IOL message but response has unexpected internal size.	2, 1
051D	Comm	CRASH	Resource error on UM$SEND_IOL call for initiation of collection of next SIOM ECL.	2,1
051E	Comm	CRASH	Illegal return status on LEF reset	2, 1
051F	Comm	CRASH	Illegal system event	2, 1
0520	Comm	CRASH	Illegal SIOM state	2, 1
0521	Comm	CRASH	Illegal SIOM state change event	2, 1
0522	Comm	CRASH	Illegal SIOM bracket event	2, 1
0523	Comm	CRASH	Illegal UM or IOM event in system event	2, 1
0524	Comm	CRASH	Illegal HPN event type	2, 1
0525	Comm	CRASH	Bad resume on recovery task	2, 1
0526	Comm	CRASH	Bad failover run resume	2, 1
0527	Comm	CRASH	Bad resume on event tasks	2, 1
0528	Comm	CRASH	Request to Control failed.	2, 1
0529	Comm	CRASH	SIOM recovery failed.	2, 1
052A	Comm	CRASH	Changing priority failed.	2, 1
052B	Comm	CRASH	Improper resume	2, 1
052C	Comm	CRASH	Improper copy of event flags	2, 1
052D	Comm	CRASH	Improper resetting of event flags	2, 1
052E	Comm	CRASH	Improper timed event setting	2, 1
052F	Comm	CRASH	Distributor COPY flags failure	2, 1
0530	Comm	CRASH	Recover SIOM failure	2, 1

Continued on next page

4.3.3 Comm/Control Hard Failure codes (Table 4-2), Continued

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0531	Comm	CRASH	IOL return failure	2, 1
0532	Comm	CRASH	Collector task did not correctly schedule a timed resetting of timesynch SCS timer LEF.	2, 1
0533	Comm	CRASH	Bad resume on Recovery Task	2, 1
0534	Comm	CRASH	Collector task did not correctly reset Num_evt_LEF.	2, 1
0535	Comm	CRASH	Collector task did not correctly perform timed setting of Num_evt_LEF.	2, 1
0536	Comm	CRASH	Collector task did not correctly perform timed set of Coll_TOG_Timer_LEF to 2 seconds.	2, 1
0537 to 05FF	Comm	CRASH	Reserved for future Event Subsystem crash codes.	1
0600	Comm	CRASH	Message size < 0 or > maximum size	2, 1
0601	Comm	CRASH	Received already released message block from DBIF.	2, 1
0602	Comm	CRASH	Error status message (2 words) can not fit into empty send buffer on error return.	2, 1
0603	Comm	CRASH	Error status message (2 words) can not fit into empty send buffer on normal return.	2, 1
0604	Comm	CRASH	DBIF resources will be lost forever.	2, 1
0605	Comm	CRASH	Received already released send-receive block from HPN.	2, 1
0606	Comm	CRASH	Reply buffer size too small	2, 1
0607	Comm	CRASH	Could not get MTOS semaphore (stack handling 1).	2, 1
0608	Comm	CRASH	Could not release MTOS semaphore (stack handling 1).	2, 1
0609	Comm	CRASH	Could not get MTOS semaphore (stack handling 2).	2, 1

Continued on next page

4.3.3 Comm/Control Hard Failure codes (Table 4-2), Continued

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
060A	Comm	CRASH	Can not add to full stack.	2, 1
060B	Comm	CRASH	Could not release MTOS semaphore (stack handling 2).	2, 1
060C	Comm	CRASH	Can not add to full list.	2, 1
060D	Comm	CRASH	List corrupted.	2, 1
060E	Comm	CRASH	Can not add to full FIFO.	2, 1
060F	Comm	CRASH	Trouble waiting on MTOS Event Flag 1	2, 1
0610	Comm	CRASH	Trouble resetting MTOS Event Flag 1	2, 1
0611	Comm	CRASH	Trouble resetting MTOS Event Flag 2	2, 1
0612	Comm	CRASH	Trouble waiting on MTOS Event Flag 2	2, 1
0613	Comm	CRASH	Trouble resetting MTOS Event Flag 3	2, 1
0614	Comm	CRASH	Trouble resetting MTOS Event Flag 4	2, 1
0615	Comm	CRASH	Size of a write request buffer is > 504 words.	2, 1
0616 to 067F	Comm	CRASH	Reserved for future HPI Subsystem crash codes.	1
0680	Comm	CRASH	Memory allocated for EVT and HPI DB is too small.	1
0681	Comm	CRASH	Structured constant security check fail 1	2, 1
0682	Comm	CRASH	Structured constant security check fail 2	2, 1
0683	Comm	CRASH	Structured constant security check fail 3	2, 1
0684	Comm	CRASH	Structured constant security check fail 4	2, 1
0685	Comm	CRASH	Structured constant security check fail 5	2, 1
0686	Comm	CRASH	Structured constant security check fail 6	2, 1
0687	Comm	CRASH	Buffer Allocated for Data Base handling is too small.	1
0688	Comm	CRASH	Control, I/O Link, or Remote processor timeout	2, 6, 7, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0689	Comm	CRASH	Change Task Priority fail 1	2, 1
068A	Comm	CRASH	Change Task Priority fail 2	2, 1
068B	Comm	CRASH	Change Task Priority fail 3	2, 1
068C	Comm	CRASH	General Data record size has changed.	1
068D	Comm	CRASH	Set/Reset Swap event flag failed.	2, 1
068E	Comm	CRASH	Wait for Swap event flag failed.	2, 1
068F	Comm	CRASH	Timed event flag failed.	2, 1
068C to 06BF	Comm	CRASH	Reserved for future GBL Subsystem crash codes.	1
06C0 to 06C2	Both	CRASH	Unused on HPM Platform.	1
06C3	Both	CRASH	Comm to Control interrupt failure	2, 6, 1
06C4	Both	CRASH	Control to Comm interrupt failure	2, 6, 1
06C5	Comm	CRASH	I/O Link code in wrong location.	1
06C6	Comm	CRASH	I/O Link code wrong size.	1
06C7 to 06DC	Comm	CRASH	Reserved for future miscellaneous crash codes.	1
06DD	Comm	CRASH	Control processor startup failure	6, 1
06DE	Comm	CRASH	I/O Link processor(s) startup failure	7, 6, 1
06DF	Comm	CRASH	Bad common memory signature	1
06E0	Comm	CRASH	CPU Free change priority fail #1	2, 1
06E1	Comm	CRASH	CPU Free change priority fail #2	2, 1
06E2	Comm	CRASH	CPU Free pause fail	2, 1
06E3	Comm	CRASH	Could not set CPU Free LEF.	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
06E4	Comm	CRASH	Could not reset CPU Free LEF.	2, 1
06E5	Comm	CRASH	Could not reset Timer Comparison LEF.	2, 1
06E6	Comm	CRASH	Could not set Timer Comparison LEF.	2, 1
06E7 to 06EF	Comm	CRASH	Reserved for future high priority task crash codes.	1
06F0	Comm	CRASH	Could not set Peer to Peer Statistics LEF.	2, 1
06F1	Comm	CRASH	Could not reset Peer to Peer Statistics LEF.	2, 1
06F2	Comm	CRASH	Could not reset Diagnostic Overflow LEF.	2, 1
06F3	Comm	CRASH	Could not set Diagnostic Overflow LEF.	2, 1
06F4 to 06FF	Comm	CRASH	Reserved for future high priority task crash codes.	1
0700	Comm	CRASH	Change Task Priority call failed.	2, 1
0701	Comm	CRASH	Mail box entry has bad MTOS return code.	2, 1
0702	Comm	CRASH	Pause Timeout if pause selected.	2, 1
0703	Comm	CRASH	Mailbox fetch returned illegal code.	2, 1
0704	Comm	CRASH	Mailbox send of response returned illegal code.	2, 1
070E	Comm	CRASH	Mailbox fetch returned illegal code.	2, 1
070F	Comm	CRASH	Resume of user's task returned illegal code.	2, 1
0710	Comm	CRASH	Task ran out of resources; not legally possible since there are more of these than SMS buffers.	2, 1
0711	Comm	CRASH	Wait for event flag returned illegal code.	2, 1
0712	Comm	CRASH	Reset of event flag returned illegal code.	2, 1
0713	Comm	CRASH	IF_action passed in MSG_if_rec is not supported.	2, 1
0714 to 07FF	Comm	CRASH	Reserved for future IOI Subsystem crash codes.	1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0800	Comm	CRASH	Mail box send returned illegal code.	2, 1
0801	Comm	CRASH	Set of event flag for CCITrn task failed.	2, 1
0802	Comm	CRASH	Reset of IMR event flag failed.	2, 1
0803	Comm	CRASH	Wait for IMR event flag failed.	2, 1
0804	Comm	CRASH	Timed set of event flag failed.	2, 1
0805	Comm	CRASH	Mail box send to DBIRET failed.	2 1
0806	Comm	CRASH	Setting of CClbuf EF failed.	2, 1
0807	Comm	CRASH	Timed set of event flag failed.	2, 1
0808	Comm	CRASH	Wait for mailbox or timeout EF failed.	2, 1
0809	Comm	CRASH	Test of timeout EF failed.	2, 1
080A	Comm	CRASH	Reset of mailbox event flag failed.	2, 1
080B	Comm	CRASH	Reset of CClbuf EF failed.	2, 1
080C	Comm	CRASH	Wait for CClbuf EF returned illegal code.	2, 1
080D	Comm	CRASH	Send of mailbox data to DBIRET failed.	2, 1
080E	Comm	CRASH	Set of IMR free EF failed.	2 1
080F	Comm	CRASH	Wait for CCI receive EF failed.	2, 1
0810	Comm	CRASH	Reset of CCI receive EF failed.	2, 1
0811	Comm	CRASH	No IMR so cannot perform clean swap.	2, 1
0812	Comm	CRASH	Reset of TMOT event flag failed.	2, 1
0813 to 08FF	Comm	CRASH	Reserved for future CCI Subsystem crash codes.	1
0900	Comm	CRASH	Mail box send to DBIGET failed.	2, 1
0901	Comm	CRASH	Pause completion returned illegal code.	2, 1
0902	Comm	CRASH	Reset of no resource EF failed.	2, 1
0903	Comm	CRASH	Wait for message if record EF failed	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0904	Comm	CRASH	Reset of DBl_ASSO_Rec EF failed.	2, 1
0905	Comm	CRASH	Wait for Asso record failed.	2, 1
0906	Comm	CRASH	Mail box receive of input data failed.	2, 1
0907	Comm	CRASH	Mail box send of response to user failed.	2, 1
0908	Comrn	CRASH	Mailbox receive of data from servers failed.	2, 1
0909	Comm	CRASH	Incorrect priority mailbox received.	2, 1
090A	Comm	CRASH	Illegal ASSOC record returned.	2, 1
090B	Comm	CRASH	Illegal MIR record returned.	2, 1
090C to 09FF	Comm	CRASH	Reserved for future DBI Subsystem crash codes.	1
0A00	Comm	CRASH	Redundancy task reset EF failure	2, 1
0A01	Comm	CRASH	Redundancy task set timed EF failure	2, 1
0A02	Comm	CRASH	Redundancy task change priority failure	2, 1
0A03	Comm	CRASH	I/O Link timeout	2, 6, 7, 1
0A04	Comm	CRASH	I/O Link in primary failed	2, 6, 7, 1
0A05	Comm	CRASH	Spare crash 1	1
0A06	Comm	CRASH	Spare crash 2	1
0A07	Comm	CRASH	Set timeout EF failure	2, 1
0A08	Comm	CRASH	Timeout failure	2, 1
0A09	Comm	CRASH	Set timeout EF failure 2	2, 1
0A0A	Comm	CRASH	Secondary is wrong Pl.	2, 1
0A0B	Comm	CRASH	Timeout failure 2	2, 1
0A0C	Comm	CRASH	Terminate failed.	2, 1
0A0D	Comm	CRASH	Spare crash 4	1
0A0E	Comm	CRASH	Illegal pause status	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0A0F	Comm	CRASH	Could not read own Checkpoint.	2, 6, 1
0A10	Comm	CRASH	Could not gain I/O Link.	2, 6, 7, 1
0A11	Comm	CRASH	Control processor failure detected.	14
0A12	Comm	CRASH	Control card mismatch	1
0A13	Comm	CRASH	Secondary lost synch.	18, 3, 10, 6
0A14	Comm	CRASH	Secondary incompatible database	2, 1
0A15	Comm	CRASH	Set EF failure	2, 1
0A16	Comm	CRASH	Wait EF failure	2, 1
0A17	Comm	CRASH	Could not write own Checkpoint.	2, 6, 1
0A18	Comm	CRASH	Primary timesynch hardware failure	2, 6, 1
0A19	Comm	CRASH	Secondary timesynch hardware failure	2, 6, 1
0A1A	Comm	CRASH	Control watchdog timed out.	2, 6, 1
0A1B	Comm	CRASH	I/O Link watchdog timed out.	2, 6, 7, 1
0A1C	Comm	CRASH	Control processor in reset	2, 6, 1
0A1D	Comm	CRASH	I/O Link processor in reset	2, 6, 7, 1
0A1E to 0A1F	Comm	CRASH	Reserved for future RDN Subsystem crash codes.	1
0A20	Comm	CRASH	UCN in primary has failed.	3, 8, 6, 1
0A21	Comm	CRASH	Secondary alone on UCN	3, 8, 6,1
0A22 to 0A2F	Comm	CRASH	Reserved for future RDN Subsystem crash codes. Upon issuing the Recovery (i.e. shutdown command, a RAM Retention startup is attempted for the A2x crash codes.	1
0A30	Comm	CRASH	Reset sync-time latch EF failed.	2, 1
0A31	Comm	CRASH	Set latch sync-time timer EF failed.	2, 1
0A32	Comm	CRASH	Wait sync-time latch EF failed.	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0A33 to 0A7F	Comm	CRASH	Reserved for future RDN Subsystem crash codes.	1
0A80	Comm	CRASH	RDR receive failed.	2, 8, 6,1
0A81	Comm	CRASH	RDR add MMS failed.	2, 1
0A82	Comm	CRASH	Node status size error	2, 1
0A83	Comm	CRASH	Wait for EF failure.	2, 1
0A84	Comm	CRASH	Reset EF failure.	2, 1
0A85	Comm	CRASH	Set response EF failure.	2, 1
0A86 to 0AFF	Comm	CRASH	Reserved for future RDR Subsystem crash codes.	1
0B00	Comm	CRASH	MTOS resource error.	2, 1
0B01	Comm	CRASH	Reserved 1.	2, 1
0B02	Comm	CRASH	Initialize task error on supervisor request.	2, 1
0B03	Comm	CRASH	Initialize task detected IOL failure in redundancy.	2, 7, 1
0B04	Comm	CRASH	Set timed EF failure.	2, 1
0B05	Comm	CRASH	Wait for timed EF failure.	2, 1
0B06	Comm	CRASH	Reset EF failure.	2, 1
0B07	Comm	CRASH	Initialize task detected wrong Comm FW.	1
0B08	Comm	CRASH	Initialize task detected wrong Control FW.	1
0B09	Comm	CRASH	Initialize task detected wrong IOL FW.	1
0B0A	Comm	CRASH	Change priority failure.	2, 1
0B0B	Comm	CRASH	I/O Link timeout.	2, 6, 7,1
0B0C	Comm	CRASH	Set/reset swap EF failure.	2, 1
0B0D	Comm	CRASH	Wait swap EF failure.	2, 1

Continued on next page

4.3.3 Comm/Control Hard Failure codes (Table 4-2), Continued

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
0B0E to 0B7F	Comm	CRASH	Reserved for future Supervisor Subsystem crash codes.	1
0B80	Comm	CRASH	Illegal task invocation	2, 1
0B81	Comm	CRASH	Set timed EF failure.	2, 1
0B82	Comm	CRASH	Illegal wait for EF	2, 1
0B83	Comm	CRASH	Illegal pause status	2, 1
0B84	Comm	CRASH	Reset EF failure.	2, 1
0B85 to 0BFF	Comm	CRASH	Reserved for future IOP Failover Subsystem crash codes.	1
0C00	Comm	CRASH	Operating system has no SRBs available.	2,1
0C01	Comm	CRASH	Bad MMU alignment	1
0C02 to 0CFF	Comm	CRASH	Reserved for future Operating system (MTOS) Subsystem crash codes.	1
0D00 to 0D0F	Both	CRASH	Unused on HPM platform.	1
0D10	Both	CRASH	SW EDAC unrecoverable Local RAM PERR.	2, 6,1
0D11	Both	CRASH	SW EDAC multiple Local RAM PERRs failure.	2, 6, 1
0D12	Comm	CRASH	SW EDAC unrecoverable I/O Link RAM PERR.	2, 7, 1
0D13	Comm	CRASH	SW EDAC multiple I/O Link RAM PERRs failure.	2, 7, 1
0D14 to 7FFF	Comm	CRASH	Reserved for future Comm crash codes.	1
8000 to FFFF	Comm	CRASH	Unused by Communications processor.	1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
8000 to FFD9	Control	CRASH	Reserved for future Control crash codes.	1
FFDA	Control	CRASH	Flush address out of Control database boundary.	2, 6, 1
FFDB	Control	CRASH	Illegal SIZ-A1A0 combination.	2, 6, 1
FFDC	Control	CRASH	Wait for 10 scan response timeout.	15
FFDD	Control	CRASH	I/O scan response failed.	15
FFDE	Control	CRASH	Unused on HPM Platform.	1
FFDF	Control	CRASH	Unused on HPM Platform.	1
FFE0	Control	CRASH	Diagnostic task detected bad Pl checksum.	2, 6, 1
FFE1	Control	CRASH	Bad common memory signature	1
FFE2	Control	CRASH	Memory sizing remainder error	1
FFE3	Control	CRASH	PPX task could not set CPU Free LEF.	2, 1
FFE4	Control	CRASH	PPX task could not reset CPU Free LEF.	2, 1
FFE5	Control	CRASH	CPU Free pause failure	2, 1
FFE6	Control	CRASH	CPU Free change priority fail #2	2, 1
FFE7	Control	CRASH	CPU Free change priority fail #1	2, 1
FFE8	Control	CRASH	Bad counts for tracking counter	2, 6, 1
FFE9	Control	CRASH	End2end context save failed.	2, 6, 1
FFEA	Control	CRASH	End2end checksum failed.	2, 6, 1
FFEB	Control	CRASH	Invalid slot in sequence	2, 1
FFEC	Control	CRASH	Sequence memory corrupted.	2, 6, 1
FFED	Control	CRASH	Invalid command during upgrade	2, 1
FFEE	Control	CRASH	Database revisions incompatible	2,1
FFEF	Control	CRASH	Prefetch-poststore wait timeout	2, 7, 6, 1
FFF0	Control	CRASH	Free IMR not avai	2, 1

Continued on next page

Comm/Control Hard failure codes, continued

Table 4-2 Communications and Control Processor Hard Failure Codes, Continued

Error Code	CPU	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
FFF1	Control	CRASH	Inconsistent Pascal and assembly database definitions	2, 1
FFF2	Control	CRASH	Redundancy private path initialization failed.	9, 6, 1
FFF3	Control	CRASH	Comm or IOL failed.	15
FFF4	Control	CRASH	IOL poststore response failed.	15
FFF5	Control	CRASH	IOL prefetch response failed.	15
FFF6	Control	CRASH	Bad request or reply-pointer in pas task	2, 1
FFF7	Control	CRASH	Bad type of startup transition	2, 1
FFF8	Control	CRASH	MTOS task start returned bas status.	2, 1
FFF9	Control	CRASH	MTOS pause failed.	2, 1
FFFA	Control	CRASH	MTOS task priority change failed.	2, 1
FFFB	Control	CRASH	Default scan rate fails data owner checks.	2, 1
FFFC	Control	CRASH	Default number of slots fails data owner checks.	2, 1
FFFD	Control	CRASH	Largest slot db too big for tracked RAM	2, 1
FFFE	Control	CRASH	Actual slot size greater than slot size constant	2, 1
FFFF	Control	CRASH	Slot plus sequence program database is less than the total number of memory units reserved.	2, 1

4.3.4 HPMM Soft Failure Codes (Table 4-3)

ATTENTION

ATTENTION—The HPM I/O Link Interface periodically monitors the integrity of each resident driver circuit on the I/O Link Interface. This capability did not exist until the introduction of the HPM. There is a possibility that upgrading to an HPM from a PM or APM, while retaining the existing IOPs, could uncover some marginal link drivers. These marginal IOP I/O Link Interface drivers, although still able to function, will generate I/O Link Interface driver errors and the accompanying Soft failures.

If no I/O Link Interface driver errors are reported, then all the drivers on the I/O Link Interface are operating properly. If I/O Link Interface driver errors exist, the offending IOP or High-Performance I/O Link card(s) should be replaced.

Errors that are logged against the I/O Link Interface resident IOP drivers are added to that IOP's (A or B) error count in the IOM I/O Link Information display. The mnemonic IOLDRVER is also displayed according to the IOP's DSA under the column that is labeled LAST ERR.

Errors logged against the HPMM's I/O Link Interface drivers are added into the appropriate CABLE (A or B) ERRORS and TOTAL ERROR counts which are displayed in the HPMM I/O Link Information display. The mnemonic IOLDRVER is also displayed in the field that is labeled LAST COMMUNICATION ERROR.

The normal cable swap algorithm annunciates a Soft failure and disables cable swap. Existing Soft failure codes (#16 – I/O LINK CABLE A FAILURE and #17 – I/O LINK CABLE A FAILURE) are used to report I/O Link Interface driver failures as well as other communications failures.

Some faults, for example power or ground shorts, that produce an HPMM I/O Link Interface driver error can also produce other I/O Link Interface errors such as the LOOPBACK error. When this occurs, the IOLDRVER error may be obscured from the LAST COMMUNICATION ERROR field by another error. Even though some errors may be obscured from the display, they are still recognized, logged, and included in the error statistics.

Continued on next page

4.3.4 HPMM Soft Failure Codes (Table 4-3), Continued

Comm/Control Soft failure error codes

Table 4-3 defines the Soft failure codes for both the HPMM Communications and the Control processors.

The corrective action(s) is identified by a number. Corrective actions are listed in Table 4-1.

Table 4-3 Comm/Control Soft Failure Error Codes

Bit Position	Failure Mnemonic	Display Text	Corrective Action (See Table 4-1)
00	CTRLNRSP	CTRL RESET/WDT EXPIRED	2, 6, 1
01	CTRLFAIL	CTRL PROCESSOR FAILURE	2, 6, 1
02	CMLDFAIL	COMM PROCESSOR LOAD FAILURE	2, 6,1
03	IOLFAIL		1
04	COMMDIAT	COMM PROC DIAG INIT TIMEOUT	2, 1
05	COMMDIAO	COMM PROC DIAG CYCLE OVERFLOW	16
06	MEMPTCHK	GLOBAL RAM EDAC CIRCUITRY	6, 1
07	SRMPTCHK	COM DETECT IOL RAM PARITY CKT	7, 1
08	LMPCCOM	COM LOCAL RAM PARITY CIRCUITRY	6, 1
09	UCNADDR	UCN ADDRESS CHANGE DETECTED	4, 1
10	PWRDROP	TRANSIENT POWER DOWN DETECTED	12, 1
11	SRMPTERR	COMM DETECTED IOL PERR HI-RATE	7, 1
12	SWITCHES		1
13	SOFTERR	PRIVATE RAM PARITY CIRCUITRY	6, 1
14	IOLNORSP	NO RESPONSE FROM IOL #1	7, 1
15	IOLMAXER	IOL MAX COMM ERRORS EXCEEDED	10, 7, 1
16	IOLAFAIL	IOL CABLE A FAILURE	10, 7, 1
17	IOLBFAIL	IOL CABLE B FAILURE	10, 7, 1
18	IOLPRSFL	NO PRIMARY IOL1 COMM TO SECNDY	10, 7, 1
19	UCNPRSFL	NO PRIMARY UCN COMM TO SECNDY	3, 8
20	UCNSCPFL	NO SECNDY UCN COMM TO PRIMARY	3, 8
21	NOSYNCH		1
22	LMBATFAL		1

Continued on next page

Comm/Control Soft failure error codes, continued

Table 4-3 Comm/Control Soft Failure Error Codes, Continued

Bit Position	Failure Mnemonic	Display Text	Corrective Action (See Table 4-1)
23	DUPIOLAD	PRIM/SECNDY DUPLICATE IOM ADDR	5
24	INCOMPFW	INCOMPATIBLE FIRMWARE	6,
25	TSCLOCK	TIMESYNCH CLOCK ERROR/DRIFT	2, 6, 1
26	IOL_TS	IOL TIMESYNCH FAILURE	2, 7, 1
27	TSIOLLAT	TIMESYNCH IOL #1 LATCH ERROR	2, 7, 1
28	TSUCNLAT	TIMESYNCH UCN LATCH ERROR	2, 6, 1
29	COMSTACK	COMM PROC STACK LIMIT OVERFLOW	2, 1
30	COM_SWE	COMM DETECTED LRM PERR HI-RATE	2, 6, 1
31	CTL_SWE	CTRL DETECTED LRM PERR HI-RATE	2, 6, 1
32	GBLRAMPE		1
33	IOLOVRUN	CTRL IOL OVERRUNS	16 1
34	UCNOVRUN	CTRL UCN OVERRUNS	16, 1
35	PPXOVRUN	CTRL POINT PROCESSOR OVERRUNS	16, 1
36	CTRLDIAT	CTRL PROC DIAG INIT TIMEOUT	16, 1
37	CTRLDIAO	CTRL PROC DIAG CYCLE OVERFLOW	16, 1
38	LMPCCTL	CTRL LOCAL RAM PARITY CIRCUITRY	6, 1
39	REDDTRN	CTRL REDUN DATA TRANSFER ERR	9, 6, 1
40	REDDTRK	CTRL REDUN DATA TRACKING ERR	6, 1
41	COMMFAIL	COMM WATCH DOG TIMER EXPIRED	2, 6, 1
42	REDPTRN		1
43	REDBYTE		1
44	REDADAC		1
45	REDADDL	REDUN PRIVATE PATH INIT ERROR	9, 6, 1
46	REDCLRR		1
47	REDPGEN		1
48	REDTRK		1
49	REDFULL		1

Continued on next page

Comm/Control Soft failure error codes, continued

Table 4-3 Comm/Control Soft Failure Error Codes, Continued

Bit Position	Failure Mnemonic	Display Text	Corrective Action (See Table 4-2)
50	REDLOCK	ALT REDUN CABLE APPLIED	18
51	PLCOVRUN	EXCESSIVE COM CPU LOAD	16, 1
52	LCIONRDY	EXCESSIVE CTL CPU LOAD	16, 1
53	KEYDISBL	EXCESSIVE I/O LINK LOAD	16, 1
54	LCLLNOSC	UCN CABLE SWITCH HW FAULT	2, 8, 1
55	LCSYSERR		1
56	LCCKSMFL		1
57	LCIOPPWFL		1
58	LCSWDTFL	IOL PF BUF SIZE EXCEEDED	19
59	LCBATTFL	IOL PS BUF SIZE EXCEEDED	19
60	PCSLFTST	UCN PF BUF SIZE EXCEEDED	19
61	LCSIOMOL	UCN PS BUF SIZE EXCEEDED	19
62	CTLSTACK	CTRL PROC STACK LIMIT OVERFLOW	2, 6, 1
63	LCIOCDFL		1
64	IOLIUNKN		1
65	IOLISTCO	IOL PROC STC OVERRUN	2, 7, 1
66	IOLIREQO	IOL PROC TASK REQUEST OVERFLOW	2, 7, 1
67	IOLIBADR	IOL PROC RESUME NON-WAIT TASK	2, 7, 1
68	IOLIDIAT	IOL PROC DIAG INIT TIMEOUT	2, 1
69	IOLIDIAO	IOL PROC DIAG CYCLE OVERFLOW	2, 7, 1
70	IOLIFTAN		1
71	IOLCBL1A	IOL CABLE 1A FAILURE	10, 7, 1
72	IOLCBL1 B	IOL CABLE 1 B FAILURE	10, 7, 1
73	IOLCBL2A	IOL CABLE 2A FAILURE	1
74	IOLCBL2B	IOL CABLE 2B FAILURE	1
75	SPARE110	NO RESPONSE FROM IOL#2	1
76	SPARE110	IOL #2 WATCH DOG TIMER EXPIRED	1
77	SPARE110	TIMESYNCH IOL #2 LATCH ERROR	1
78	SPARE110	NO PRIMARY IOL2 COMM TO SECNDY	1

Continued on next page

Comm/Control Soft failure error codes, continued

Table 4-3 Comm/Control Soft Failure Error Codes, Continued

Bit Position	Failure Mnemonic	Display Text	Corrective Action (See Table 4-2)
79	SMBATSFL		1
80	SMTSFLT		1
81	LCTSFLT		1
82	IOL_HMRG	HIGH POWER SUPPLY MARGINING	13
83	IOL_LMRG	LOW POWER SUPPLY MARGINING	13
84	IOLIPERR	IOL DETECTED IOL PERR HI-RATE	7, 1
85	IOLPCHKR	IOL DETECT IOL RAM PARITY CKT	7,1
86	SPARE110	UART ACCESSIBILITY ERROR	6, 1
87	SPARE110	BATTERY BACKUP CIRCUITRY FAIL	6, 1
88	STCKLIM	IOL PROC STACK LIMIT OVERFLOW	7, 1
89	SPARE110		1
90	SPARE110		1
91	WDTOFF	WATCH DOG TIMER DISABLED	6, 1
92	CTL_NOTG	NO TOG FROM CTRL PROCESSOR	6, 1
93	DRM_SBE	GLOBAL DRAM EDAC SBE HI-RATE	6, 1
94	CTL CE	CTRL CONSOLE EMULATOR UNLOCKED	17
95	COM_CE	COMM CONSOLE EMULATOR UNLOCKED	17

4.3.5 I/O Link Hard Failure Codes (Table 4-4)

I/O Link processor Hard failure error codes

Table 4-4 provides the I/O Link processor Hard failure codes.

The corrective action(s) that are identified in the table are located in Table 4-1.

Table 4-4 I/O Link Hard Failure Error Codes

Error code	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
00	UNKNOWN	Unknown Hard Failure.	None
01	POWERDWN	Powerdown occurred.	None
02	I NVPRGEX	Unused on I/O Link interface	1
03	EPROMERR	Program checksum error.	2, 7, 1
04	RAMCNTER	RAM contents error.	2, 7, 1
05	RAMADRER	RAM address decoding error.	7
06	DPAERROR	Device Physical Address (DPA) error.	2, 7, 1
07	DSAERROR	Device Soft Address (DSA) error.	2, 7, 1
08	RXBUFOFL	Unused on I/O Link interface	1
09	IOLJA8ER	I/O Link jabber circuit fired.	7
0A	SRAMFAIL	Unused on I/O Link interface.	1
0B	BADPGJMP	Unused on I/O Link interface.	1
0C	ADCINCMP	Unused on I/O Link interface	1
0D	ADOUTOVF	Unused on I/O Link interface.	1
0E	ADOUTUDF	Unused on I/O Link interface.	1
0F	ADCCALER	Unused on I/O Link interface.	1
10	BADDCLTC	Unused on I/O Link interface.	1
11	DMT_TMOT	Dead Man Timer timeout.	2, 7, 1
12	MLTOUTFL	Unused on I/O Link interface.	1
13	DATBUSFL	Unused on I/O Link interface.	1
14	BADDARNG	Unused on I/O Link interface.	1
15	MSTRTMOT	Communications timeout.	2, 6, 1
16	UM51_WDT	UM51 Watch Dog Timer timeout.	2, 7, 1
17	CTRCKTFL	Unused on I/O Link interface.	1

Continued on next page

4.3.5 I/O Link Hard Failure Codes (Table 4-4), Continued

I/O Link processor Hard failure error codes, continued

Table 4-4 I/O Link Hard Failure Error Codes, Continued

Error code	Failure Mnemonic	Description	Corrective Action (See Table 4-1)
18	SOECNTFL	Unused on I/O Link interface.	1
19	OUTCTLFL	Unused on I/O Link interface.	1
1A	PRC TYPE	Wrong processor type.	7
1B to FF	SPARExxx	Unused on I/O Link interface.	1

4.3.6 IOP Hard Failure Codes (Table 4-5)

IOP Hard failure error codes

Table 4-5 defines the Input/Output Processor (IOP) Hard failure codes. The recommended corrective action(s) are included in the table.

Table 4-5 IOP Hard Failure Error Codes

Last Failure Mnemonic	Description	Corrective Action
ADCCALER	Internal calibration signal in the HLAI is off by more than ± 5%.	Replace the HLAI IOP card.
ADCINCMP	A/D conversion incomplete.	Replace the HLAI IOP card.
ADOUTOVF	Not applicable	
ADOUTUDF	A/D reference point conversion value ≤ zero.	Replace the HLAI IOP card.
BADDARNG	AO IOP card DAC load value is NAN or +INF or -INF.	Replace the AO IOP card.
BADDCLTC	AO card detected that DAC IOP card interface latch was bad.	Replace the AO IOP card.
BADPGJMP	Current Calibration/Conversion mode is invalid for this IOP	Select Calibration/Conversion mode that is valid for this IOP
CTRCKTFL	IOP counter failed.	Replace IOP card
DMT_TMOT	Dead man timer timeout	Replace the LLAI IOP card. Call TAC if problem persists.
DPAERROR	A physical device address error.	Replace the IOP card.
DSAERROR	Device software address error.	Replace the IOP card. If multiple IOP cards failed with this code, or a replacement IOP card fails with this same code, the card file file backplane may be bad.
EPROMERR	EPROM checksum error.	Replace the IOP card.
INVPRGEX	Invalid program execution.	Replace the IOP card. If the replacement card provides the same results, call TAC for assistance.
IOLJABER	I/O Link jabber circuit fired.	Replace the IOP card.
MLTOUTFL	More than one output has failed in a DO IOP card. The DO IOP card has failed so the outputs are set to their shed states.	Check for the unexpected presence of an active DO Standby Manual device connected to the FTA. Also, check for blown fuse F17 on the 24 Vdc nonisolated DO FTA or improper TB1-17, 18, 19 connections on the same FTA. Check the FTA wiring, replace the DO IOP card and/or the FTA.
MSTRTMOT	68K timeout.	Applicable to I/O Link Interface only (not an IOP error)
OUTCTLFL	Not applicable	

Continued on next page

IOP Hard failure error codes, continued

Table 4-5 IOP Hard Failure Error Codes, Continued

Last Failure Mnemonic	Description	Corrective Action
POWERDWN	Power down occurred. The IOP card lost power and restarted.	None, unless only a single IOP or group of IOPs exhibit this problem continually when a loss of power should not be occurring in the HPM. Check to see that the IOP is properly inserted in the card file. Also check the seating of the power distribution cables between the card file and the power system.
RAMADRER	RAM address decoding error.	Replace the IOP card.
RAMCNTER	RAM contents error.	Replace the IOP card.
RXBUFOFL	Not applicable	
DATBUSFL	PI data bus diagnostic test failure	Replace the IOP card
SPARE026 to SPARE255	Not used.	N/A
SOECNTFL	SOE counter failure.	Reset IOP. Replace the IOP card if the problem persists
SRAMFAIL	SRAM failure.	Reset IOP. Replace the IOP card if the problem persists
UM51_WDT	Not applicable	
UNKNOWN	Unknown hardware failure.	If an IOP card fails and this code is present during restart, the IOP was disabled, probably by the Watch Dog Timer time-out circuit, ESD, or RFI. Check the situation. Replace the IOP if the problem persists.
WRONGCPU	CPU is not the correct part - 80C31 or 80C32	Applicable to I/O Link Interface only (not presently an IOP error)

4.3.7 IOP Box Soft Failure Codes (Table 4-6)

IOP Box Soft failure error codes

The IOP Box Soft failure codes are defined in Table 4-6. The corrective actions are identified in the table.

Table 4-6 IOP Box Soft Failure Error Codes

Error Code	Failure Mnemonic	Description	Corrective Action
00	UNKNOWN	Null Soft failure. No failure	None.
01	STCOVRUN	Sample time clock overrun.	Investigate a possible I/O Link problem. Data access to the IOP cards may not be operating properly. Check the High-Performance I/O Link card, the I/O Link cable, and the IOP cards.
02	REQOFLOW	IOP task request overflow.	Call TAC for assistance.
03	BADRESUM	IOP executive resumed a nonwaiting task.	Call TAC for assistance.
04	DIAGTMOT	Diagnostics not run in at least 5 seconds indicates a processing overload.	Investigate control point mix/strategy for an excessive load. Otherwise, a possible I/O Link problem exists. Check the High-Performance I/O Link card, the I/O Link cable, and the IOP cards.
05	DIAGOFLO	Entire diagnostic cycle overran the 2-minute allocated time in which diagnostics have to run to completion.	Same as error code 04.
06	FTAMISSG	The FTA is missing.	Install the FTA. If an FTA is present, replace the FTA or check the FTA cable. (Note: For the LLMux, this code refers to the Power Adapter assembly. RTD and TC FTAs are diagnosed by error codes 50 and 51.)
07	EECKSMER	EEPROM (used to hold calibration information in Analog Output IOPs) checksum failure. It usually means an Analog Output IOP is not calibrated properly.	Calibrate the Analog Output IOP card (refer to Section 7 for the procedure). If the error persists, replace the HLAI, or the AO IOP card, or the FTA.
08	EECNTERR	EEPROM counter error. The number of writes to EEPROM has exceeded the safe number (10,000). This could indicate the IOP has not been calibrated because a virgin EEPROM will fail this test.	Same as error code 07.
09	EEFLAGER	EEPROM semaphore (incompletion) error.	Same as error code 07.

Continued on next page

4.3.7 IOP Box Soft Failure Codes (Table 4-6), Continued

IOP Box Soft failure error codes, continued

Table 4-6 IOP Box Soft Failure Error Codes, Continued

Error Code	Failure Mnemonic	Description	Corrective Action
09	EEFLAGER	EEPROM semaphore (incompletion) error.	Same as error code 07.
10	SWTCHERR	No longer used.	No action required.
11	ADRAMCNT	ADP (Analog to Digital Processor – LLAI only) private RAM contents failure.	Replace the appropriate IOP card because the ADP has failed.
12	ADRAMADR	ADP (LLAI only) private RAM address error.	Replace the IOP card.
13	MBRAMCNT	LLAI shared RAM contents failure.	Replace the IOP card.
14	MBRAMADR	LLAI shared RAM address error.	Replace the IOP card.
15	MBCHKMER	LLAI shared RAM checksum error.	Replace the IOP card.
16	ADROMERR	ADP (LLAI only) ROM checksum failure.	Replace the IOP card.
17	BADADPER	Application processor (LLAI or STI) has a communication failure with the High-Performance I/O Link card.	If the error persists, replace the IOP card.
18	ADSTRTUP	ADP (LLAI only) failed on IOP startup.	Replace the IOP card.
19	SCANORUN	Input IOP overran its input scan. Inputs have been lost.	Check for a "chattering" DI point. Another possible cause would be intermittently bad I/O link hardware.
20	SCANURUN	DI IOP scan underrun.	No longer used. No action required.
21	INPTFAIL	Input point failure.	Check which input is failing, then check the hardware for that input. Replace the hardware if required.
22	BADSECRG	DO IOP card secondary regulator is not functioning.	Replace the DO IOP card.
23	OUTPUTFL	Output point failure.	Check which output is failing, then check the hardware for that output. Replace the hardware if required.
24	STCKLIM	Internal stack usage in the 8051 processor is close to the limit.	Call TAC for assistance.

Continued on next page

IOP Box Soft failure error codes, continued

Table 4-6 IOP Box Soft Failure Error Codes, Continued

Error Code	Failure Mnemonic	Description	Corrective Action
25		Not used.	N/A
26	DIAGCTFL	Output loopback circuit is bad.	Replace the appropriate IOP card.
27	ADPCOMFL	I/O Link processor cannot gain access to the shared RAM. Input conversion will be prohibited.	Replace the IOP card.
28	NOACLINE	No external ac line is present in the LLAI. (6 volts ac used for power noise cancellation)	Check optical coupler and associated fuse on the backplane.
29	BADPLUGM	Bad plug-in module on the FTA.	Replace the plug-in module.
30	VTESTFAL	Test Volume Reference Failure. PV is set to NAN by the IOP.	Replace the IOP card.
31	FTAMSMCH	The FTA type and point configuration are mismatched.	Replace the FTA type or reconfigure.
32	VZERO_FL	Zero Reference Volume failure.The PV is set to NAN by the IOP.	Replace the IOP card.
33	BADRJVAL	LLAI reference junction value is bad.	Check that the reference junction wire is correctly implemented on the FTA.
34	BADADPJP	Probable RAM failure in ADP portion.	Replace the LLAI IOP card for the LLAI FTA.
35	ZEROCNFG	Bad configuration byte passed to the ADP.	Check the configuration.
36	FTA1FAIL	LLMux: FTA 1 has a Soft failure.	LLMux: Check FTA 1. SI: Correct the error condition at the device connected to FTA 1.
37	FTA2FAIL	LLMux: FTA 2 has a Soft failure.	LLMux: Check FTA 2. SI: Correct the error condition at the device connected to FTA 2.
38	CALBABRT	Calibration of an IOP card has been aborted during the procedure.	Check the precision voltage/resistance source for accuracy. Also, make sure that the correct calibration procedure is being followed
39	BADCALRF	Calibration reference input is bad.	Replace the HLAI.

Continued on next page

IOP Box Soft failure error codes, continued

Table 4-6 IOP Box Soft Failure Error Codes, Continued

Error Code	Failure Mnemonic	Description	Corrective Action
40	EEFAILED	Output EEPROM write failure.	If an HLAI or AO, replace the IOP. If an LLAI, replace the affected plug-in module.
41	VREFFAIL	LLMUX FTA ref voltage failure	If the problem persists replace the FTA
42	ADOUTUDF[1]	Analog to digital conversion value underflowed (HLAI only).	Check the input wiring at the FTA; possible bad contact. Otherwise, replace the IOP card and/or the FTA.
43	ADOUTCAL	HLAI A/D is out of calibration by more than ±3%.(refer to Section 7).	Calibrate or replace the IOP card (refer to Section 7).
44	BADFLREG	AO IOP failure selection register is bad.	Replace the AO IOP card.
45	BDSNDTC	Bad output module secondary latch.	Replace the IOP. Use a Standby Manual device if nonredundant.
46	BDOUTBFR	Bad output buffer.	Replace IOP. Use Standby Manual device if nonredundant.
47	VCALFAIL	Calibration reference out of range.	Replace the IOP or recalibrate.
48	F1NOTCAL	LLMux: FTA 1 is not calibrated. SI: FTA 1 write buffer has overflowed.	LLMux: Calibrate FTA 1. SI: Reduce the number of writes to the FTA.
49	F2NOTCAL	LLMux: FTA 2 is not calibrated. SI: FTA 2 write buffer has overflowed.	LLMux: Calibrate FTA 2. SI: Reduce the number of writes to the FTA.
50	F1COM_FL	LLMux: FTA 1 fails to communicate. SI: FTA 1 fails to communicate.	Check the connection from the Power Adapter to FTA 1. If the FTA is missing, install the FTA. If the FTA is present, replace the FTA.
51	F2COM_FL	LLMux: FTA 2 fails to communicate. SI: FTA 2 fails to communicate.	Check the connection from the Power Adapter to FTA 2. If the FTA is missing, install the FTA. If the FTA is present, replace the FTA.
52	F1_IDERR	FTA #1 is pinned as #1.	Verify/correct the FTA pinning.
53	F2_IDERR	FTA #2 is pinned as #0.	Verify/correct the FTA pinning.

Continued on next page

[1] Slot Soft failure only. The display is incorrect.

IOP Box Soft failure error codes, continued

Table 4-6 IOP Box Soft Failure Error Codes, Continued

Error Code	Failure Mnemonic	Description	Corrective Action
54	F1VREFFL	FTA 1 has a reference voltage failure.	Replace the FTA.
55	F2VREFFL	FTA 2 has a reference voltage failure.	Replace the FTA.
56	F1CAL_FL	FTA 1 calibration procedure failed.	Recalibrate the FTA.
57	F2CAL_FL	FTA 2 calibration procedure failed.	Recalibrate the FTA.
58	LOSTSYNC	Secondary IOP has lost synchronization.	If the primary IOP is in OK, resynch with the START command. If the primary IOP is in IDLE, resynch with the IDLE command.
59	WRITENBL	AO or DO IOP write enable failure.	Replace the IOP at the earliest convenience. IOP failure can result in indeterminate outputs.
60	MLTINPFL	Multiple input failure detected.	Replace the IOP.
61	REDNDIAG	Redundancy diagnostic failure.	If an AO, replace the FTA's plug-in module after forcing IOP A to be the primary. If an HLAI, replace the IOPs one at a time following database synchronization.
62	Spare062		
63	WRONG_HW	Wrong hardware revision for IOP redundancy	Replace the IOP with an IOP that supports redundancy (proper hardware revision).
64	HWFIFOFL	The DISOE Hardware FIFO diagnostic failed. The PVs of all points are set to BAD.	Replace the IOP.
65	PRVRAMFL	The DISOE Private RAM diagnostic failed. The PVs of all points are set to BAD.	Replace the IOP.
66	SOECLKFL	The DISOE clock failed. The PVs of all points are set to BAD.	Replace the IOP.
67	PVVALDFL	The PV validation diagnostic failed. The PVs of all points are set to BAD.	Replace the IOP.
68	SOECNTFL	The DISOE SOE counter diagnostic failed.	Replace the IOP.

Continued on next page

IOP Box Soft failure error codes, continued

Table 4-6 IOP Box Soft Failure Error Codes, Continued

Error Code	Failure Mnemonic	Description	Corrective Action
69	DTPATHFL	Data path failure.	Replace the FTA when convenient.
70	DTPATHTO	Data path failure.	Replace the FTA when convenient.
71	STMACHFL	The DISOE State Machine diagnostic failed. The PVs of all points are set to BAD.	Recalibrate the FTA.
72 to 255		Not used.	Not applicable.

4.3.8 IOP Slot Soft Failure Codes (Table 4-7)

IOP Slot Soft failure error codes

Table 4-7 defines the Input/Output Processor (IOP) Slot Soft failures. The recommended corrective actions are included in the table.

Table 4-7 IOP Slot Soft Failure Error Codes

Error Code	Failure Mnemonic	Description	Corrective Action
00	Null	No error	
01 to 06		Not used.	N/A
07	EECKSMER	LLAI EEPROM checksum during write.	Replace the FTA plug-in module or recalibrate.
08	EECNTERR	LLAI EEPROM counter error.	Replace the FTA plug-in module or recalibrate.
09 to 20		Not used.	N/A
21	INPTFAIL	Input failure.	Replace the IOP or check the FTA wiring.
22		Not used.	N/A
23	OUTPUTFL	Output failure (AO or DO).	Check the output connection at the FTA. If it is good, try replacing the FTA and/or the appropriate IOP card.
24 to 25		Not used.	N/A
26	DIAGCTFL[2]	Input/output loopback failure for the slot.	Replace the IOP when convenient. Use a Standby Manual device if appropriate.
27 to 28		Not used.	Replace the IOP card. If the replacement card provides the same results, call TAC for assistance.
29	BADPLUGM	Plug-in module failure.	Test that the slot is wired correctly. If it is, replace the FTA plug-in module.
30		Not used.	N/A
31	FTAMSMCH	FTA mismatched with slot configuration.	Reconfigure or replace the FTA.
32 to 34		Not used.	N/A

Continued on next page

[2] Slot Soft failure only. The display is incorrect.

4.3.8 IOP Slot Soft Failure Codes (Table 4-7), Continued

IOP Slot Soft failure error codes, continued

Table 4-7 IOP Slot Soft Failure Error Codes, Continued

Error Code	Failure Mnemonic	Description	Corrective Action
35	BADADPJP	Illegal internal zero configuration attempted on this channel.	Check for an open thermocouple, fuse, or replace the IOP.
36 to 37		Not used.	N/A
38	CALBABRT	Calibration of this slot has aborted.	Check the precision voltage source for accuracy.
39 to 41		Not used.	N/A
42	ADOUTUDF	Analog to digital conversion value under flowed (HLAI only).	Check the input wiring at the FTA; possible open contact. Otherwise, replace the IOP card and/or the FTA.
43 to 255		Not used.	N/A

4.4 Smart Transmitter Interface

Introduction

A fault in an Smart Transmitter Interface (STI) point can be isolated to one of the following areas.

- STI (STIM) IOP
- Associated FTA
- Smart Transmitter device

STI IOP and FTA faults

If a fault occurs in the STI (STIM) IOP or the FTA, the fault can be isolated by the same procedure as was described previously for other IOPs.

Two wire link or Smart Transmitter faults

If the fault is in the 2-wire link or in the transmitter, the PV value on the Universal Station display changes to a **BADPV** value for the particular STI point. Perform the procedure in Table 4-8 to isolate the fault to either the link or the transmitter.

Table 4-8 Two-Wire Link/Smart Transmitter Fault Isolation Procedure

Step	Action
1	Check the Transmitter Status Field on the second page of the Detail Status display. If “Device Not Communicating” or “In Analog Mode” is displayed, proceed to step 2. Otherwise, determine the status of the transmitter by using Table 4-23 and take the appropriate action.
2	Check the status of the transmitter using the Smart Field Communicator (SFC) as described in the appropriate Honeywell publication.
3	If the status check of the transmitter indicates that it has no malfunction, the fault may be in the 2-wire link. Proceed with the following steps. • Disconnect the 2-wire link at the transmitter and at the FTA. Perform a wire continuity test. If necessary, replace the 2-wire link. • If the status check of the transmitter indicates that it is a malfunction, troubleshoot the transmitter according to the procedures provided in the appropriate Honeywell publication.
4	After the fault has been corrected, reload the transmitter data base from the Universal Station.
5	Remove the control loop from the manual mode.

4.5 FTA Redundancy Indicators

Introduction

The switching indicator, DS1, on the High Level Analog Input FTA and the Analog Output FTA indicate different IOP control conditions. Output control of the Analog Output FTA is switched on the FTA between IOP A and IOP B. The inputs to the High Level Analog Input IOPs from the FTA are connected in parallel.

AO FTA redundancy indicator

If the indicator, **DS1**, on the Analog Output FTA is illuminated, IOP A is controlling the FTA's output terminals. When IOP A is controlling the FTA's output terminals, IOP B, the switching module, M1, or the cable between IOP B and the FTA can be replaced.

When the indicator on the Analog Output FTA is extinguished, IOP B is controlling the FTA's output terminals, and IOP A or the cable between IOP A and the FTA can be replaced. The indicator may briefly illuminate during self-test. This is a normal condition.

HLAI FTA redundancy indicator

If the indicator, **DS1**, on the High Level Analog Input FTA is illuminated, IOP A is the primary IOP or available to become the primary IOP. When the indicator on the FTA is not illuminated, IOP A is not available to be the primary IOP.

4.6 Redundant Analog Output IOP Failure Diagnosis

Introduction

The procedure that follows is recommended when encountering a problem with redundant Analog Output IOPs. It is not intended to be a replacement for the experience acquired in the use of redundant Analog Output IOPs, but it should improve your approach to locating, isolating, and correcting a problem.

Considerations

A knowledge of the information provided by the Universal Station displays, detailed in Section 3, and discussions in early subsections of Section 4 is needed to understand a systematic troubleshooting procedure. Consider the following information and suggestions.

Avoid removing IOP A

If at all possible, do not remove IOP A. The IOP A is the IOP connected by cable to the FTA Cable A connector, J1, on the Analog Output FTA.

IOP A preference

Redundancy for the Analog Output IOPs is biased toward IOP A. A hardware bias exists because IOP B (the physical secondary) is connected to the Analog Output FTA through a switching module on the FTA, while IOP A (the physical primary) is connected directly to the FTA circuitry that interfaces the FTA's field wiring outputs.

Replacing the FTA switching module

The switching module can be replaced without disturbing the FTA's outputs when IOP A is the primary IOP because IOP A has a direct connection to the field wiring terminals, independent of the switching module's presence.

Switch to IOP A when a Soft failure occurs

If the IOP pair has a Soft failure because of a redundancy hardware problem, and IOP B is the primary IOP **BSF/SF**** on the HPM Status display] and still in synch, it is important to switch to IOP A before proceeding. Once IOP A becomes the primary IOP, replacement of IOP B, or the switching module on the FTA, can occur without the loss of outputs to the field.

** The "**XX/YY**" represents the status shown on the HPM Status display. The correct interpretation is that "**XX**" is IOP A, and "**YY**" is IOP B. The backup IOP is identified by either "**BKP**" or "**BSF**."

Consider use of an AO Standby Manual device

If the user is conservative, you can always connect an Analog Output Standby Manual device to the FTA and then replace either the Analog Output IOP or the switching module on the FTA. However, you must realize that with the Analog Standby Manual device in place, all control points using these outputs will go into initialization.

Continued on next page

OK/CNF [S] status

If the HPM Status display indicates an **OK/CNF [S]*** status, or any combination of **SF**, **IDL**, or **ISF** for IOP A, the problem is either the cables are improperly wired to the FTA, or the FTA switching module is bad. Do not attempt to disrupt power to IOP A by toggling its upper retractor or remove the IOP. Additional information may be available in the "Status" field on the IOP's Detail Status display.

* The **[S]** represents the synchronization status of the redundant IOP pair. The "**S**" has two background colors, red for **SYNC_FAIL** and yellow for **SYNC_WARNING**. A **SYNC_FAIL** status indicates the IOP has tried several times to synchronize the database between the IOPs with no success. The only way to reinitiate a synchronization for the IOP with a **CFG** status, from the Universal Station, is to send the present state of the communicating IOP to its redundant partner. For example, if the HPM Status display indicates **OK/CFG [S]**, execute the **RUN** command for the pair. If the status is **IDL/CFG [S]**, execute the **IDLE** command. You will see the red "**S**" change color to yellow as synchronization of the IOPs is attempted again.

Replacing the switching module

If it is determined that the switching module is bad, the switching module can be replaced without disturbing the field outputs, as long as IOP A is the primary IOP.

[S] CNF/OK status

If the HPM Status display indicates a ***[S] CNF/OK** status, or any combination of **SF**, **IDL**, or **ISF** for IOP B, the problem is either the cables are improperly wired to the FTA, or the switching module on the FTA is defective. If any of the FTA outputs are in the "on" state, a special problem exists because the removal of the switching module will result in the loss of control output to the device.

* The **[S]** represents the synchronization status of the redundant IOP pair. The "**S**" has two background colors, red for **SYNC_FAIL** and yellow for **SYNC_WARNING**. A **SYNC_FAIL** status indicates the IOP has tried several times to synchronize the database between the IOPs with no success. The only way to reinitiate a synchronization for the IOP with a **CFG** status, from the Universal Station, is to send the present state of the communicating IOP to its redundant partner. For example, if the HPM Status display indicates **OK/CFG [S]**, execute the **RUN** command for the pair. If the status is **IDL/CFG [S]**, execute the **IDLE** command. You will see the red "**S**" change color to yellow as synchronization of the IOPs is attempted again.

Continued on next page

Best solution when replacing switching module

The best solution is to use the Analog Output Standby Manual device to hold the field outputs in a safe state while the IOP or switching module is replaced.

Switching module replacement procedure

The procedure in Table 4-9 is required when any of the outputs are in the "on" state and the switching module is defective.

Table 4-9 Switching Module Replacement Procedure

Step	Action
1	Verify that a current Checkpoint for the problem IOP is available, and if not, save a Checkpoint before proceeding.
2	Connect an Analog Output Standby Manual device to the FTA and balance the outputs.
3	On the Analog Output Standby Manual device, switch control of the FTA output field terminals from the IOP to the Analog Standby Manual device.
4	Remove the switching module on the FTA and then disrupt power at IOP A.
5	IOP A should now be in the idle state and the primary IOP. Restore the Checkpoint to the IOP and start the IOP. IOP B should be in Soft failure with a **MISSING FTA** status and should synchronize with IOP A.
6	Replace the switching module on the FTA and verify that IOP B clears its Soft failure and synchronizes with IOP A. The HPM Status display should now indicate **OK/BKP**.
7	Align the outputs with those on the Analog Output Standby Manual device and switch control of the field terminals from the Analog Standby Manual device back to the IOP.

IOP B should be secondary

Always remember that IOP B should be the secondary during normal operation to provide the best subsystem availability. IOP B's functions should be periodically tested using the procedure found in subsection 8.3.1.

4.7 Battery Backup Exhaustion

Introduction

When the 48 Vdc backup batteries become exhausted after approximately 20 minutes of operation because of Power Supply Module failure or loss of ac power, the 24 Vdc output from the Power System collapses abruptly to zero. Until that time, the 24 Vdc output from the Power System remains within specification. There is no gradual decay of the 24 Vdc output.

Loss of 24 Vdc

If the 24 Vdc output is lost, the control signals from the Analog Output and Digital Output FTAs in the cabinet or cabinet complex powered by the particular Power System will become inactive, with the AO FTA outputs dropping to a nonpowered condition and the DO FTAs output relays assuming their deenergized state.

Multiple battery backup

Be aware that other Power Systems (additional cabinets) with battery backup that may be in the High-Performance Process Manager subsystem may not exhaust their battery capacity at the same time. The effect of the situation on the overall control and safety of the process being controlled should be considered.

US response to 48 Vdc battery failure

As a result of the loss of 24 Vdc power, the HPM cabinet becomes nonpowered. The HPM status displays at the Universal Station (US) will show the status of the HPMMs to be **OFFNET** or **UNKNOWN**. Without access to the HPMMs, the IOP displays are not available.

4.8 HPMM Card and Module Indicators

Application of power

When power is first applied to the HPMM, check the **Power** indicator on each HPMM card and the HPM UCN Interface module. The **Power** indicator should be illuminated whenever dc power is present.

Status indicators and Alphanumeric display

After a few seconds, the **Status** indicator on the High-Performance Communications/Control and High-Performance I/O Link cards should be illuminated and the alphanumeric display at the front of the High-Performance Communications/Control cards should display an code that indicates the HPMM is in the Alive state, such as **Axxx**.

HPM UCN Interface module

Either the **Rx-A** or **Rx-B** indicator at the front of the HPM UCN Interface module should be illuminated, indicating which UCN cable is active. Normally, the Transmit indicator will flicker to indicate communication with the Universal Control Network.

Continued on next page

Indicator functionality

Table 4-10 describes the functionality of the indicators at the front of the High-Performance Communications/Control and High-Performance I/O Link cards, and the HPM UCN Interface module.

Table 4-10 HPMM Card and Module Indicators

Card/Module Type	Indicator	Functionality
High-Performance Comm/Control	Power	The LED illuminates when power is applied to the HPMM card file. If the LED is not illuminated, check the Power System, the power cables to the card file, and the High-Performance I/O Link card. The High-Performance I/O Link card provides power to itself, the High-Performance Comm/Control card and the HPM UCN Interface module.
	Status	When power is applied to the HPMM card file, the indicator illuminates and self-test begins. If the LED extinguishes after a few seconds, the self-test has encountered a Hard failure. The LED blinks once a second if the self-test encounters a failure. The LED remains on continuously if there are no failures.
High-Performance I/O Link	Power	The LED should be illuminated when power is applied to the HPMM card file. If the LED is not illuminated, check the Power System and the power cables to the card file. The High-Performance I/O Link card provides logic power to itself, the High-Performance Comm/Control card, and the HPM UCN Interface module. A field replaceable 3.2 amp. fuse on the card provides overload protection for the +5 volt HPMM supply on this board.
	Status	The Status LED illuminates when the HPMM personality has been successfully downloaded. If a failure occurs, the LED extinguishes.

Continued on next page

Indicator functionality, continued

Table 4-10 HPMM Card and Module Indicators, Continued

UCN Interface Module	Power	The LED is illuminated when power is applied to the HPMM card file. If the LED is not illuminated, check the Power System, the power cables to the card file, and the High-Performance I/O Link card. The High-Performance I/O Link card provides power to the card and the HPM UCN Interface module through a fuse which is mounted on the backplane immediately behind the module itself..
	Transmit	The LED flickers when transmitting data. This does not occur unless the HPMM is loaded or is in network test mode. Before the HPMM personality is downloaded, the LED will blink occasionally.
	Rx-A	The indicator illuminates (or flickers rapidly) when the UCN A cable is active.
	Rx-B	The indicator illuminates (or flickers rapidly) when the UCN B cable is active.

High-Performance Comm/Control card Status indicator

During power startup, the High-Performance Comm/Control card's internal diagnostic tests should complete after approximately 10 seconds, and the **Status** indicator should stay on, indicating the diagnostic tests were successful. If the **Status** indicator does not stay on, the card has detected a hardware or firmware failure.

High-Performance I/O Link card Status indicator

The **Status** indicator does not indicate whether or not the High-Performance I/O Link card's internal diagnostic tests were successfully completed. The **Status** indicator illuminates only after the HPMM's personality has been has been successfully downloaded. A failure detected after the personality is loaded (HPMM is in operation) will cause the Status indicator to turn off.

HPM UCN Interface module Transmit indicator

On the HPM UCN Interface module, the **Transmit** indicator is used to indicate that the card is transmitting data on the UCN and flickers periodically. Many times the off state of this indicator is very short. If the Network Interface Module (NIM) has not been downloaded and token passing has not begun, the **Transmit** indicator remains off. See the *High-Performance Process Manager Checkout* manual.

Continued on next page

Power and Status indicators

Check the **Power** and **Status** indicators on both cards and the HPM UCN Interface module. If any of the indicators are off, troubleshoot the cause based on descriptions and checks previously described. Replace the failed card or module by using the appropriate procedure described in Section 6.

HPMM fuse

The HPMM card set is powered through a 3.2 A fast-action fuse on the High-Performance I/O Link card. If the fuse is blown, power to the entire HPMM card set is removed. If either HPMM cards or its UCN Interface module has its **Power** indicator illuminated, the status of the fuse on the High-Performance I/O Link card is good.

UCN Interface Module fuse

The UCN Interface Module is supplied regulated dc power from the High-Performance I/O Link card through a 2 amp. fuse on the backplane. This fuse is located immediately to the right of the leftmost connector on the backplane. Removal of the UCN Interface Module is required to gain access for replacement of this fuse.

Note: If the same 7-Slot or 15-Slot card file is used as an IOP card file, the fuse will provide power protection for the IOP (and associated FTA) in the leftmost card slot.

HPMM Card extractors

If the upper card extractor on either the High-Performance Communications/Control card or High-Performance I/O Link card is unlocked and lifted slightly, power is disconnected from the card.

The 24 Vdc from the Power System is distributed on the card file backplane from the backplane's power connectors to the High-Performance Communications/Control card. On the card, it passes through a switch that is controlled by the upper card extractor back through the backplane to the High-Performance I/O Link card.

On the High-Performance I/O Link card, it passes through a switch that is controlled by the upper card extractor, through a 3.2 Amp. fuse, to the a voltage converter on the card that produces +5 Vdc that is distributed internally to the High-Performance I/O Link card and externally through the backplane to the High-Performance Communications/Control, and the UCN Interface module.

4.9 HPMM Alphanumeric Display

Introduction

The High-Performance Comm/Control card has a four character alphanumeric display at the front of the card that provides the following types of diagnostic information.

- Runtime Operation – Provides indication of normal HPMM operation which includes the HPMM state, primary/secondary status, and UCN node address (number).
- Failure Status – Display startup, or UCN load or Runtime failure status information
- Cold/Warm Startup Diagnostics – Displays the **STRT** status during the startup diagnostic tests, system bootstrap operations, and software integrated checks.

Detailed Display switch

The amount of detailed information that is displayed can be conditionally enabled by the use of the Detailed Display switch that is located in a recess behind the front panel on the High-Performance Comm/Control card. Use of the switch determines whether detailed information such as test sequence numbers or non-detailed messages that indicate the general phase of HPMM validation/transition/operation. In general, the Detailed-display switch is used primarily for detailed Hard failure analysis.

Rapidly changing of display contents

When the Detailed Display mode (switch) is enabled, the alphanumeric display will frequently show a rapidly changing display content as the various detailed sequences are cycled through. It is impossible to distinguish each unique sequence number displayed. The value lies in the test number/indication displayed when a particular sequence fails to complete (hangs).

Detailed HPMM sequence tables are provided in subsections 4.9.3 thru 4.9.7.

4.9.1 Alphanumeric Display Format

Introduction

The High-Performance Comm/Control card has a four digit alphanumeric display. Generally, the left one or two most significant positions on the display indicate the state of the HPMM with alpha characters, and the right two positions on the display indicate either a test sequence number or a UCN node number with numeric characters. In addition, there are generic text messages that describe the overall phase of the HPMM.

UCN node number

When displaying the UCN node number, it is important to realize that the HPMM has no concept of redundancy while in the Alive, Loading, or Fail state. Therefore, at best, the HPMM knows the user configured UCN node number (pinned odd address only) and the physical card file number (pinned), and whether it resides in a 7 or 15 slot HPM backplane. This information produces the following methods of uniquely displaying a UCN node number at all times.

fnn **nn** represents the user configured decimal UCN node number (01-64) preceded by a physical position indicator during the Alive, Loading. and Fail HPM states.

The actual physical position indicators are represented as “L” and “R” to indicate residency in a 7-Slot card file and “1” and “2” to indicate residency in the file-1 and file-2 15-Slot backplanes.Although this information is inconsistent when viewed from the LCN, it eliminates the ambiguity of having another HPMM node in the Alive, Loading, or Fail state display the identical UCN node number of its redundant partner in the Idle or OK state.

nn **nn** represents the decimal UCN node number (01-64) during normal HPMM Runtime operation. The primary (or nonredundant configured) HPMM node displays the user configured odd node address, and the secondary HPMM, if configured and loaded, displays the even node address. This is consistent with the information that is viewed from the LCN.

Continued on next page

4.9.1 Alphanumeric Display Format, Continued

Format descriptions

Using the UCN node number conventions described on the previous page, the alphanumeric display formats are described in Table 4-11.

Table 4-11 Alphanumeric Display Formats

Condition	Format	Description
Alive State	Afnn	Indicates the successful Cold startup of the HPMM Communications processor. In this state the Communications processor loops indefinitely while performing background diagnostics and waiting for a UCN download to occur. The Control processor and I/O Link processor are held initialized. This display message blinks at a 1/2 second rate to indicate the Communications processor is still running.
Backup State	B nn	Indicates the personalities of the Communications, Control, and I/O Link processors have been loaded into the secondary HPMM, or the primary HPMM has successfully transitioned to the synchronized secondary status. This display does not blink.
Backup Soft Fail State	BSnn	Indicates that the HPMM has transitioned to the Backup Soft Fail state.
Fail State	Ffnn	Indicates that the HPMM has transitioned to the Fail state. If the Detailed-display switch is not engaged after a failure is noted, the display continues to blink showing the Ffnn. If the Detailed Display switch is engaged after a failure is noted, the display alternates between the Communications processor and Control processor crash code displays and the Fail state display as long as the failure condition permits the Communications processor to maintain the display. Refer to subsection 4.3.2 for descriptions of the Communications and Control processor Hard failure codes. Since the Communications and Control processor crash codes are not all unique to the processors, they are preceded by a flag in the display sequence (COMM/CTRL). For example, Fail state, COMM flag, Communications processor Hard failure code, CTRL flag, Control processor Hard failure code, blank, Fail state, --pattern repeats. Note that prior to successfully loading the HPMM, the Control processor is held initialized. Therefore, only the code for the Communications Hard failure code is significant. In this case the Control processor code would be null.
Idle State	I nn	Indicates that the HPMM personalities for the Communications, Control, and I/O Link processors have been loaded, and the HPMM has transitioned to the Idle state or has been placed in the idle state from the Universal Station display.
Idle Soft Fail State	ISnn	Indicates that the HPMM has transitioned to the Idle Soft Fail state.
Loading State	Lfnn	Indicates that the HPMM is currently in the process of down loading the HPMM personality from the LCN. This display blinks at a 1/2 second rate to indicate the Communications processor is still running.

Continued on next page

Format descriptions, continued

Table 4-11 Alphanumeric Display Formats, Continued

Run State	OKnn	Indicates the HPMM has transitioned to the Run state and is the primary HPMM. This display does not blink.
Run Soft Fail State	SFnn	Indicates that the HPMM has transitioned to the Run Soft Fail State. This display does not blink.
Startup	STRT	Indicates that the HPM is performing its Cold or Ram Retention Startup processing. This generic message does not blink, and it is only available when the HPMM Diagnostic detailed-display mode (switch) is not enabled. Otherwise, (with the detailed display mode enabled) this display scrolls through the test sequence numbers (i.e. T xx) of the Cold or RAM Retention startup diagnostics.
Swap Primary	SWAP	This message is momentarily displayed by the primary HPMM while transitioning to secondary status. This generic message does not blink, and it is only available when the HPM alphanumeric detailed-display mode (switch) is not enabled. Otherwise (with the detailed-display enabled), this display scrolls through the test sequence numbers (i.e. Txx) of the RAM Retention startup diagnostics required to reach the Secondary status. Note that there is no visible delay while the secondary HPMM transitions to the primary status.
Synchronize Secondary	SYNC	This message is temporarily displayed by a Secondary HPMM while performing database synchronization with the Primary HPMM. It indicates that the Personalities of the High-Performance Comm/Control and High-Performance I/O Link cards have been loaded into the secondary HPMM or that a Primary HPMM has successfully transitioned to the non-synchronized Secondary status (See “B nn” above). This display does not blink.
Test Sequence Number	T xx	The display provides the hexadecimal test sequence number, “xx,” which is performed during a HPMM Startup. The test sequence numbers are unique for both the Communications and Control processors. (See Table 4-1 for a complete list) The test sequence numbers are displayed only when the detailed-display mode (switch) has been previously enabled (since the last power cycle). Otherwise, the appropriate generic message is displayed (for example, STRT, Afnn, SWAP).

Unsynchronized secondary HPMM

Note that a unsynchronized secondary HPMM displays **I nn** instead of **B nn** since this is a transitional state.

4.9.2 Notification Displays

Introduction

In addition to the standard display formats, the alphanumeric display provides the user with special event notification. Notification messages blink at a 1/2 second rate.

Soft failure

Soft failure conditions which require more than a blinking Status LED are also conveyed through the Alphanumeric display as user notification messages.

Note that **any** Soft failure status is indicated by the blinking Status LED on the High-Performance Comm/Control card. This is true for the entire Process Manager family

Message descriptions

The notification messages are described in Table 4-12.

Table 4-12 User Notification Message Formats

Message	Format	Description
Control Processor Failure	FCTL	Notifies the user that the Control processor has failed in a nonredundant HPMM configuration. Since this is considered a Soft failure condition, the High-Performance Communications/Control card's **Status** indicator blinks at a 1/2 second rate.
Factory Test	FTST	Notification that the Factory Test mode is enabled. At this point, a subset of startup diagnostics has been successfully completed, the Comm Console Emulator has been initialized, and the Communications processor lops indefinitely. The Control and I/O Link processors are held in the reset state. Note the LLC initialization does not occur when the Factory Test mode is enabled.
I/O Simulation Mode	SIML	Notifies the user that the Communications and Control processors are executing I/O simulation software. This display blinks at a 1/2 second rate.
UCN Token Holder Test	UTST	Notifies the user that the UCN Token Holder Test mode has been invoked through a backplane jumper. (For factory use only.)

4.9.3 Cold HPMM Startup Display Sequences

Cold start scenarios

A cold HPMM Startup is done any time that power is applied to the HPMM card set and the contents of the HPMM memory is not valid. A Cold Startup is also performed when the **RECOVER** target on the HPM Status display is used to reset a Hard failure condition in the HPMM.

When an HPMM Cold Startup is performed, only the Communications processor is released from reset and it executes from the Startup and Base Utilities firmware. Therefore, the information displayed during startup reflects the Communications processor's powerup diagnostics, followed by the transition to the HPMM Alive state.

Startup sequence

An example of a (short) HPMM Startup display sequence is listed in Table 4-13 for the Detailed Display mode and non-Detailed Display mode.

Table 4-13 Alphanumeric Display for a Normal Startup Sequence

Detailed Display	Non-Detailed Display	Description
STRT	STRT	Begin Communications processor firmware based tests.
T 0D	STRT	Global DRAM EDAC sweep
T 13	STRT	Global DRAM initialization
T 17	STRT	Comm Local RAM destructive pattern test
T 1B	STRT	Comm Local RAM initialization
T 21	STRT	UCN TBC Private RAM destructive pattern test
T 25	STRT	UCN TBC Private RAM Initialization
T 4F	STRT	Initialize the (FW resident) LLC Communications layer
A139	A139	Alive state (file 1, UCN node 39)

Continued on next page

Startup/Factory Test mode sequence

If the Factory Test mode had been selected, the Startup sequence would end prior to LLC initialization as listed in Table 4-14 for the Detailed-display mode and non-Detailed Display mode.

Table 4-14 Alphanumeric Display for Startup/Factory Test Mode Sequence

Detailed Display	Non-Detailed Display	Description
STRT	STRT	Begin Communications processor firmware based tests.
T 0D	STRT	Global DRAM EDAC sweep
T 13	STRT	Global DRAM initialization
T 17	STRT	Comm Local RAM destructive pattern test
T 1B	STRT	Comm Local RAM initialization
T 21	STRT	UCN TBC Private RAM destructive pattern test
T 25	STRT	UCN TBC Private RAM Initialization
T 4C	STRT	Transition to the FW Alive state
AR00	AR00	Alive state (UCN node 00, Right file position)
FTST	FTST	Factor Test mode notification
AR00	AR00	Status is displayed for 1/2 second.
FTST	FTST	Notification is displayed for 1/2 second.

Continued on next page

Startup/HPMM failure sequence

An HPMM failure during or after a Startup results in alternating failure and Communications processor Hard failure code. This is dependent upon whether the Detailed Display mode (switch) is enabled. The description in Table 4-15 is an example of a sequence when a spurious interrupt failure occurs listing both the Detailed Display mode and non-Detailed Display mode.

Table 4-15 Alphanumeric Display for HPMM Cold Startup Failure Sequence

Detailed Display	Non-Detailed Display	Description
A239	A239	Alive state (file 2, UCN node 39)
F239	F239	Failure (file 2, UCN node 39)
COMM	F239	Flag – Communications processor failure code follows
0057	F239	Communications processor failure: bad or unexpected exception.
CTRL	F239	Flag – Control processor failure code follows.
NULL	F239	Control processor failure code. No failure reported (because Control processor was still being held in reset condition at this point).
The failure pattern repeats		
COMM	F239	Flag – Communications processor failure code follows.
. . .	F239	. . .

ATTENTION

ATTENTION—The non-Detailed Display mode blinks at a 1/2 second rate when the failure is displayed.

4.9.4 HPMM Load Display Sequence

HPMM Load display sequence

The HPMM remains in the Alive state until a UCN download is initiated at the Universal Station. Midway through the loading process, the Control processor is released from reset to perform its local Startup diagnostics. The loading then continues by using the Communications processor.

Alphanumeric display sequence for HPMM load

An example of the Alphanumeric display sequence during the personality download process is listed in Table 4-16 for the Detailed Display mode and non-Detailed Display mode.

Table 4-16 Alphanumeric Display for Load Sequence

Detailed Display	Non-Detailed Display	Description
AR07	AR07	In the Alive state (right file, UCN node 7)
LR07 . . . LR07	LR07 . . . LR07	Start the Communications processor's personality image download. Display blinks at 1/2 second rate Complete Communications processor personality image download.
T 5B	LR07	Initialize the (SW resident) LLC Communications layer
LR07 . . LR07	LR07 . . LR07	Start Control processor personality image download. Continue with Control processor personality download.
T 5E	LR07	Monitor Control processor local State Change (i.e. release Control processor from the reset state).
T 70	LR07	Control processor Local RAM destructive pattern test
T 98	LR07	Control processor transition to the SW Alive state.
LR07 . . . LR07	LR07 . . . LR07	Continue with the Control processor personality image download (i.e. Control Local RAM portion). Complete the Control processor personality image download.
T A5	LR07	I/O Link RAM destructive pattern test
T B4	LR07	Transition I/O Link processor to Idle state.
T FB	LR07	Backup Local RAM into Global RAM

Continued on next page

Alphanumeric display sequence for HPMM load, continued

Table 4-16 Alphanumeric Display for Load Sequence, Continued

Detailed Display	Non-Detailed Display	Description
T FE	LR07	Transition to MTOS
I 07	I 07	HPMM download is completed. This is the HPMM idle state. (The Idle state display does not blink.)

ATTENTION

ATTENTION—The **Lxxx** message blinks at a 1/2 second rate.

4.9.5 Nonredundant HPM Failure Sequences (After Load)

Comm or I/O Link processor failure (nonredundant HPMM)

A Communications or I/O Link processor failure of a nonredundant HPMM (after transitioning to the Idle or Run state) results in a blinking Fxxx indication. Enabling the detailed display mode using the Detailed Display switch results in a sequenced Fail/Comm error/Control error display. Table 4-17 lists the display sequence for both the Detailed Display and non-Detailed Display modes.

Table 4-17 Communications/I/O Link Processor Failure Display Sequence

Detailed Display	Non-Detailed Display	Description
OK39	OK39	In the Run state (UCN node 39). This display does not blink.
F239	F239	Fail (UCN node 39, file position 2) The Non-detailed failure display blinks at a 1/2 second rate.
COMM	F239	Flag – Communications processor failure follows.
0010	F239	Communications processor failure: Local RAM parity error.
CTRL	F239	Flag – Control processor error code follows.
FFF3	F239	Control processor failure code: No response from Communications processor.
	F239	Failure display repeats
F239	F239	Fail (UCN node 39, file position 2)
COMM	F239	Flag – Communications processor failure follows.
.	.	
.	.	

Continued on next page

4.9.5 Nonredundant HPM Failure Sequences (After Load), Continued

Control processor failure (nonredundant HPM)

A Control processor failure of a nonredundant HPM (after transitioning to the Idle or Run state) results in a sequencing display of **IDLE** or **OK** alternating with FCTL. If the Detailed Display mode (switch) is enabled, a failure code is displayed in the sequence. Table 4-18 lists the sequences.

Table 4-18 Control Processor Failure Display Sequence

Detailed Display	Non-Detailed Display	Description
OK39	OK39	In the Run state (UCN node 39). This display does not blink.
SF39	SF39	Run Soft Fail state. (UCN node 39)
COMM	FCTL	Flag – Communications processor failure code follows.
NULL	SF39	Communications processor failure. No failure reported.
CTRL	FCTL	Flag – Control processor failure code follows.
004E	SF39	Control processor failure code: No response from Communications processor
blank	FCTL	
Detailed Display error sequence repeats		
SF39	SF39	Run Soft Fail state. (UCN node 39)
COMM	FCTL	FLag -- Communications processor failure code follows.
.	.	
.	.	

4.9.6 RAM Retention Startup Sequence

RAM Retention Startup sequence

An HPMM RAM Retention startup is performed whenever power is restored and the CMOS memory battery backup was successful in maintaining the integrity of the operating personality software and database in the RAM memory.

When an HPMM RAM Retention Startup process is performed, only the Communications processor is initially released from reset and executes from the Startup and Base Utility firmware. Once a RAM Retention Startup is considered possible, program execute control is transferred to the previously loaded Communications processor software image. The Control processor and I/O Link processors are then released so that they can verify their respective Startup conditions. Table 4-19 lists a HPMM RAM Retention startup to Run state.

Table 4-19 RAM Retention Startup Display Sequence

Detailed Display	Non-Detailed Display	Description
OK39	OK39	In the Run state (UCN node 39). This display does not blink.
STRT	STRT	Communications processor based tests
T 0D	STRT	Global DRAM EDAC sweep
T 13	STRT	Global DRAM initialization
T 17	STRT	Communications processor Local RAM destructive pattern test
T 1B	STRT	Communications processor Local RAM initialization
T 21	STRT	UCN TBC Private RAM destructive pattern test
T 25	STRT	UCN TBC Private RAM initialization
T 3E	STRT	Communications processor builds memory reference table.
T 59	STRT	Transition to the SW Alive state.
T 5E	STRT	Monitor Control processor local state change (i.e release Control processor from reset state)
T 70	STRT	Control processor Local RAM destructive pattern test
T 76	STRT	Control processor Local RAM initialization
T 8E	STRT	Control processor builds memory reference table
T A5	STRT	I/O Link RAM destructive pattern test
T B4	STRT	Transition I/O Link processor to the Idle state.
T FE	STRT	Transition to MTOS
OK39	OK39	Run state (UCN node 39)

4.9.7 Redundancy Display Sequences

HPMM redundancy sequence

Each redundant HPMM partner conforms to the Startup sequences as described earlier in this section. In addition, upon receiving a Swap command, the primary HPMM temporarily displays the **SWAP** text while transitioning to a secondary status. However, there is no visible delay while the secondary HPMM transitions to a primary status. An example of the this sequence is given in the table below.

SWAP sequence (Detailed Display mode)

An example of a display sequence during the HPMM swapping process with the Detailed Display mode enabled is listed in Figure 4-20 for HPMM 1 and HPMM 2.

Table 4-20 Alphanumeric Display for HPMM Swapping Sequence (Detailed Display Mode)

HPMM 1	HPMM 2	Description
OK39	B 40	Run state (UCN node 39 = primary/UCN node 40 = Backup)
SWAP	OK39	HPMM swap command received
T 17	OK39	Communications processor Local RAM destructive pattern test
T 1B	OK39	Communications processor Local RAM initialization
T 21	OK39	UCN TBC Private RAM destructive pattern test
T 25	OK39	UCN TBC Private RAM initialization
T 3E	OK39	Communications processor builds memory reference table.
T 59	OK39	Transition to the SW Alive state.
T 5E	OK39	Monitor Control processor local state change (i.e release Control processor from reset state)
T 70	OK39	Control processor Local RAM destructive pattern test
T 76	OK39	Control processor Local RAM initialization
T 8E	OK39	Control processor builds memory reference table
T A5	OK39	I/O Link RAM destructive pattern test
T B4	OK39	Transition I/O Link processor to the Idle state.
T FE	OK39	Transition to MTOS
SYNC	OK39	Secondary HPMM performing database synchronization
B 40	OK39	HPMM swap complete

Continued on next page

4.9.7 Redundancy Display Sequences, Continued

SWAP sequence (non-Detailed-Display mode)

If the Detailed Display mode is not enabled, then the swap sequence described on the previous page would not display any of the test sequence numbers as listed in Table 4-21 for HPMM 1 and HPMM 2.

Table 4-21 Alphanumeric Display for HPMM Swapping Sequence (Non-Detailed Display Mode)

HPMM 1	HPMM 2	Description
OK39	B 40	Run state (UCN node 39)
SWAP	OK39	HPMM swap command received
SWAP . . . SWAP	OK39 OK39	HPMM 1 begins RAM Retention startup diagnostics. HPMM 1 completes RAM Retention startup diagnostics.
SYNC	OK39	Secondary HPMM performs database synchronization
B 40	OK39	HPMM swap complete

HPMM failover

In the event of an HPMM failover, the primary HPMM transitions to the Fail state and the secondary HPMM becomes the primary.

Continued on next page

Failover sequence (Detailed Display mode)

An example of a display sequence for a failover when a RAM parity error occurs with the Detailed Display mode enabled is listed in Table 4-22 for HPMM 1 and HPMM 2.

Table 4-22 Alphanumeric Display for Failover HPMM Swapping Sequence (Detailed Display Mode)

HPMM 1	HPMM 2	Description
OK39	B 40	Run state (UCN node 39)
F139	OK39	HPMM 1 failure
COMM	OK39	Flag -- Communications processor Hard failure code is next
0010	OK39	HPMM 1 Communications processor failure: Local RAM parity error.
CTRL	OK39	Flag -- Control processor Hard failure code is next
FFF3	OK39	HPMM (file 1) Control processor failure: No response from Communications processor.
Blank	OK39	
F139	OK39	HPMM 1 failure
COMM	OK39	Flag -- processor Hard failure code is next
0010	OK39	HPMM 1 Communications processor failure: Local RAM parity error.
CTRL	OK39	Flag -- Control processor Hard failure code is next
FFF3	OK39	HPMM (file 1) Control processor failure: No response from Communications processor.
The above failure pattern repeats indefinitely or until the Detailed-display mode is disabled.		

Continued on next page

Failover display sequence (non-Detailed Display mode)

An example of a display sequence for a failover when a RAM parity error occurs with the Detailed Display mode not invoked is listed in Table 4-23 for HPMM 1 and HPMM 2.

Table 4-23 Alphanumeric Display for Failover HPMM Swapping Sequence (Non-Detailed Display Mode)

HPMM 1	HPMM 2	Description
OK39	B 40	Run state (UCN node 39)
F139	OK39	HPMM 1 failure
blank		
F139	OK39	HPMM 1 failure
blank		
The failure pattern repeats and blinks (F139, blank, F139, blank, - - -.)		

4.9.8 HPMM Alphanumeric Display Blanking

HPMM alphanumeric display blanking

The HPMM's Communications processor is the designated owner of the Alphanumeric display and is responsible for maintaining the display with current information. In the event of a Communications processor failure, it is undesirable for the alphanumeric display to latch erroneous information. To prevent this situation from occurring, the alphanumeric display is blanked by the hardware if the Communications processor Watch Dog Timer (WDT) times out. This covers any ungraceful Communications processor failures scenarios.

It is possible to override the alphanumeric display blanking by pressing and holding the Detailed Display switch on the High-Performance Comm/Control card. The information gained by doing this cannot be guaranteed to be correct or meaningful.

Control processor WDT timeout

In the event of a HPMM Control processor Watch Dog Timer (WDT) timeout, the operation of the alphanumeric display is unaffected except that the Communications processor displays the appropriate failure information to indicate that the Control processor's WDT has timed out.

4.9.9 Listing of Diagnostic Tests

Test List

Table 4-24 lists all of the existing diagnostic tests. They are listed in step number order. These diagnostic tests are not necessarily executed in sequential order. The sequences were defined earlier in this section.

Table 4-24 Diagnostic Test Listing

Sequence Number	Label	Description
00	None	Null sequence number
01		Spare
02	CMF_ROMTST	ROM checksum validation
03		Spare
04		Spare
05	CMF_CPUTST	CPU Register test
06		Spare
07	CMF_QKDRAM	Quick DRAM accessibility test
08		Spare
09	CMF_GRMSYS	Initialize system portion of Global DRAM
0A		Spare
0B	CMF_ASICREG	ASIC Register accessibility test
0C		Spare
0D	CMF_GRMPAR	Global DRAM EDAC sweep
0E		Spare
0F	CMF_GRMDRT	Global DRAM destructive pattern test
10		Spare
11	CMF_GRM_BWL	Global DRAM B/W/L decode test
12		Spare
13	CMF_GRMCLRR	Global DRAM initialization
14		Spare
15	CMF_GRMPCHK	Global DRAM EDAC circuitry test
16		Spare
17	CMF_LRMDRT	Local SRAM destructive pattern test
18		Spare

Continued on next page

Test List, continued

Table 4-24 Diagnostic Test Listing, Continued

Sequence Number	Label	Description
19	CMF_LRM_BWL	Local SRAM B/W/L decode test
1 A		Spare
1 B	CMF_LRMCLRR	Local SRAM initialization
1 C		Spare
1 D	CMF_LRMPCHK	Local SRAM parity circuitry test
1 E		Spare
1 F	CMF_PRMPCHK	UCN TBC Private SRAM parity circuitry test
20		Spare
21	CMF_PRMDRT	UCN TBC Private SRAM destructive pattern test
22		Spare
23	CMF_PRM_BW	UCN TBC Private SRAM B/W decode test
24		Spare
25	CMF_PRMCLRR	UCN TBC Private SRAM initialization
26		Spare
27		Spare
28	CMF_BLDVECT	Build Exception Vector table
29		Spare
2A	CMF_BLDMRF	Build Memory Reference table
2B		Spare
2C		Spare
2D		Spare
2E		Spare
2F		Spare
30		Spare
31	CMF_TIMER	Timer comparison test
32		Spare

Continued on next page

Test List, continued

Table 4-24 Diagnostic Test Listing, Continued

Sequence Number	Label	Description
33		Spare
34	CMF_GETSLOT	Get Slot address and verify odd parity
35	CMF_GETFILE	Get File address and verify odd parity
36	CMF_GETUCN	Get UCN address and verify odd parity
37		Spare
38		Spare
39	CMF_EEPRMC	COMM/CTRL Serial EEPROM access test
3A		Spare
3B	CMF_EEPRMU	UCN I/F Serial EEPROM access test
3C		Spare
3D		Spare
3E	CMF_FV_EXC	Force and verify Exception test
3F		Spare
40		Spare
41	CMF_COLD	HPM COLD startup
42		Spare
43	CMF_WARM	HPM RAM retention startup
44		Spare
45		Spare
46	CMF_RBLDVEC	Rebuild Exception Vector table
47		Spare
48		Spare
49	CMF_CEINIT	FW Console Emulator initialization
4A	CMF_PRCTYPE	Verify correct processor type
4B		Spare
4C	CMF_ALIVE	Transitions to the (FW) Alive state

Continued on next page

Test List, continued

Table 4-24 Diagnostic Test Listing, Continued

Sequence Number	Label	Description
4D		Spare
4E		Spare
4F	CMF_LLCINIT	Initialize the LLC UCN layer
50	CMS_BLDEXC	Build Exception Vector table
51		Spare
52		Spare
53	CMS_CEINIT	SW Console Emulator initialization
54		Spare
55		Spare
56	CMS_FLASHRW	Build Exception Vector table
57		Spare
58		Spare
59	CMS_ALIVE	Transitions to the (SW) Alive state
5A		Spare
5B	CMS_LLCINIT	Initialize the LLC UCN layer
5C		Spare
5D		Spare
5E	CMS_MON_CTL	Monitor Control Local state change
5F		Spare
60		Spare
61	CTS_CPUTST	CPU Register test
62		Spare
63		Spare
64	CTS_QKDRAM	Quick DRAM accessibility test
65		Spare
66		Spare

Continued on next page

Test List, continued

Table 4-24 Diagnostic Test Listing, Continued

Sequence Number	Label	Description
67	CTS_GRMSYS	Initialize system portion of Global DRAM
68		Spare
69		Spare
6A	CTS_ASICREG	ASIC Register accessibility test
6B		Spare
6C		Spare
6D	CTS_GRMPCHK	Global DRAM EDAC circuitry test
6E		Spare
6F		Spare
70	CTS_LRMDRT	Local SRAM destructive pattern test
71		Spare
72		Spare
73	CTS_LRM_BWL	Local SRAM B/W/L decode test
74		Spare
75		Spare
76	CTS_LRMCLRR	Local SRAM initialization
77		Spare
78		Spare
79	CTS_LRMPCHK	Local SRAM parity circuitry test
7A		Spare
7B		Spare
7C	CTS_BLDVECT	Build Exception Vector table
7D		Spare
7E		Spare
7F		Spare
80		Spare

Continued on next page

Test List, continued

Table 4-24 Diagnostic Test Listing, Continued

Sequence Number	Label	Description
81		Spare
82	CTS_BLDDMRF	Build Memory Reference table
83		Spare
84		Spare
85	CTS_TIMER	Timer comparison test
86		Spare
87		Spare
88	CTS_TRKRAM	Tracking Mechanism test
89		Spare
8A		Spare
8B	CTS_CEINIT	Console Emulator initialization
8C		Spare
8D	CTS_FV_EXC	Force and verify Exception test
8E		Spare
8F	CTS_PRCTYPE	Verify correct processor type
90		Spare
91		Spare
92	CTS_COLD	HPM COLD startup
93		Spare
94		Spare
95	CTS_WARM	HPM RAM Retention startup
96		Spare
97		Spare
98	CTS_ALIVE	Transitions to the (SW) Alive state
99		Spare
9A		Spare
9B	CTS_LR_BKUP	Backup the Local RAM to Global RAM

Continued on next page

Test List, continued

Table 4-24 Diagnostic Test Listing, Continued

Sequence Number	Label	Description
9C		Spare
9D		Spare
9E	CTS_MTOS	Transitioning to MTOS
9F to A1		Spare
A2	CMS_PRGFLASH	Program the Flash ROM
A3		Spare
A4		Spare
A5	CMS_I OLD RT	I/O Link SRAM destructive pattern test
A6		Spare
A7	CMS_IOL_BWL	I/O Link SRAM B/W/L decode test
A8		Spare
A9	CMS_IOLCLRR	I/O Link SRAM initialization
AA		Spare
AB	CMS_IOLPCHK	I/O Link SRAM parity circuitry test
AC		Spare
AD	CMS_GB_PCHK	Global Bus parity circuitry test
AE		Spare
AF	CMS_EEPRMI	I/O Link Serial EEPROM access test
B0		Spare
B1		Spare
B2	CMS_IOL1 RST	Release I/O Link #1 from reset
B3		Spare
B4	CMS_IOL1 IDL	Transition I/O Link #1 to IDLE
B5		Spare
B6		Spare
B7	CMS_IOL1 RUN	Transition I/O Link #1 to RUN

Continued on next page

Test List, continued

Table 4-24 Diagnostic Test Listing, Continued

Sequence Number	Label	Description
B8		Spare
B9	CMS_IOL2RST	Release I/O Link #2 from reset
BA		Spare
BB	CMS_IOL2IDL	Transition I/O Link #2 to IDLE
BC		Spare
BD	CMS_IOL2RUN	Transition I/O Link #2 to RUN
BE to FA		Spare
FB	CMS_LR_BKUP	Backup the Local RAM to Global RAM
FC		Spare
FD		Spare
FE	CMS_MTOS	Transitioning to MTOS
FF		Spare

4.10 I/O Card Indicators

CAUTION

CAUTION—Loss of power detected by an Analog Output IOP card causes all of the channels of an Analog Output IOP to drop to a nonpowered state and all channels of a Digital Output IOP to set its outputs to off. Refer to Section 6 regarding use of a Standby Manual device to maintain process point output values.

A Journal output status of **NORESP** may indicate this detected loss of power. Check the outputs and the mode of the related control points should this occur.

Introduction

When power is first applied to any IOP or I/O Link Extender card, check the **Power** and **Status** indicators. The **Power** indicator is illuminated whenever dc power is applied. After a few seconds, the **Status** indicator should be illuminated in a steady state.

Indicator functionality

Table 4-25 describes the function of the **Power** and **Status** indicators on IOP and I/O Link Extender cards. The functionality of the **Status** indicator on IOPs with model numbers that have a "Y" in the model number, such as MU-PAOY22, have additional functionality which is described in Table 4-24. The function of the Power indicator is the same for all IOPs.

Table 4-25 IOP Card Indicators

Card Type	Indicator	Functionality
IOP	Power	Power is applied to the card. If the indicator is extinguished, check the Power System, the power cable to the card file, and the fuse on the backplane.
	Status	If the LED blinks once a second, a Soft failure has occurred. If the LED remains off, a Hard failure has occurred.
I/O Link Extender	Power	Power is applied to the card. If the indicator is extinguished, check the Power System, the power cable to the card file, and the fuse on the backplane.
	Status	Flickers when data is being transmitted. If the LED blinks at a one second rate, an Optic Coupler module is disconnected.

Continued on next page

Multifunctional Status indicator

The **Status** indicator on an IOP with model number that has a "Y" in the model number, such as MU-PAOY22, has functionality beyond the description in Table 4-25. One of two colors are normally displayed. A third color, red, is abnormal and would be an LED failure. Table 4-26 defines the colors.

Table 4-26 IOP Multicolor Status Indicator

Color	Status
Green	The IOP is assigned primary status.
Orange	The IOP is assigned backup status. Occurs in redundant IOP configurations.

4.11 FTA Indicators

Introduction

FTA indicators provide functional status information. The number of indicators and their purpose varies with the type of FTA.

FTA indicators

Table 4-27 describes the function of the various indicators on the FTAs and associated assemblies.

Table 4-27 FTA Indicators

Card Type	Indicator	Functionality
Power Adapter	Cable Fault	The red LED indicates a grounded or shorted cable when lit. There is one indicator for each cable.
LLMux	Power	Indicates that power is present on the FTA.
Analog Input	Power Calibration	Indicates that power is present. Extinguishes for approximately 15 seconds during a calibration cycle.
Redundant Analog Output	Switch Position	Lit when IOP A is active and not lit when IOP B is active or either IOP is not active. Cable A and IOP A can be replaced when the LED is not lit, and Cable B and IOP B can be replaced when the LED is lit.
Redundant HLAI	IOP Availability	When lit, the A IOP is the primary or available to be the primary. When not lit, the A IOP is not available to be the primary.
Serial Device Interface	Power	Indicates that power is present on the FTA.
	Status	One of the following indicator conditions exists. Not lit: The FTA self-test failed. Slow blink: (Symmetrical 1 sec. blink) A communication error between the FTA and the IOP/HPMM was detected. Fast blink: (Symmetrical .5 sec. blink) A communication error between the device and the FTA was detected. Constantly lit: The FTA self-test was successful and the FTA is fully operational.

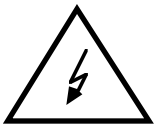
Continued on next page

FTA indicators, continued

Table 4-27 FTA Indicators, Continued

Card Type	Indicator	Functionality
Serial Interface	Power	Indicates that power is present on the FTA.
	Status	One of the following indicator status conditions exists. The conditions are listed in the order of importance. Not lit: This condition exists only when the FTA is in a Hard failure state. Slow blink: (Symmetrical 1 sec. blink) This condition indicates that the FTA has not received a Time Out Gate (TOG) refresh from the SI IOP within 10 seconds. Fast blink: (Symmetrical .5 sec. blink) This condition indicates that one or more Array Points configured for this FTA have a communications error. Odd blink: (Asymmetrical 1/.25 sec. blink) This condition indicates that one or more Array Points configured for this FTA have an error in the Array Point configuration error category. The IOP/HPMM is not configured or configured improperly. Constantly lit: This condition indicates that no errors exist in the FTA. Due to the long ACK/Message timeout time and the required three tries, the FTA may indicate a TOG timeout if the CIM is responding with an ACK to the FTA requests, or if the destination PLC device is not responding to the requests. Additional troubleshooting information can be found in the *Serial Interface Options* manual.

4.12 Power System Indicators



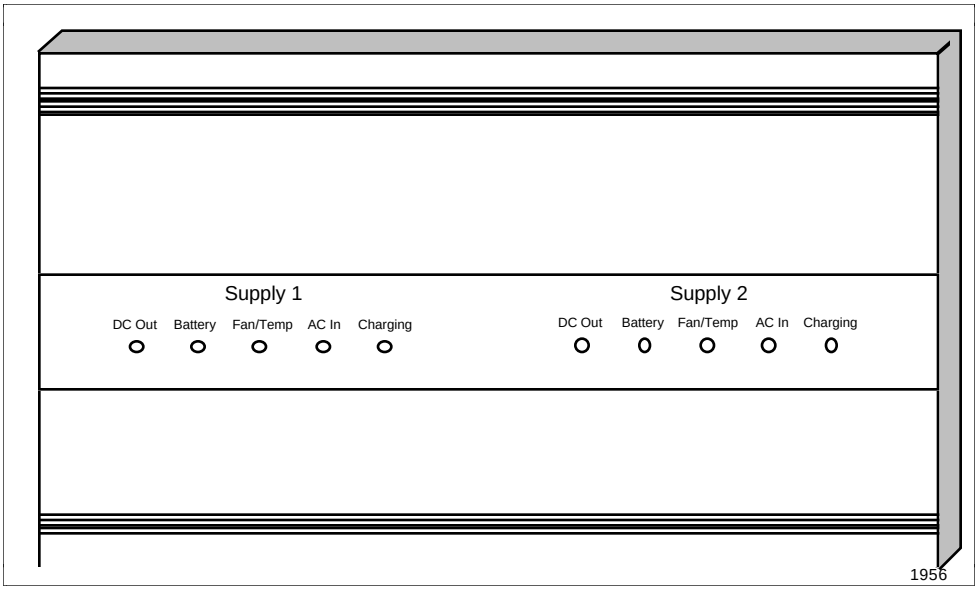
CAUTION, RISK OF ELECTRIC SHOCK

4.12.1 Standard Power System

Introduction

Examine the **DC Out, Battery, Fan/Temp, AC In**, and **Charging** indicators for each Standard Power Supply Module. The Standard Power System cover, illustrated by Figure 4-7, identifies these LED indicators. If the Power System is fully functional, all five of the indicators are illuminated.

Figure 4-7 Standard Power System Indicators



DC Out indicator

If a **DC Out** LED is off, ac line power has been lost (check the **AC In** LED) or the Power Supply Module has failed. If the Power System is nonredundant, or if both **DC Out** LEDs are off, the HPM has lost 24 Vdc. The CMOS backup system maintains power to the CMOS memory, so subsystem programs are not lost. See the **Battery** LED description below. A set of annunciator contacts, which are illustrated in Figure 4-8, open when these conditions occur.

Continued on next page

Battery indicator

If the **Battery** LED is off and the **Charge** LED is on, the **48 Volt Battery** switch is in the off position or the 48 V Battery Backup system has failed. A set of annunciator contacts, which are illustrated in Figure 4-8, open when these conditions occur. If the Power System does not have the battery pack option, the **Battery** LED will normally be on, and the **Charge** LED will normally be on.

Fan/Temp indicator

If the **Fan/Temp** LED is off, the fan in the Power Supply Module has failed or the temperature of the HPM has exceeded a safe value. An annunciator contact, discussed below, is activated by any of the five conditions described below.

AC In indicator

If the **AC In** LED is off, ac power to the HPM has been lost or the switch on the Power Supply Module is off. Backup systems, if operating, are maintaining the unit. Check the **DC Out** and **Battery** indicators to determine the state of the system. Some installations may have the Power Supply Modules connected to the separate ac power sources to minimize outage caused by a power loss. Annunciator contacts, illustrated in Figure 4-3, signifying power loss from either supply, are activated independently.

Charging indicator

When the **Charging** LED is off, the charging circuit that maintains the optional 48 V Battery Backup system has failed. Check the batteries, their corresponding connections, and the charging circuits in the Power Supply Module (s). An annunciator contact output, illustrated in Figure 4-8, is activated by this condition.

Alarms

The primary Power Supply Module alarm and secondary Power Supply Module alarm contacts monitor five functions within each Power Supply Module. They will open if:

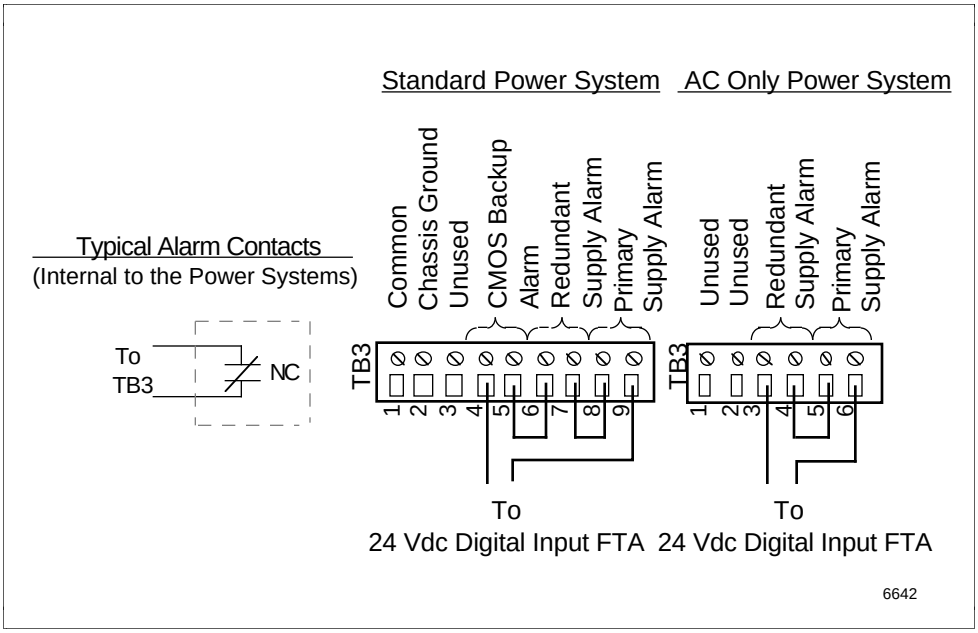
- The dc output voltage is not within normal limits.
- AC input power to the supply has failed.
- The Power Supply Module electronics have overheated or the Power Supply Module fan has failed.
- The 48 V backup battery system has failed because the batteries have discharged or they have been disconnected.
- The battery charger in the Power Supply Module has failed.

Continued on next page

Annunciator contacts

Three annunciator contacts are shown in Figure 4-8. These contacts are normally wired in series by the user as illustrated.

Figure 4-8 Standard Power System Annunciator Contact Connections



CMOS alarm

The CMOS Backup Alarm contacts open if the CMOS backup batteries have been removed or the batteries have degraded to where the CMOS charging and monitoring circuit has determined they should be replaced.

Component replacement

Power System component replacement is discussed in Section 7.

4.12.2 AC Only Power System

Introduction

There are two LED indicators on the AC Only Power System and no test points. The two green LED indicators are located on the AC/DC Distribution assembly and provide a visual indication of the primary and redundant Power Supply Modules' operational status. When the LED is illuminated, its associated Power Supply Module is functional. The locations of the indicators are illustrated in Figure 2-25.

CMOS batteries

The three alkaline batteries on the AC/DC Distribution Assembly provide backup power for the CMOS Memory in the HPMM. They are not rechargeable and must be replaced periodically. The period should not exceed 6 months, provided there is no sustained loss of power to the CMOS Memory. If there is, replace the batteries after dc power is restored to the HPM.

Alarm annunciator contacts

Connection points for two sets of annunciator contacts that signal the status of the primary and redundant Power Supply Modules are provided by terminals on TB3. See Figure 4-3. Terminals 3 and 4 are connection points for the secondary Power Supply Module and terminals 5 and 6 are the connection points for the primary Power Supply Module. The annunciator contact connection terminals are normally wired in series to a monitoring 24 Vdc Digital Input FTA.

4.13 Power System Voltage Checks

WARNING

WARNING—Redundant power cables normally provide power to a card file or Power Distribution Assembly, so a single power cable can be disconnected for voltage measurements at the Power System connector without affecting the performance of the equipment. However, sometimes an insufficient number of Power System connectors are available and only a single cable provides power to the card file or Power Distribution Assembly.

Before disconnecting a power cable for voltage measurements, be sure power to a card file or Power Distribution Assembly will not be interrupted.

4.13.1 Standard Power System

Voltage test points

Refer to Figures 4-9 through 4-11 for identification the voltage points listed in Table 4-28.

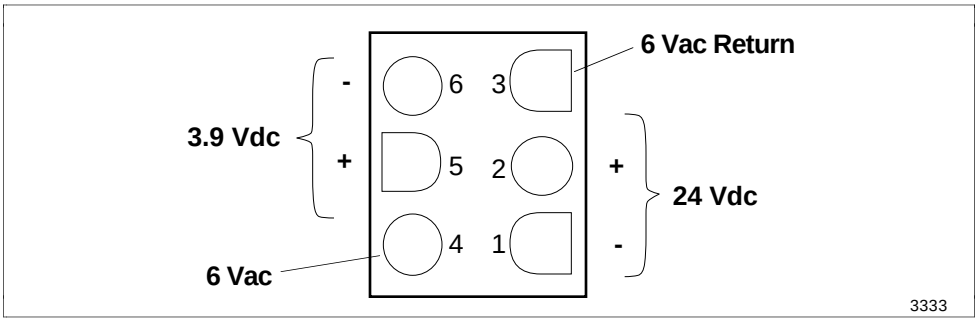
Table 4-28 Standard Power System Voltage Test Points

Voltage Test Point	Acceptable Range	Corrective Action
AC Input		
120 Vac or 240 Vac	100 to 264 Vac	Check ac power source.
Power Supply Module	`	
Common		Common reference
DC Out		
PSM (25.5 Vdc)		Replace Power Supply Module
Battery Power (24.5 Vdc)		Replace Power Supply Module
AC Out (6 Vac for clock)		Replace primary (left) Power Supply Module.
CMOS Battery Backup		
NiCad Battery (Set of 3)	1.2 - 1.6 Vdc (1) 3.6 - 4.8 Vdc (3)	Replace NiCad batteries.

Continued on next page

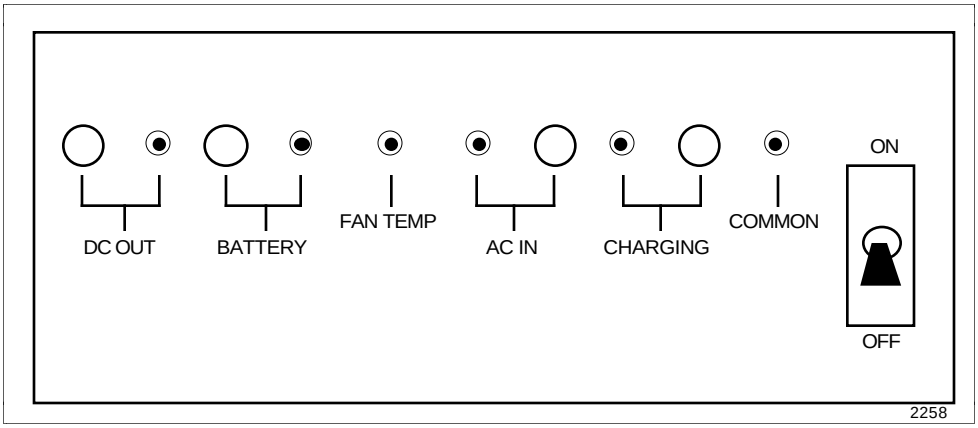
Power output connector

Figure 4-9 Power System Power Output Connector Pin Assignments



PS Module test points and indicators

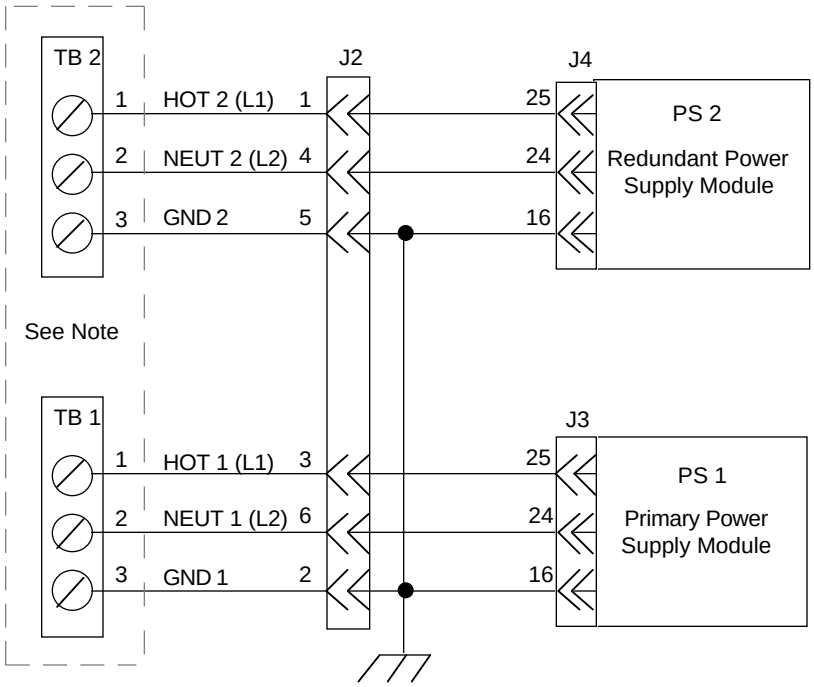
Figure 4-10 Power Supply Module Test Points and Indicators



Continued on next page

Power System ac wiring

Figure 4-11 Power System AC Wiring



Note:

Terminal strips TB1 and TB2 are located on the backplane in the Standard Power System. The terminal strips are located on the AC/DC Distribution Assembly in the AC Only Power System.

6643

4.13.2 AC Only Power System

Voltage test points

Refer to Figure 4-9 to identify the voltage points listed in Table 4-29. The locations of the Power System power output connectors are illustrated in Figure 2-25.

Table 4-29 AC Only Power System Voltage Test Points

Voltage Test Point	Acceptable Range	Corrective Action
AC Input		
120 Vac 220 Vac	100 to 132 Vac 187 to 264 Vac	Check ac power source.
Power Supply Module		
Common DC Out (24 Vdc) Connector Pins 3 and 4 (6 Vac for clock)	None 24 to 26 Vdc 2.0 to 6.0 Vac	Common reference Replace Power Supply Module. Replace primary (left) Power Supply Module.
CMOS Battery Backup		
Alkaline Battery (Set of 3)	1.2 to 1.5 Vdc 3.6 to 4.5 Vdc total	Replace alkaline batteries.

Section 5 – UCN Exerciser

5.1 Overview

Section contents

The topics covered in this section are:

	Topic	See Page
5.1	Overview	333
5.2	Applications	334
5.3	Request Data Response (RDR) Test	335
5.4	Triangulation Test	336
5.5	Test Operation	337
5.6	Analyzing Results	344

Purpose

This section covers the operation of the UCN Exerciser program that is used for isolating communications problems in a UCN node.

CAUTION

CAUTION—The UCN Exerciser is an off-process program intended to provide a level of confidence in the connectivity and communication capabilities of an installed network. This test must not be used for an on-process system because the added communication and CPU loads induced by the test may cause throughput and response time degradation of the control system. The test works best if the physical node states of the participating configured nodes do not change during the duration of the test.

Each node must be configured in the NIM to participate in either test.

More than one logical UCN can normally be configured for a single physical UCN. The UCN Exerciser program must be configured to include, for test, only NIMs (and their redundant partners) from the same logical UCN. Configuring NIMs from more than one logical UCN will cause false errors to be indicated for some of the NIMs. This restriction does not apply to for other UCN node types, such as a High-Performance Process Manager, Advanced Process Manager, Process Manager, or Logic Manager.

5.2 Applications

Purpose

The purpose of the UCN Exerciser is:

- To provide the user with confidence that the UCN is operating properly by sending messages between UCN nodes.
- To test the peer-to-peer communications path. The status of peer-to-peer communications between High-Performance Process Managers is not shown on the Universal Station (US) display.
- To provide a means of isolating communication problems to a certain High-Performance Process Manager by observing the gross level of errors detected.

Two part test

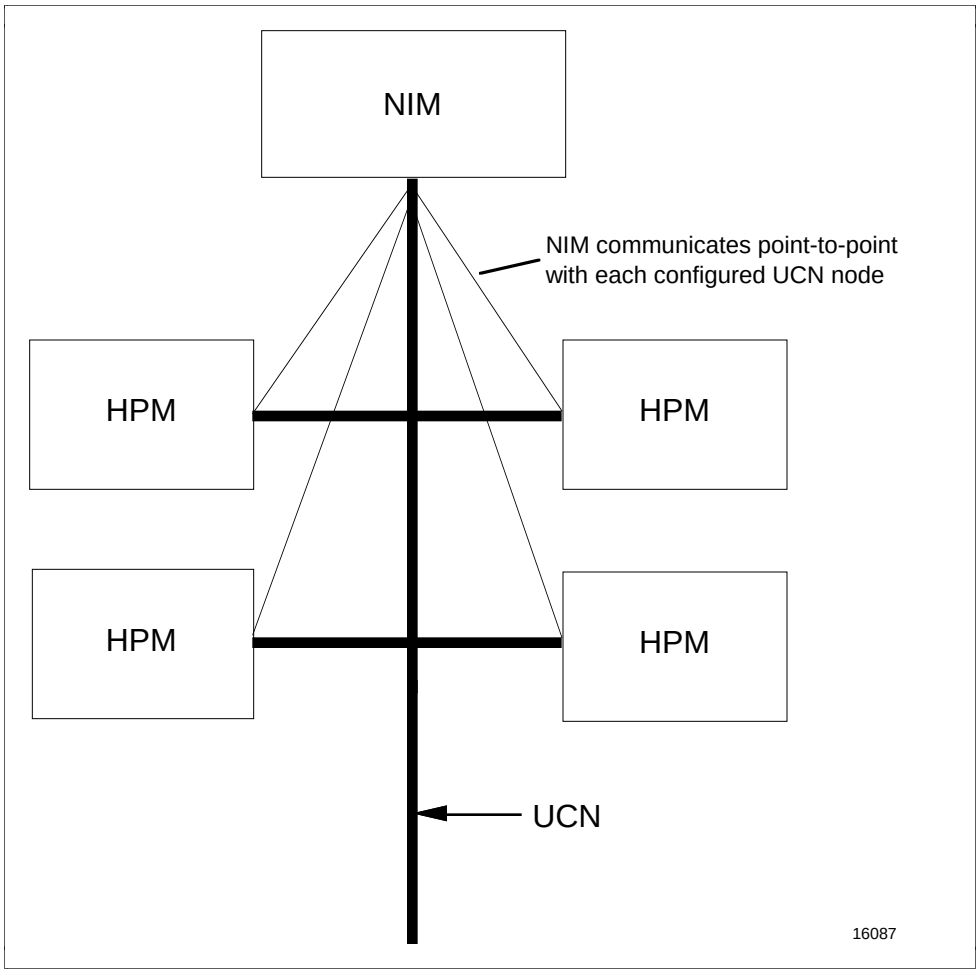
The test has two parts, an RDR test and a Triangulation test, with both performed in succession repeatedly until the test is halted.

5.3 Request Data Response (RDR) Test

Introduction

In the Request Data Response test, as illustrated in Figure 5-1, the Test Master, a Network Interface Module (NIM), attempts to communicate on a point-to-point basis with every UCN node configured to participate in the test. A node can be ALIVE, BUT NOT TOKEN PASSING and still participate in this test using its "shadow address," numbered 65-128. This check is to determine with which participants in the test the Master can communicate.

Figure 5-1 RDR Test Configuration



RDR protocol

The communications protocol used for this part of the test is RDR protocol. All nodes that are powered on and/or are capable of receiving and transmitting messages, should respond to the RDR from the test Master. A node that does not respond is assumed to be not on the network and is not requested to participate in the triangulation part of the test. A node that does respond but whose status indicates that it is not capable of token passing will also not be requested to participate in the triangulation part of the test.

5.4 Triangulation Test

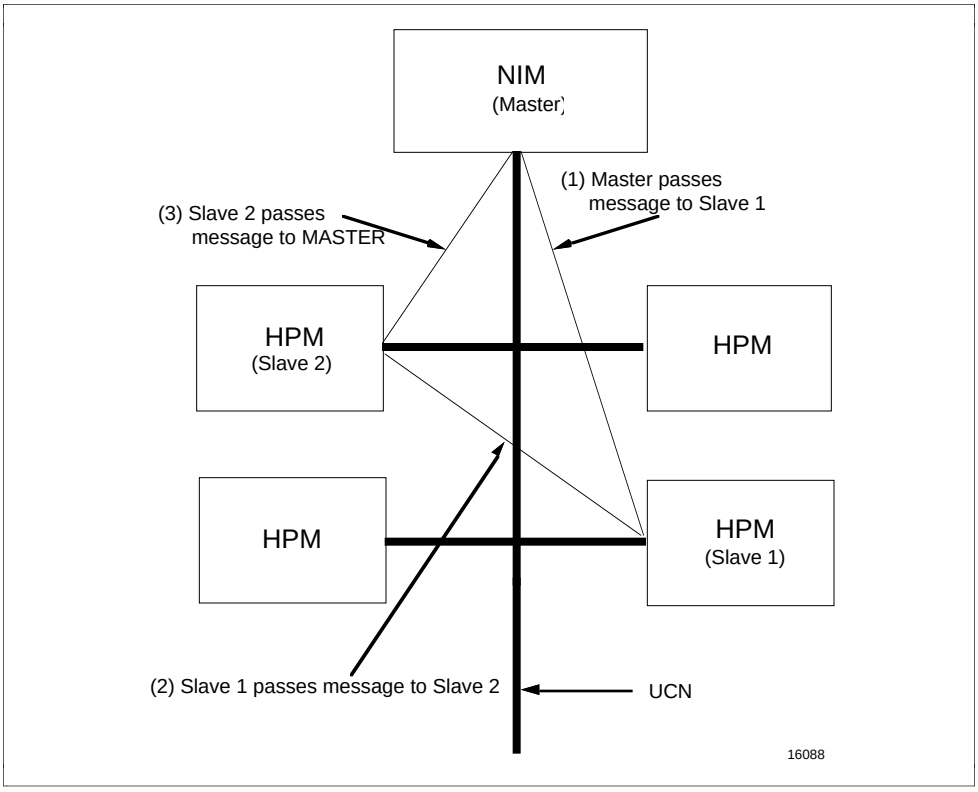
ATTENTION

ATTENTION—This test requires a minimum of one NIM and one server (other UCN nodes). With only two nodes, the NIM talks point-to-point. Three nodes are required for true triangulation.

Introduction

In the triangulation test, as illustrated in Figure 5-2, only nodes that are configured in the test are capable of token passing participate. For example, HPMs that have not been loaded, cannot pass tokens and therefore do not participate. For those nodes that do participate, the test Master issues a message to another node in the test and requests the message to be forwarded to a third node. The third node in the test then sends a message back to the test Master, which verifies that the path has successfully completed. While passing the message, the following communication paths are checked: Master (NIM) to Slave 1, Slave 1 to Slave 2, and Slave 2 to back to the Master.

Figure 5-2 Triangulation Test



Timeout policy

Because a message may be lost or an error may occur, the Master has a reasonable timeout policy for receiving the response back from Slave 2. The timeout policy assumes that each Slave in the test is serving only one Master. This means that responses arriving late are considered errors. By examining several paths together, it is usually possible to determine which nodes are experiencing communication problems.

5.5 Test Operation

UCN Exerciser operation

The operator at the Universal Station (US) can control the operation of the UCN Exerciser. Use the following procedure to perform the UCN Exerciser tests. The display used in the test is explained below. Use the procedure in Table 5-1 to run the UCN Exerciser.

ATTENTION

ATTENTION—If the display does not appear after starting the UCN Exerciser, the Pathname Catalog must be reconstituted by adding the search path **NET>DIA1**.

Starting the UCN Exerciser

The UCN Exerciser is started by pressing the <**SCHEM**> key, typing in **HPNXOVR**, and pressing the <**ENTER**> key.

Page 1 of the UCN Exerciser Overview display will appear as shown in Figure 5-3. The display shows the status of the UCN Exerciser for the LCN nodes 1 through 64 that are NIMs on the LCN. If no status is indicated for the node address, the node is not a NIM.

PAGE target

Selecting the **PAGE** target will invoke Page 2 of the UCN Exerciser Overview display as shown in Figure 5-4. LCN nodes 65 through 96 are represented.

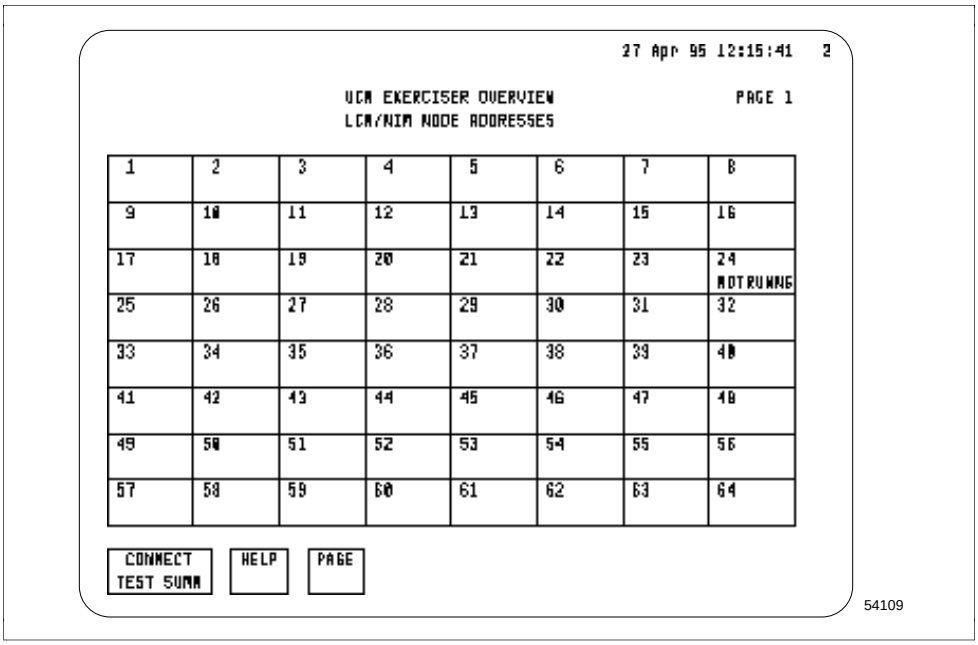
HELP target

Selecting the **HELP** target will invoke the UCN Exerciser Help display as shown in Figure 5-5. Selecting the **UCN EX OVERVIEW** target provides a return to the UCN Exerciser Overview display.

Continued on next page

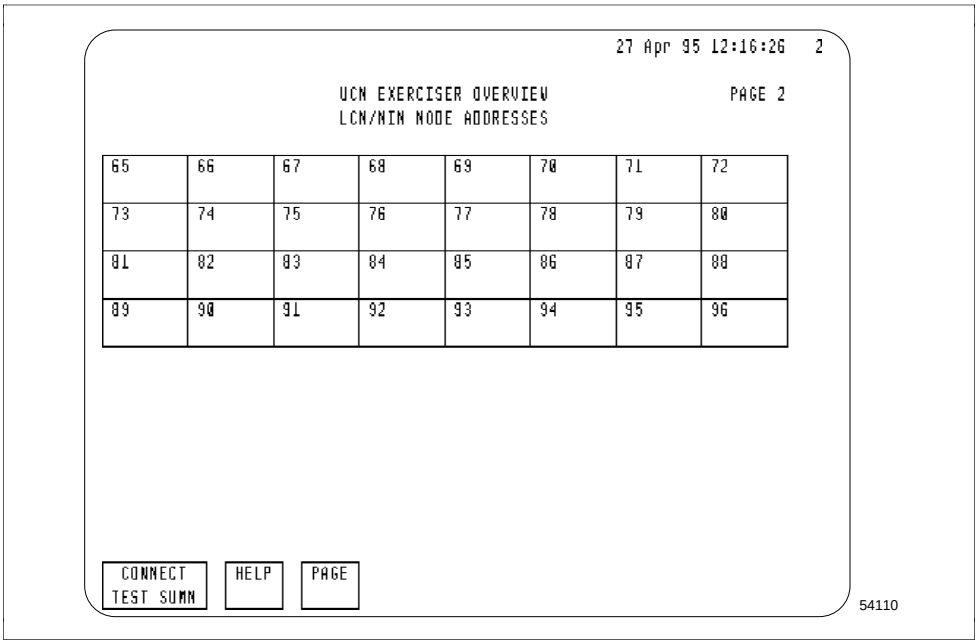
UCN Exerciser Overview display Page 1

Figure 5-3 UCN Exerciser Overview Display – Page 1



UCN Exerciser Overview display Page 2

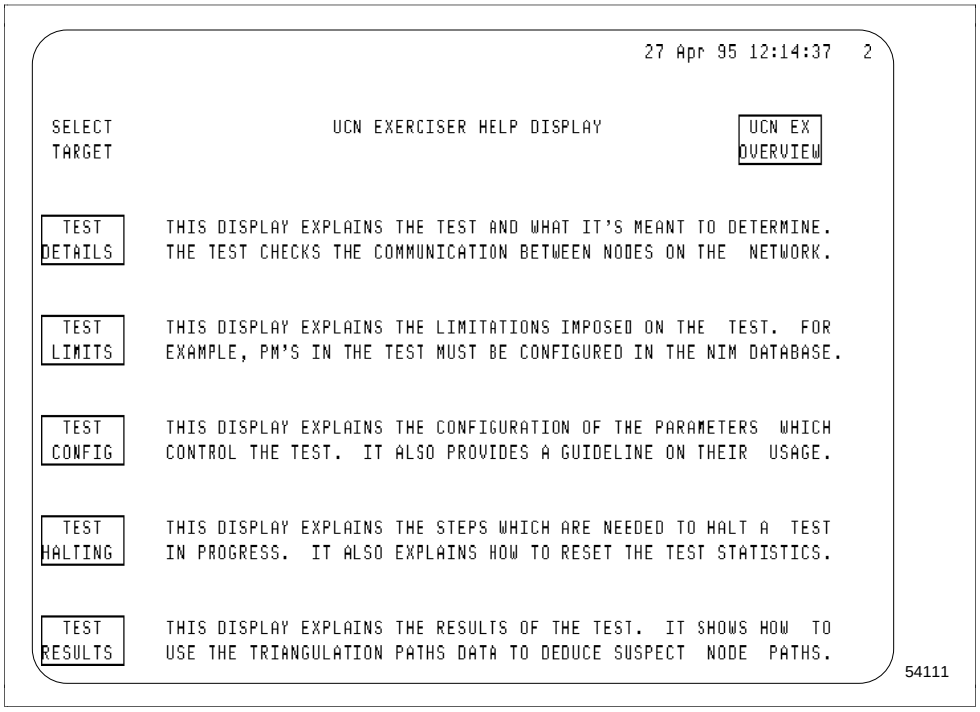
Figure 5-4 UCN Exerciser Overview Display – Page 2



Continued on next page

UCN Exerciser Help display

Figure 5-5 UCN Exerciser Help Display



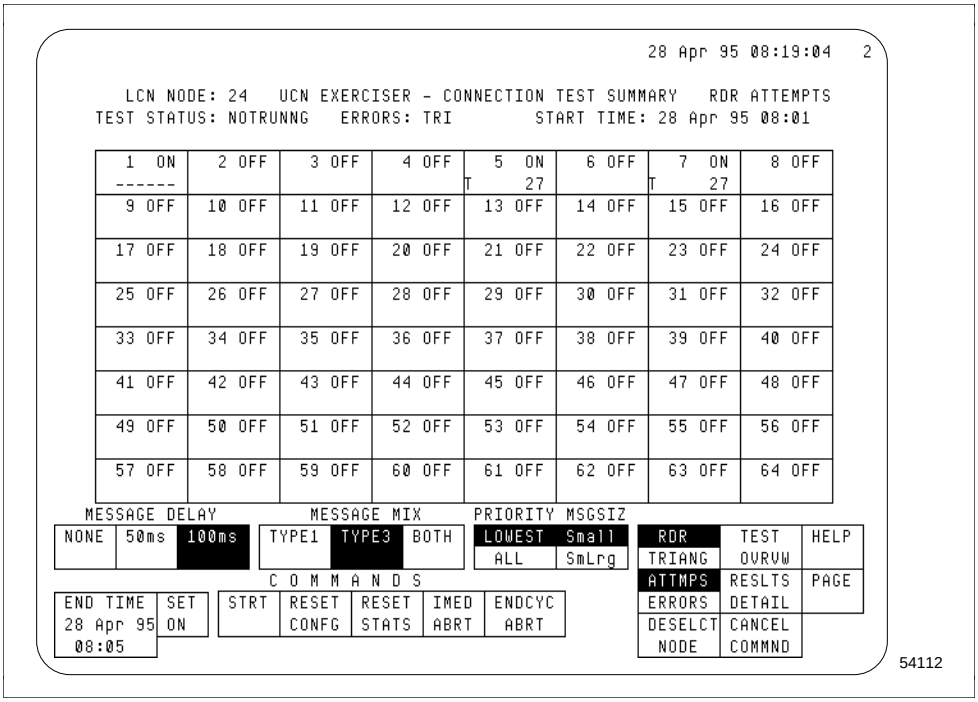
Continued on next page

Connection Test Summary display – Page 1

Each box in the grid on the UCN Exerciser Overview is a target, that when chosen and followed by selection of the **CONNECT TEST SUMM** target, invokes Page 1 of the Connection Test Summary display for the NIM node.

The display is shown in Figure 5-6. Nodes 1 through 64 are represented.

Figure 5-6 Connection Test Summary Display – Page 1



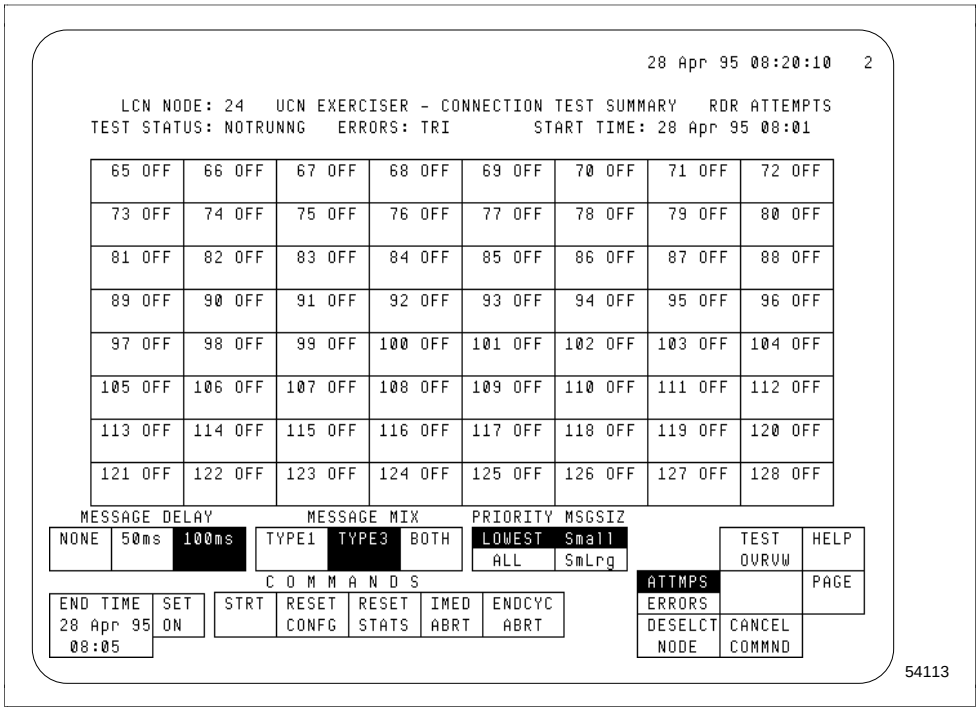
Continued on next page

Connection Test Summary display – Page 2

Selecting the **PAGE** target invokes Page 2 of Connection Test Summary display. Nodes 65 through 128 are represented. The display is shown in Figure 5-7.

Selecting the **PAGE** target provides a return to Page 1 of the Connection Test Summary display.

Figure 5-7 Connect Test Summary Display – Page 2



Continued on next page

UCN Exerciser test procedure

Table 5-1 is a UCN Exerciser test procedure. Follow the procedure to test the UCN.

Table 5-1 UCN Exerciser Test Procedure

Step	Action
1	Start the UCN Exerciser by pressing the <**SCHEM**> key, type in **HPNXOVR**, and press the <**ENTER**> key.
2	Each box in the grid on the UCN Exerciser Overview display is a target, that when chosen and followed by selection of the **CONNECT TEST SUMM** target, invokes Page 1 of the Connection Test Summary display for the NIM node. Nodes 1 through 64 are represented. Selecting the **PAGE** target invokes Page 2 of Connection Test Summary display. Nodes 65 through 128 are represented. Make a selection.
3	Select each node on the UCN that is to participate in the test. This is accomplished by choosing the node in the grid and then the **SET ON** target. Repeat this procedure until all desired nodes are on. For example, Figures 5-6 and 5-7 show nodes 1, 5, and 7 configured for the test. If a node is selected by mistake, select it again and the **SET ON** target will toggle to **SET OFF**. Selecting **SET OFF** deselects that node.
4	Configure the MESSAGE DELAY parameter by selecting the **NONE**, **50 ms**, or **100 ms** target. For example, Figures 5-6 and 5-7 show 100 ms selected.
5	Configure the MESSAGE MIX parameter by selecting one of the three targets • **TYPE 1** Send only Type 1 messages. These are unacknowledged unconnected messages. • **TYPE 3** Send only Type 3 messages. These are acknowledged messages. • **BOTH** Send both Type 1 and Type 3 messages. Figures 5-6 and 5-7 show **TYPE 3** selected.
6	Configure the **PRIORITY** parameter by selecting one of two targets. • **LOWEST** Send messages at the lowest priority. • **ALL** Send messages at each of four priorities.

Continued on next page

UCN Exerciser test procedure, continued

Table 5-1 UCN Exerciser Test Procedure, Continued

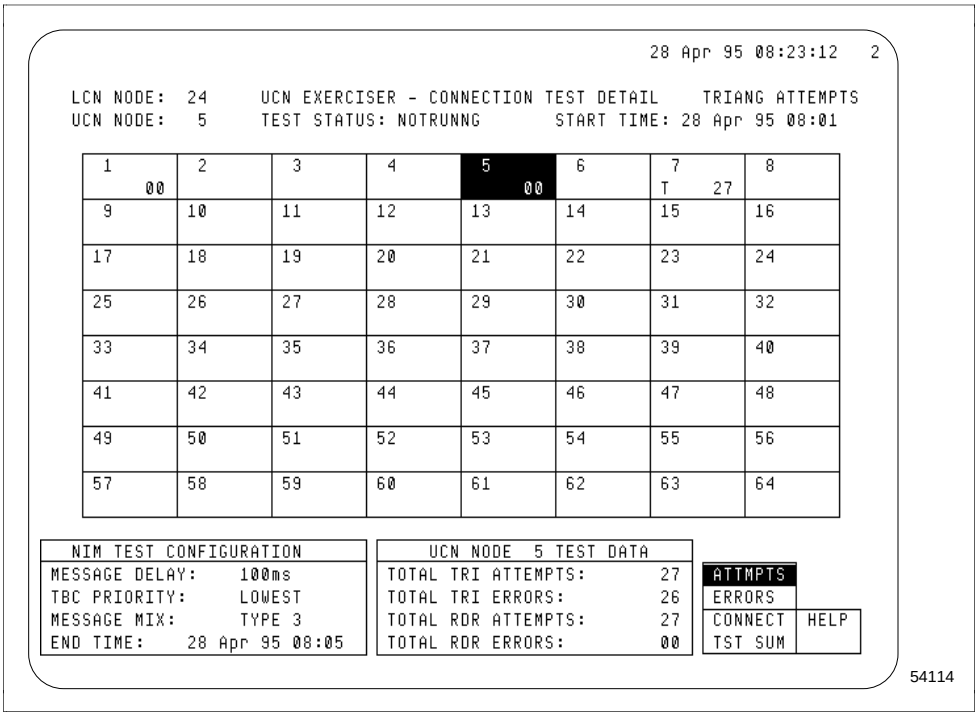
Step	Action
7	Configure the **MSGSIZ** (MESSAGE SIZE) parameter by selecting one of two targets. • **SMALL** Send 50 word messages. • **SMLRG** Send 50 and 100 word messages.
8	Configure the end time date parameter by selecting the **END TIME** target and entering the date in the format shown. Press <**ENTER**>. Enter the time parameter in the format shown and press <**ENTER**>.
9	Select the **STRT** (START) target followed by the **EXEC** (EXECUTE) target to start the test. The **EXEC** target appears to the right of the **ENDCYC** (END CYCLE) target when the **STRT** target has been selected. There are five commands shown in Figures 5-6 and 5-7. To execute the chosen command, the **EXEC** target must also be selected. The following commands are available. • **STRT** Starts the RDR and Triangulation test. • **RESET CONFG** Resets the configuration to off for all nodes. • **RESET STATS** Resets the statistics to zero. • **IMED ABRT** Aborts the test wherever it is in the procedure. • **ENDCYC ABRT** Aborts the test at the end of the current test cycle.
10	Select the **TEST OVRVW** (TEST OVERVIEW) target to return to the UCN Exerciser Overview display. See Figures 5-6 and 5-7. Wait for the test to complete. The **NOTRUNNG** (NOT RUNNING) status appears on the UCN Exerciser Overview display as shown in Figure 5-3.

5.6 Analyzing Results

Connect Test Detail display

To see the results, chose the node of interest and select the **RESLTS DETAIL** (RESULTS DETAIL) target on the Connect Test Summary display. This invokes the Connection Test Detail display as shown in Figure 5-8.

Figure 5-8 Connection Test Detail Display



Number of attempt errors

Check the boxes in the grid target for nodes 0, 5, and 7. The number in the lower right corner of the box reports the number of attempts if the **ATTMPS** (ATTEMPTS) target is backlighted, or the number of errors if the **ERRORS** target is backlighted on the Connect Test Summary display. The display is selected with the **CONNECT TST SUM** (Connect Test Summary) target.

Problem correction

The node that has the highest number of errors is likely to be the node causing a problem. The problem should be corrected by replacing the HPM UCN Interface module or by checking the UCN cable connections. If this does not correct the problem, call the Technical Assistance Center (TAC) for assistance.

Section 6 – Removal and Replacement

6.1 Overview

Section contents

The topics covered in this section are:

	Topic	See Page
6.1	Overview	345
6.2	Electrostatic Discharge Protection	346
6.2.1	ESD Guidelines for HPMM and IOP Cards	347
6.3	HPMM and IOP Cards	348
6.3.1	Removal and Replacement	348
6.3.2	Standby Manual Device Overview	350
6.3.3	AO Standby Manual Device Operation	353
6.3.4	DO Standby Manual Device Operation	359
6.3.5	HPMM or IOP Card Case Replacement	364
6.4	Field Termination Assembly	366
6.4.1	IOP to FTA Cable	366
6.4.2	FTA Replacement	367
6.4.3	FTA Module and Relay Replacement	368
6.5	Card File Replacement	369
6.6	Power System	370
6.6.1	CMOS Battery Replacement	370
6.6.2	48 V Backup Battery Replacement	371
6.6.3	Power Supply Module Replacement	376
6.6.4	CMOS Backup Assembly Replacement	377
6.7	Cabinet	377
6.8	I/O Link Extender Optical Coupler Module Replacement	378

Introduction

This section describes how to remove and replace assemblies in the High-Performance Process Manager.

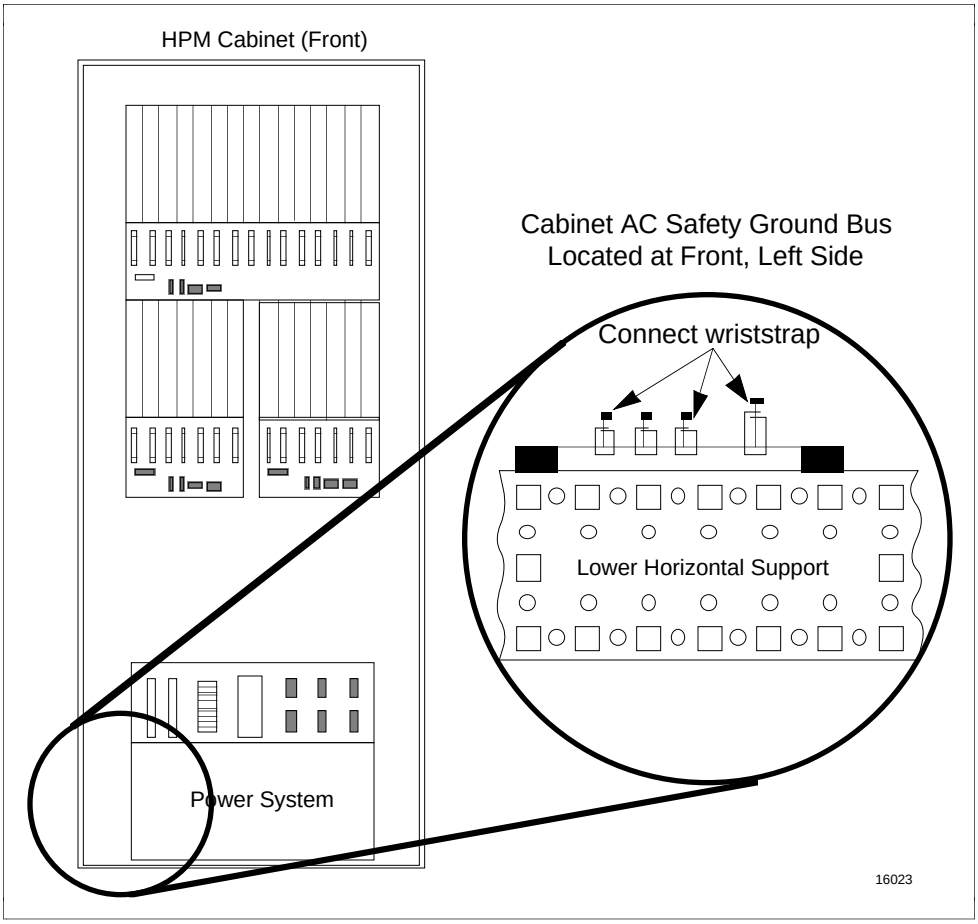
6.2 Electrostatic Discharge Protection

CAUTION

CAUTION—It is extremely important that you wear a properly connected Electrostatic Discharge (ESD) wriststrap while removing, handling, and installing these High-Performance Process Manager components. Slip the strap on your wrist like a wristwatch and connect its clip to the ground bus located inside the left front side of the cabinet. See Figure 6-1 for connection points. There is no danger of personnel receiving shocks from wearing an approved wrist strap. Be sure to place the component in a static-safe carrying pouch, if appropriate, immediately after its removal.

Honeywell can supply a wriststrap manufactured by 3M Company that has a maximum resistance of 10 megaohms and a minimum resistance of 500 kohms.

Figure 6-1 Cabinet ESD Wriststrap Connection



6.2.1 ESD Guidelines for HPMM and IOP Cards

Static discharge effects

When inserting an HPMM or IOP card into a card file and following normal ESD procedures, other cards in the card file, HPMM or IOP, can go **OFFNET** because of electrostatic discharge. It does not result in damage to any of the components on the card when an ESD wriststrap is worn, but does affect subsystem integrity. A procedure has been developed to discharge the card using a 10 megaohms Static Discharge Probe.

ESD kit

Honeywell has available an ESD kit, part number 30185H, that contains the following components.

- 10 megaohm static discharge probe
- Static discharge wriststrap (AESOPS Inc. Model 31531)
- Static discharge cord, 15 feet (AESOPS Inc. Model 30204)
- Static discharge cord, 6 feet (AESOPS Inc. Model 30205)
- Antistatic work surface with bag

Building a static discharge probe

A static discharge probe can be built by placing a 10 megaohm resistor in series with any available probe or clip lead.

ESD prevention rules

When installing a firmware upgrade, or replacing or adding a card, adhere to the following rules to prevent ESD from affecting the HPMM or IOP cards.

- Ground the antistatic work surface to the card file chassis.
- Ground the wriststrap that is to be worn when removing or inserting card to the card file chassis.
- Ground the wriststrap that is to be worn when upgrading card firmware to the antistatic work surface.
- When removing or inserting a card, handle only the card frame. Do not touch the circuit board or the components
- The 10 megaohm static discharge probe must be grounded to the card file chassis.
- When inserting a card, insert the card 3/4 of the way into the slot and then discharge the card with the 10 megaohm static discharge probe by touching the lower lead of the upper LED, or if there is a daughter board by touching the minus/lower lead of the bypass capacitor labeled C1 or C2.

6.3 HPMM and IOP Cards

6.3.1 Removal and Replacement

CAUTION

CAUTION—Cycling power or removing nonredundant Analog or Digital Output IOPs results in their outputs going to the nonpowered state regardless of the **FAILOPT** selection configured. Follow the Analog or Digital Standby Manual device instructions in this section.

HPMM and IOP card removal and replacement

Use the following procedure when removing and replacing an HPMM or IOP card.

Step	Action
1	When removing an HPMM or IOP card, first connect your ESD wriststrap to the cabinet's ground bar.
2	Before removing an analog or digital output IOP from a card file, system operational requirements may require that a Standby Manual device be connected to the FTA to control operations while the IOP is removed.
3	Any HPMM or IOP card can be removed by simultaneously pulling on the upper and lower extractor levers. When the upper extractor is first moved, power is disconnected from the card. Further operation of both extractors moves the card away from its backplane connector.
4	After the card is free from the connector, carefully slide it out on the card rails and into your hands. Immediately place the card in a static-safe pouch for transport.
5	When installing an HPMM or IOP card, first connect your ESD wrist strap, then remove the card from its pouch.
6	Carefully slide the card onto the card rails, checking to be sure that the card is inserted in both rails.
7	Slide the card into the card file until it has made contact with the backplane connectors. Then firmly press on the front of the card with the heel of your hand. Do not use excessive force! If the card doesn't slip easily into its connectors, remove the card and locate the source of the obstruction. Check for bent contacts at the backplane connectors.

Continued on next page

6.3.1 Removal and Replacement, Continued

HPM UCN Interface module removal and replacement

The HPM UCN Interface module uses a power interlock technique that allows it to be removed from, or installed, in the card file without affecting operation of the High-Performance Comm/Control or High-Performance I/O Link cards. The module is not provided with ground, by way a metal strip on both the module and a mounting rail, until the module is seated in its connector.

The HPM UCN Interface module is mounted in the connector directly below the High-Performance Comm/Control card in slot 1 of the Left 7-Slot or 15-Slot card file, or in slot 9 of the Right 7-Slot card file. The module's case has two extrusions that are inserted into a rail below the card cage to guide the module into position. A captive spring-loaded screw with a knurled head secures the module in place.

Tightening the knurled screw

The UCN Interface Module knurl knob (grounding) fastener must be sufficiently tightened while no UCN drop cables are connected to the front panel connectors. The cables interfere with the tightening procedure. The knurled screw must first be finger-tightened by using your thumb and forefinger and then tightened further using a screwdriver. Use the Phillips-head screwdriver slot in the end of the knurled screw. If a torque screwdriver is available, a setting of 15 inch-pounds is sufficient. If a torque screwdriver is not available, tighten the screw one more turn past finger-tight. Do not over tighten and possibly strip the Phillips-head screw insert.

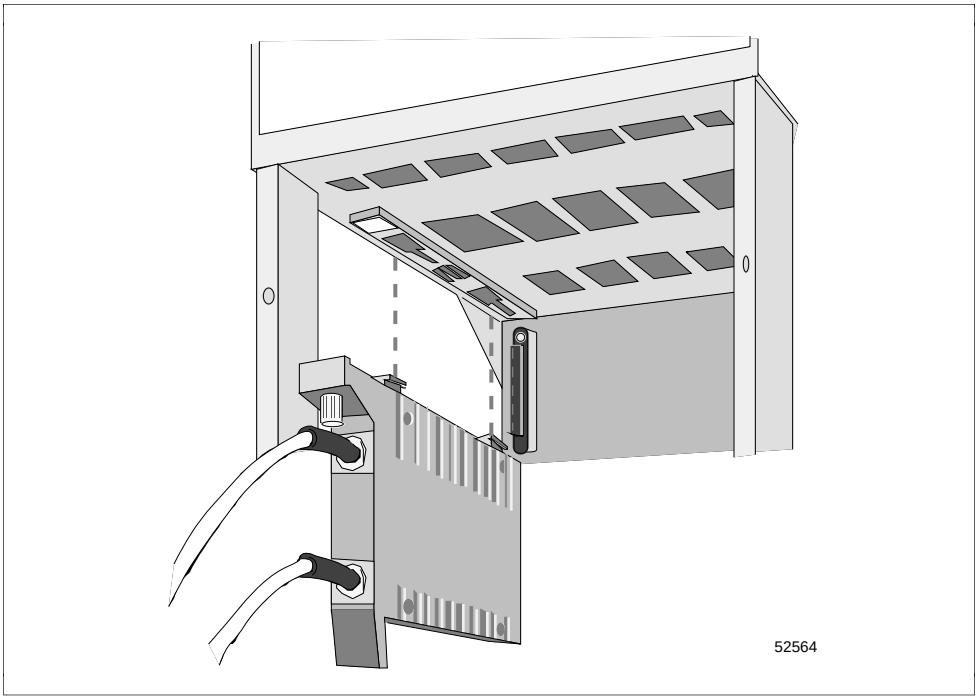
Continued on next page

6.3.1 Removal and Replacement, Continued

HPM UCN Interface module installation

Figure 6-2 illustrates the installation of the HPM UCN Interface module in a card file.

Figure 6-2 HPM UCN Interface Module Installation



6.3.2 Standby Manual Device Overview

Introduction

A Standby Manual device provides the capability to maintain output signals from an Analog Output or 24 Vdc Digital Output FTA while its nonredundant IOP is replaced. An Analog Output IOP to FTA cable can be replaced if an external power source is connected directly to the Standby Manual device since the cable is the FTA's normal 24 Vdc source. The IOP switching module on the Analog Output FTA can also be replaced.

No external power source option

The Digital Output Standby Manual device does not have an external power source option.

Standby Manual device connections

The connection of the Analog Output Standby Manual device and the Digital Output Standby Manual device to the FTA differs. The Analog Output Standby Manual device connects by cable to a unique connector on the FTA that is labeled **STANDBY MANUAL**. The Digital Output Standby Manual device connects to one of the two IOP interface connectors.

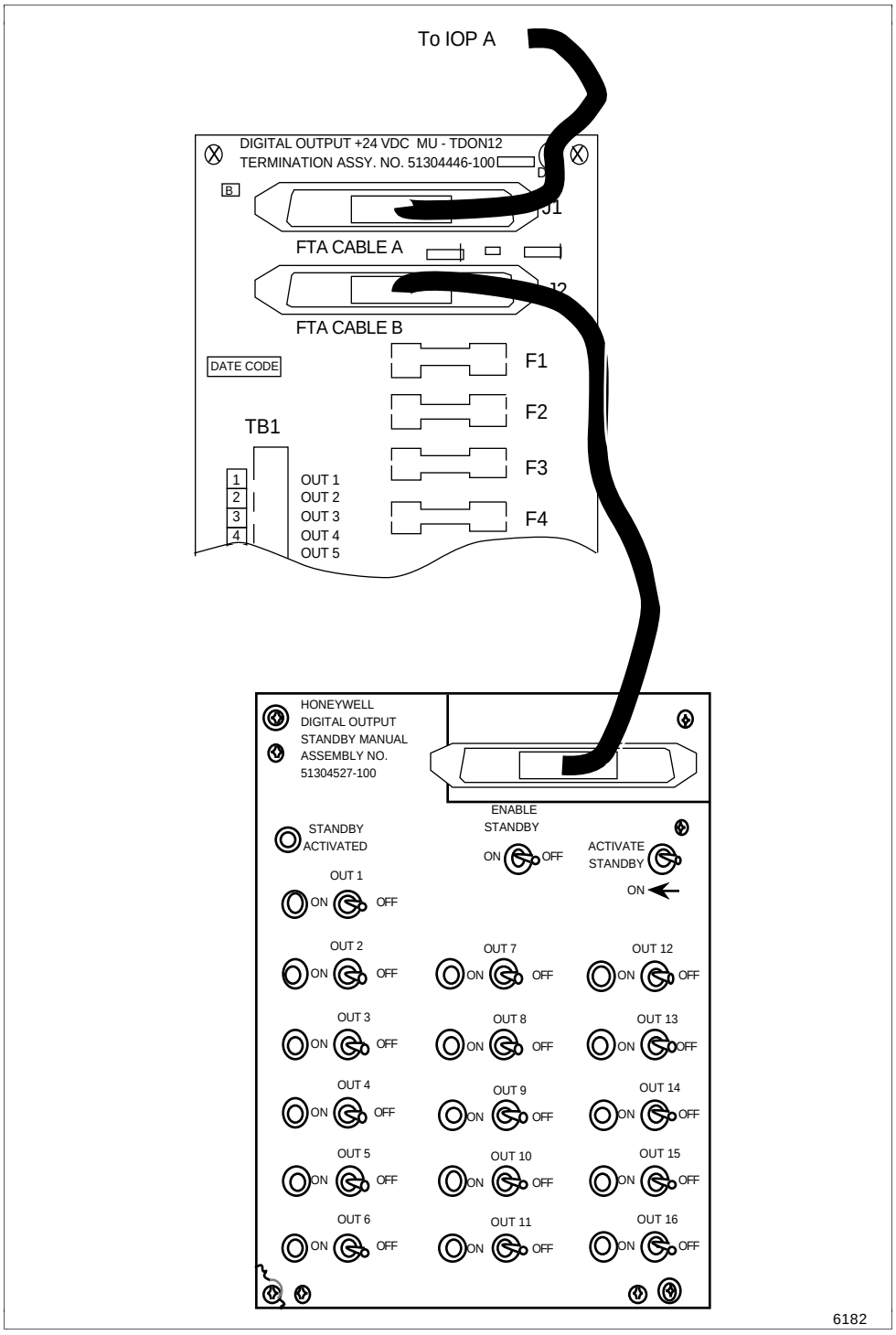
Continued on next page

6.3.2 Standby Manual Device Overview, Continued

DO Standby Manual device connection

Figure 6-3 illustrates the connection of a Digital Output Standby Manual device to a model MU-TDON12 24 Vdc Digital Output FTA.

Figure 6-3 Digital Output Manual Device Interconnection



Continued on next page

6.3.2 Standby Manual Device Overview, Continued

Device interchangeability

There is an interchangeability problem with the Digital Output Standby Manual devices. The software Release 300, or later, model of the Digital Output Standby Manual device is not compatible with a Release 230, or earlier Digital Output FTA, nor is the Release 230, or earlier, Digital Output Standby Manual device compatible with a software Release 300, or later, FTA. Software Release 300, or later, devices are identified by having phone-type cable connectors, while software Release 230, or earlier, devices have DIN-type cable connectors.

DIN to phone connector adaptor cable

However, a DIN to phone connector adaptor cable, Honeywell part number 51201561-xxx, where the suffix "xxx" is the length of the cable in meters, can be used to interconnect an incompatible Digital Output Standby Manual device to an FTA, provided the circuit board inside the Digital Output Standby Manual device is the proper revision as follows.

- Digital Standby Manual device with phone connector
  PWB 51304451-100, Revision B
- Digital Standby Manual device with DIN connector
  PWB 51304076-100, Revision C

Board revision level

The 24 Vdc required by the Digital Output Standby Manual device will be missing if the device's circuit board is not at the listed revision level.

The R230 and R300 Analog Output Standby Manual devices do not have the same problem.

6.3.3 AO Standby Manual Device Operation

Purpose

There are two models of the Analog Output Standby Manual (AOSM) device. Both models provide the same primary function, which is to control the loads connected to an Analog Output FTA while its associated Analog Output IOP can be removed from service and replaced. The Analog Output Standby Manual device connects to the Analog Output FTA and provides control of any or all eight of the outputs that are normally controlled by the IOP.

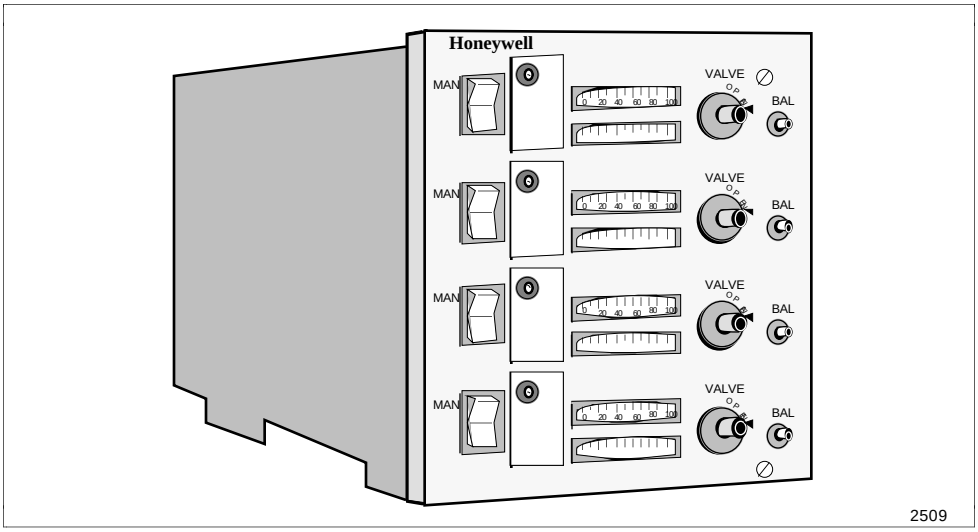
Two models

The original Analog Output Standby Manual device model is not as convenient to use as the newer compact Analog Output Standby Manual device model which also offers more features. A description and the use of both models is discussed in the information that follows.

Original Analog Output Standby Manual device overview

The original model MU-SMAC01/MU-SMAC02 Analog Output Standby Manual (AOSM) device, as shown in Figure 6-4, monitors the outputs of an Analog Output (AO) IOP by displaying its output values on meters as a percentage of the range. Figure 6-4 illustrates one of the two Analog Output Standby Manual device assemblies that comprise the Analog Output Standby Manual device. When you press one of the **BAL** switches on the Analog Output Standby Manual device, the corresponding meter indicates the IOP's output value. Using the **VALVE** knob, you adjust the Analog Output Standby Manual device's output to match the output of the IOP. Then, you switch control of the FTA output to the Standby Manual device by moving the mode switch to the **MAN** position.

Figure 6-4 Original Analog Output Standby Manual Device (Two per device)



Continued on next page

Control of FTA outputs

To use an Analog Output Standby Manual device to control the FTA outputs to the field while an Analog Output IOP or the IOP switching module on a redundant Analog Output FTA is replaced, place all of the mode switches on the Standby Manual device to the position opposite the **MAN** position after you have duplicated the IOP's outputs.

FTA connection

Connect the Standby Manual device to the **STANDBY MANUAL** connector on the FTA with its cable.

ATTENTION

ATTENTION—If the FTA cable to be connected to the Standby Manual device has a phone-type connector, use the adapter cable, Honeywell part number 51201561-xxx (The suffix "xxx" represents the length of the cable in meters), to make the connection.

Standby Manual device control procedure

Use the HPM Status display to save the Checkpoint for the IOP, and then use the following procedure to provide Standby Manual device control of the FTA field devices.

Step	Action
1	For the first output, press the **BAL** switch and note the IOP's output value.
2	Release the **BAL** switch and adjust the **VALVE** knob to make the output of the Analog Output Standby Manual device equal to the output of the IOP.
3	Place the mode switch for this output in the **MAN** position.
4	Repeat steps 1 through 3 for all remaining outputs from the IOP.
5	Remove and replace the IOP or switching module, as appropriate, and proceed to the **Normal IOP Control** procedure.

Continued on next page

Normal IOP control procedure

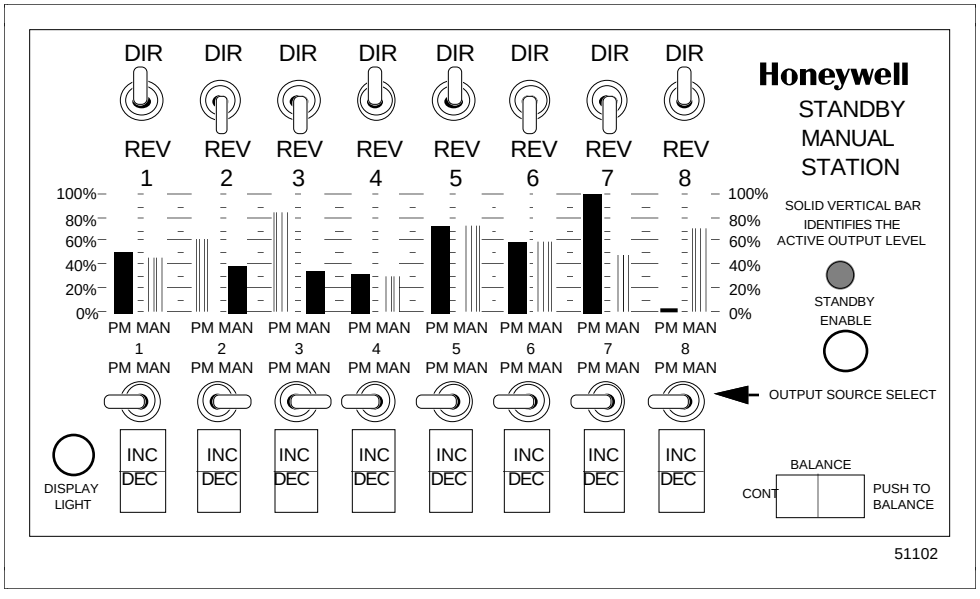
Use the following procedure to return to normal IOP control of the FTA field devices.

Step	Action
1	Use the HPM Status display to restore the Checkpoint to the replacement IOP, to select **RUN STATES**, and to **STARTUP** the IOP.
2	For the first point controlling the output of the IOP, use the point's Detail or Group display to place the point in the Manual mode.
3	Use the Detail or Group display to adjust the first IOP output to match that of the Analog Output Standby Manual device.
4	On the Analog Output Standby Manual device, change the mode switch for this output to the position opposite the **MAN** position.
5	Use the point's Detail or Group display to select the Normal mode for the point.
6	Repeat steps 2 through 5 for all remaining outputs from the IOP.
7	Disconnect the Analog Output Standby Manual device cable from the **STANDBY MANUAL** connector on the FTA, if desired.

Compact Analog Output Standby Manual device overview

The compact Analog Output Standby Manual (AOSM) device display panel, as shown in Figure 6-5, monitors the outputs of an Analog Output (AO) IOP as well as the AOSM itself, presenting their output values on the display panel as a percentage of the range. It can be ordered by Honeywell part number 51401926-100.

Figure 6-5 Compact Analog Output Standby Manual Device



Continued on next page

6.3.3 AO Standby Manual Device Operation, Continued

Features

The Analog Output Standby Manual device has the following features.

- The Analog Output Standby Manual device will accept the standard IOP to FTA cables with either DIN or phone type connectors.
- The Analog Output Standby Manual device can be powered by any of two methods.
  1. The HPM card file backplane through its connection to the **STANDBY MANUAL** connector on the FTA.
  2. By applying 110 or 220 Vac to connector at the side of the AOSM. The universal power supply in the AOSM will accept 100 to 240 Vac, 50/60 Hz.
- The panel display shows the 4-20 milliamp current levels in a 0% to 100% scale for all eight IOP outputs as well as the level of all eight AOSM outputs.
- The toggle switches are a “tamper-proof” style that require the operator to lift up on the bat handle before changing the switch position.
- The compact AOSM’s output current and the its **OUTPUT SOURCE SELECT** switches are disabled when the device is first connected to the FTA, the **STANDBY ENABLE** indicator is extinguished, or the cable to the FTA is disconnected.
- When the AOSM is enabled by depressing the **STANDBY ENABLE** switch, the **STANDBY ENABLE** indicator is illuminated and the **OUTPUT SOURCE SELECT** switch settings are active.
- The balancing of the AOSM output values to equal the IOP output values is performed automatically, either continuously, or by single snapshot action. Balancing in the other direction, IOP to AOSM, is an operator function.
- A **DIR/REV** switch for each channel flips the display and reverses the **INC/DEC** action relative to the actual current level. In the **DIR** position, 4 mA equals 0% and 20 mA equals 100%. The **INC** position of the **INC/DEC** switch will increase current and the **DEC** position will decrease current. With the **DIR/REV** switch in the **REV** position, 20 mA equals 0% and 4 mA equals 100%. The **INC** position of the **INC/DEC** switch will decrease current and the **DEC** position will increase current.

Continued on next page

6.3.3 AO Standby Manual Device Operation, Continued

Standby Manual device control procedure

Use the HPM Status display to save the Checkpoint for the IOP, and then use the following procedure to provide Standby Manual device control of the FTA field devices.

Step	Action
1	Be sure all the **OUTPUT SOURCE SELECT** switches are in the **PM** position.
2	Place the **DIR/REV** switches in the correct position for all eight channels.
3	Connect a standard IOP to FTA cable between the **STANDBY MANUAL** connector on the FTA and the AOSM.
4	Verify that all **OUTPUT SOURCE SELECT** switches are in the **PM** position.
5	The **BALANCE** switch has three positions, left (**CONT**), center (inactive), and right (**PUSH TO BALANCE**). Select the left or right position. **CONT** Position In the **CONT**inuous (left) position, the switch remains toggled and all the channels with their **OUTPUT SOURCE SELECT** switch in the **PM** position will automatically have their Standby Manual device output level continuously set equal to the IOP level. Manual **INC**rement and **DEC**rement control for a channel is not possible when a channel is in the **PM** position while the **BALANCE** switch is in the **CONT** position. **PM** Position In the **PUSH TO BALANCE** (right) position, the position is momentary and all channels with their **OUTPUT SOURCE SELECT** switch in the **PM** position will automatically have their Standby Manual device output level set equal to the IOP output level. However, this balance method is a single event and the switch returns to the center position when it is released. Any subsequent change in the IOP's output level will not be transferred to the Standby Manual, but the **INC**rement and **DEC**rement control for a channel can alter the Standby Manual device's current level.
6	The **STANDBY ENABLE** switch can now be depressed. The green LED illuminates to indicate that the FTA is now ready for control by the Standby Manual device.
7	Placing any or all of the **OUTPUT SOURCE SELECT** switches in the **MAN**ual position will automatically place all eight IOP channels in the Standby Manual mode.
8	When all eight **OUTPUT SOURCE SELECT** switches are in their **MAN**ual position, the Analog Output IOP can be placed in the Idle state and removed.

Continued on next page

Normal IOP control procedure

Use the following procedure to return to normal IOP control of the FTA field devices.

Step	Action
1	Use the HPM Status display to restore the Checkpoints to the replacement IOP, to select RUN STATES, and to STARTUP the IOP.
2	For the IOP's first point that controls the channel 1 output level of the IOP, use the point's Detail or Group display to place the point in the Manual mode.
3	Use the Detail or Group display to adjust the first IOP output to match that of the Analog Output Standby Manual device.
4	When the output level for channel 1 matches the output level of the Analog Output Standby Manual device, place the **OUTPUT SOURCE SELECT** switch for channel 1 in the **PM** position. The IOP will now be controlling channel 1.
5	Use the point's Detail or Group display to select the Normal mode for the point.
6	Repeat steps 2 through 5 for IOP channels 2 through 8.
7	Disconnect the Analog Output Standby Manual device cable from the **STANDBY MANUAL** connector on the FTA, if desired.

6.3.4 DO Standby Manual Device Operation

Purpose

The primary function of the model MU-SMDC02 or model MU-SMDX02 Digital Output Standby Manual (DOSM) device is to control Digital Output FTAs while the associated Digital Output IOP card is serviced. Except in the case of the +24 Vdc nonisolated FTA which has no relays, the FTA's relays are controlled, not their loads.

Secondary function

A secondary function of the Digital Output Standby Manual device is to indicate the state of each IOP output (LED on = output on). The LEDs indicate the output state of the IOP as soon as the connection is made.

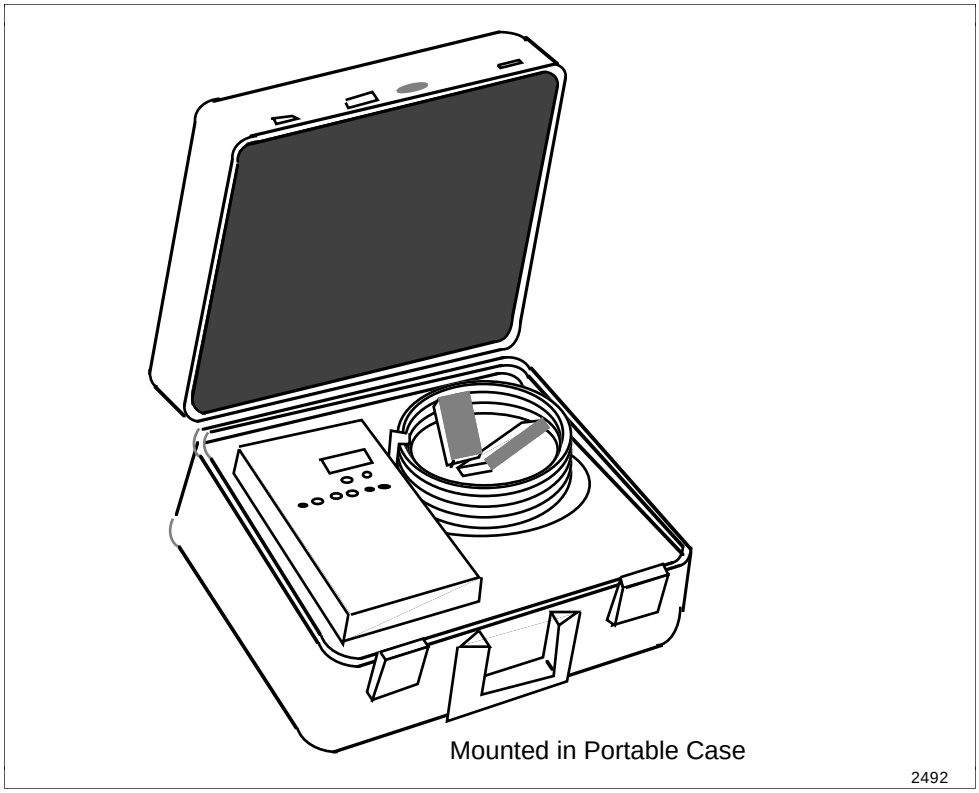
Mounting locations

The model MU-SMDX02 Digital Output Standby Manual device can be mounted in an HPM cabinet on an FTA Mounting Channel. The model MU-SMDC02 Digital Output Standby Manual device is mounted in a carrying case for portable applications.

Connection

Connection of the Digital Output Standby Manual device to the FTA Standby connector is made with a standard IOP to FTA cable. A 3-meter cable is included with the model MU-SMDC02 Digital Output Standby Manual device that is shown in Figure 6-6.

Figure 6-6 Model MU-SMDC02 Portable Digital Output Standby Manual Device



Continued on next page

6.3.4 DO Standby Manual Device Operation, Continued

Output control switches disablement

The Digital Output Standby Manual device's output control switches are disabled when the DOSM is first connected to the FTA, or whenever the **ENABLE STANDBY** switch on the DOSM is in the **OFF** position.

Switch activation

When the **ENABLE STANDBY** switch is in the **ON** position, momentary operation of the **ACTIVATE STANDBY** switch latches the manual mode of the Digital Output Standby Manual device and activates the 16 output switches to control the FTA as discussed below.

ATTENTION

ATTENTION—The IOP to FTA cable, from the card file backplane to the FTA, must be connected to carry the +24 Vdc and the common from the IOP backplane to the FTA and the Digital Output Standby Manual device. Also, the Digital Output Standby Manual device cannot be used with the 24 Vdc nonisolated Digital Output FTA if the FTA load voltage for any output is other than +24 Vdc.

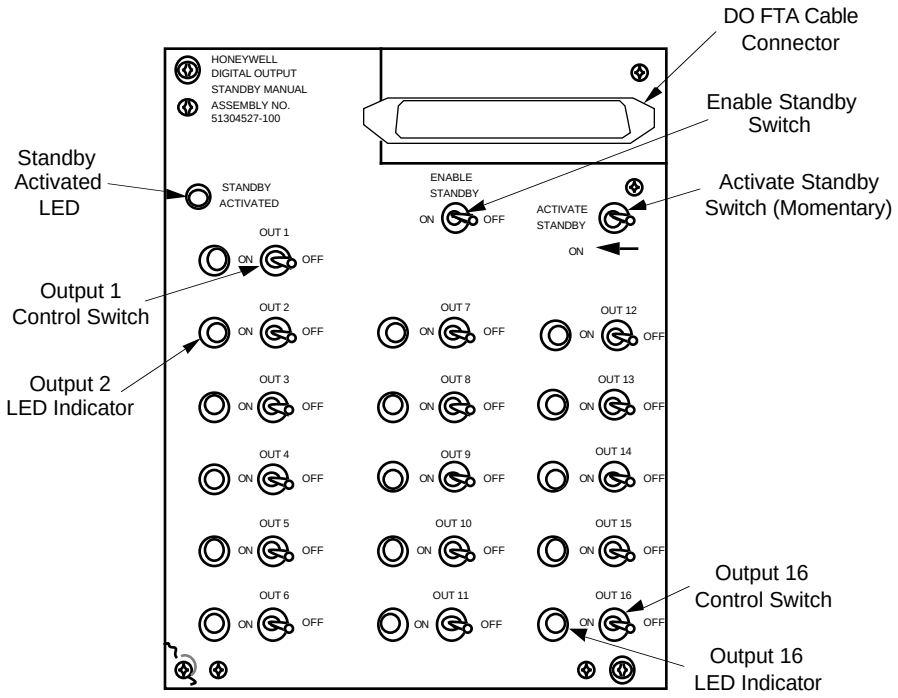
Continued on next page

Standby Manual device control procedure

Use the HPM Status display to save a Checkpoint for the IOP(s), if desired, and then use the following procedure to provide Standby Manual device control of the FTA field devices.

Step	Action
1	Place **ENABLE STANDBY** switch on the Digital Output Standby Manual device in the **OFF** position.
2	Connect the Digital Output Standby Manual device cable to the **FTA CABLE B** connector, J2, on the Digital Output FTA.
3	When the Digital Output Standby Manual device is connected to the connector on the Digital Output FTA, all "on" IOP outputs light their corresponding indicator on the Digital Output Standby Manual device. See Figure 6-7 for an illustration of the model MU-SMDX02 Digital Output Standby Manual device panel. If you only want to display outputs, stop at this point.

Figure 6-7 Digital Standby Manual Device Panel



Continued on next page

Standby Manual device control procedure, continued

Step	Action
4	If you want to use the Digital Output Standby Manual device to hold the current FTA output states while servicing the associated Digital Output IOP, set each of the 16 output switches equal to the output state displayed by the LEDs on the Digital Output Standby Manual device and perform Steps 5 through 7 below. You can also set any of the 16 output switches to an alternate state, if desired.
5	Place the **ENABLE STANDBY** switch on the Digital Output Standby Manual device in the **ON** position.
6	Toggle the momentary **ACTIVE STANDBY** switch on the Digital Output Standby Manual device. The **STANDBY ACTIVATED** LED should illuminate. This allows the Digital Output Standby Manual device's switch settings to control the Digital Output FTA and also send a status signal to the IOP to indicate that the connected Digital Output Standby Manual device is armed and possibly controlling FTA outputs.
7	While the Digital Output Standby Manual device is controlling outputs, the IOP can be placed in the idle mode or removed/replaced for servicing, and the FTA outputs will be held by the Digital Output Standby Manual device. After servicing the IOP, proceed to the **Normal IOP Control** procedure to restart the IOP.

ATTENTION

ATTENTION—While the Digital Output Standby Manual device and the FTA's associated IOP are both present and controlling outputs (they are connected in parallel to the FTA), either can override an "off" output from the other, but not an "on" output. Until the IOP is removed or reset, the Digital Output Standby Manual device's output LEDs indicate the resultant outputs actually delivered to the FTA's switching elements.

Continued on next page

Normal IOP control procedure

After using the Digital Output Standby Manual device to maintain FTA digital output states while servicing the associated Digital Output IOP, proceed with the following steps to return FTA output control to the IOP

Step	Action
1	Use the HPM Status display to restore the IOP database, then restart the IOP.
2	Activate the outputs on the IOP Slot Summary display at the Universal Station and ensure that the outputs agree with the 16 output switch settings on the Digital Output Standby Manual device. This allows the IOP to regain FTA output control and provide the same output states, if so desired, that existed before the Digital Output Standby Manual device established control.
3	Set the **ENABLE STANDBY** switch on the Digital Output Standby Manual device to the **OFF** position. The **STANDBY ACTIVATED** LED should be "off," indicating that the Digital Output Standby Manual device is no longer controlling the FTA digital outputs. Control has been returned exclusively to the IOP.
4	Remove the Digital Output Standby Manual device connection to the FTA, if desired.

ATTENTION

ATTENTION—When a digital output point indicates Standby Manual mode (**STDBYMAN**) on an operating display, such as Group or Detail, the output cannot be changed using that display. To set the point output to match the Digital Output Standby Manual device setting, the output point must be set using the IOP Slot Summary display.

6.3.5 HPMM or IOP Card Case Replacement

CAUTION

CAUTION—It is extremely important that you wear a properly connected Electrostatic Discharge (ESD) wrist strap while removing, handling, and installing these High-Performance Process Manager components. Follow the guidelines discussed in subsection 6.1.

Disassembly/assembly procedure

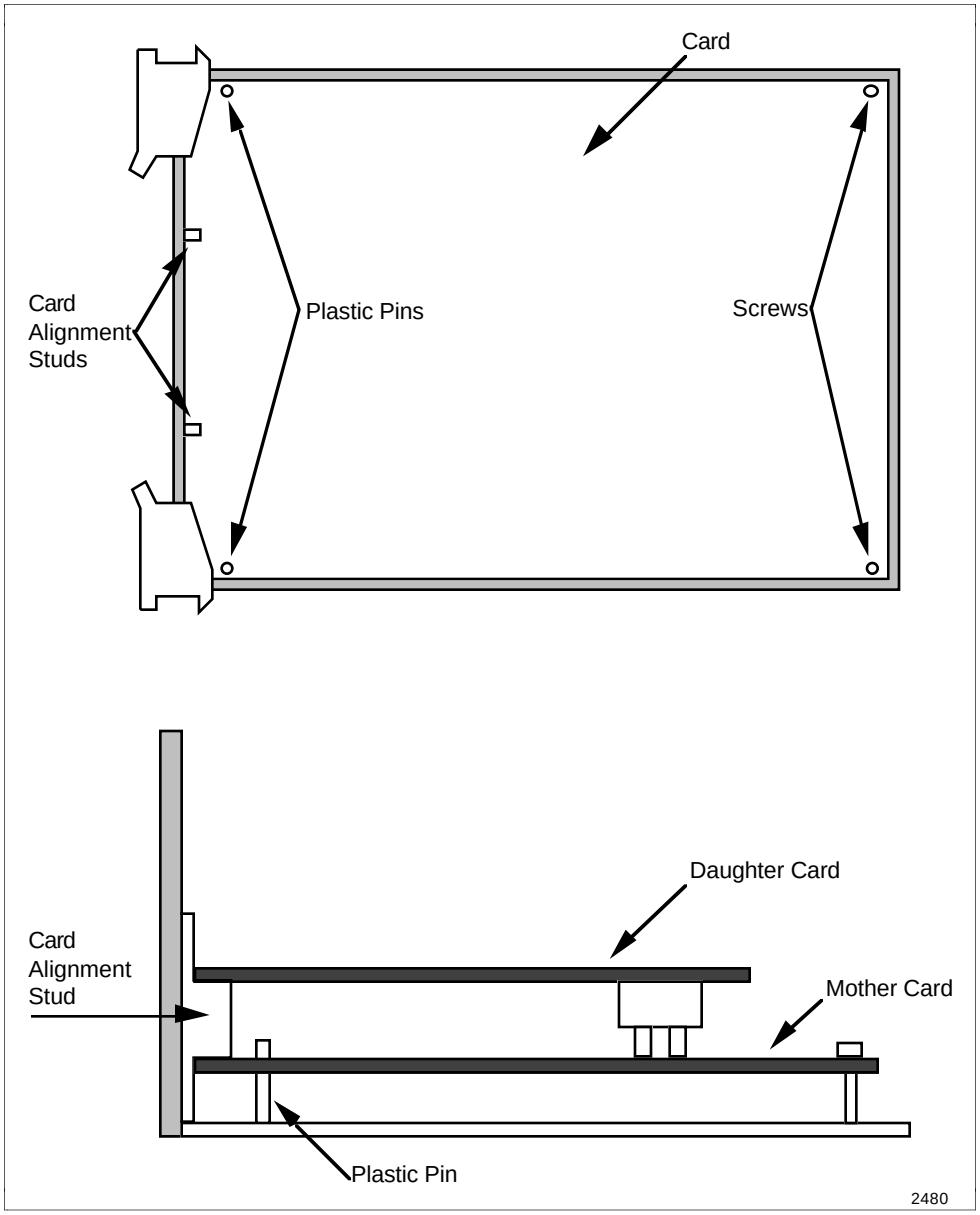
To replace the plastic case on a card assembly use the following procedure.

Step	Action
1	Remove the card assembly from the card file. Place the card on a static free work surface.
2	Remove the two screws at the corners near the connector edge of the card as illustrated in Figure 6-8.
3	Lift the connector end of the card to approximate 30 degree angle with the case.
4	Lift the card from the plastic pins at the front left corners of the circuit board. If the card has a daughter board attached, the plastic pins are hidden under the daughter circuit board.
5	To insert the card in the new case, place the front of the card on the plastic pins while holding the card at approximately a 30 degree angle. If a daughter board is attached, the two alignment studs at the front edge of the case must fit between the two circuit boards. See Figure 6-8.
6	Lay the card flat on the work surface and replace the two screws removed in Step 2.
7	Check the alignment of the LEDs with the openings in the front of the plastic case for visibility.
8	Reinstall the card in the card file.

Continued on next page

Card case illustration

Figure 6-8 Replacing HPMM or IOP Card Case



6.4 Field Termination Assembly

6.4.1 IOP to FTA Cable Replacement

Nonredundant IOP cable replacement

All outputs or inputs carried by the IOP to FTA cable, as well as 24 Vdc from the IOP that powers the FTA, will be disconnected when the cable is removed. The use of an Analog Output or Digital Output Standby Manual device, as discussed in subsection 6.3, may be appropriate to maintain the present outputs of an output type FTA.

Redundant IOP cable replacement

Before removing an IOP to FTA cable from a redundant IOP configuration, be sure that the FTA cable to be removed is not controlling analog output field terminals on the FTA or providing inputs. When the green **DS1** LED on an AO redundancy FTA is illuminated, the "B" FTA cable can be removed, since the "A" FTA cable is controlling the FTA output field terminals. When the green DS1 LED on an AO redundancy FTA is not illuminated, the "A" FTA cable can be removed, since the "B" FTA cable is controlling the FTA output field terminals. The HPM Status display at the Universal Station can also be used to determine whether the "A" or "B" FTA cable is controlling the FTA output field terminals.

For critical analog outputs, it is recommended that the "A" AO IOP be removed before the "A" FTA cable is removed. It is also recommended that the "B" AO IOP be removed before the "B" FTA cable is removed.

When removing FTA cables from High Level Analog Input (HLAI) IOPs, use the HPM Status display at the Universal Station to determine whether or not the cable being removed is being used to provide subsystem inputs.

6.4.2 FTA Replacement

WARNING

WARNING—Remove power from the FTA by unplugging the IOP to FTA cable before disconnecting the process wiring.

Replacement procedure

Use the following procedure to replace an FTA.

Step	Action
1	Unplug the cable(s) from the associated IOP card connector to the FTA at the FTA. Remove the field power serving the FTA to be replaced. Unplug the field wiring terminal-strip from the FTA. It is not necessary to unscrew the field wiring if compression terminals are used.
2	Remove the screws that hold the FTA to the mounting channel. Carefully remove the FTA.
3	Compare the replacement FTA with the removed FTA. Be sure any 250 ohm or zero-ohm resistors that have been clipped on the removed FTA are also clipped on the replacement FTA. Be sure all fuses are in place and jumpers are properly positioned.
4	Install the replacement FTA with the screws that were removed in step 2. Rotate them counterclockwise until they fall into the original threads, then tighten them clockwise. Reconnect the field wiring terminal connector and the cable from the associated IOP card(s).

ATTENTION

ATTENTION

- Connecting the HPMM's High-Performance I/O Link card to an FTA through its backplane connector causes continuous I/O Link errors to occur.
- Connecting the HPMM's High-Performance Comm/Control card to an FTA through its backplane connector could cause damage to the HPMM card set as well as the backplane.
- Inserting an HPM UCN Interface module in slot 1 (slot 9 in a Right 7-Slot card file) with an IOP present in the slot and configured as IOP A causes an IOP Configuration Mismatch status. IOP A erroneously determines that it is connected to the FTA B connector.

6.4.3 FTA Module and Relay Replacement

Replacement procedure

Modules and relays plug into the FTA circuit boards and are held in place by a retaining screw(s). Use the following procedure to replace a module or relay.

Step	Action
1	Remove the screw(s) holding the module or relay to the circuit board and then firmly lift it straight away until it is free.
2	Align the replacement module or relay with the holes and connector on the FTA circuit board before inserting it. Replace the retaining screw(s).

LLAI Module replacement

The LLAI plug-in module can be replaced while power is applied to the FTA. After replacement, power initialize the LLAI IOP. The initialization will initiate a background diagnostics. Allow at least two (2) minutes for it to complete before analyzing the results.

AO redundancy switching module replacement

Before removing the Analog Output (AO) Redundancy Switching Module from an AO Redundancy FTA for testing or replacement, be sure that the associated "A" AO IOP is controlling the FTA outputs. When the green **DS1** LED on the FTA is illuminated, the associated "A" AO IOP is controlling the FTA's output. The HPM Status display at the Universal Station also can also be used to determine if the "A" AO IOP is controlling the FTA output.

For critical analog outputs, it is recommended that the "B" AO IOP be removed, or an Analog Output Standby Manual device be connected before removing the Analog Output Redundancy Switching Module.

SDI/SI module and fuse replacement

Before attempting to replace any components on a Serial Device Interface (SDI) or Serial Interface (SI) FTA, remove power from the FTA by loosening the captive screws on the connector J1 and removing the connector. After power has been removed from the FTA, module M1 and fuses F1 and F2 can be removed and replaced as applicable.

When the removal/replacement process is complete, reconnect J1 and tighten the captive screws. As power is applied to the FTA, the FTA will initiate background diagnostics, followed by normal FTA operation.

Continued on next page

Galvanic isolation module replacement

If the field device, controlled by a Galvanic Isolation Module that must be replaced, is an output device, be sure the loss of control is acceptable. Also, when the environment is Division 2, be sure the atmosphere is nonhazardous.

The module can be removed and replaced while power is applied to the FTA. Remove the module's pluggable field connector. Loosen the screws that retain the module. Lift the module from its connector on the FTA and replace it. Reinstall the pluggable field connector.

6.5 Card File Replacement

Replacement procedure

Use the following procedure to replace a card file.

Step	Action
1	Disconnect all cables attached to the card file.
2	Remove the side plates connecting the card file to the card file above and/or below by first removing the two screws at the inside of the panel.
3	Loosen, but do not remove, the four screws holding the card file to its supports.
4	Grasp the card file firmly and lift it about 1 cm (1/2 inch) to release the card file into your hands.
5	Install the replacement card file in a reverse manner, making sure it is engaged by all four mounting screws. Tighten the screws when the card file is in place. Reconnect the cables that were disconnected in step 1.

6.6 Power System

Introduction

The subsections that follow describes the removal and replacement of major assemblies in the Power System.

If all options are installed, most of the major assemblies in the Power System can be removed and replaced while the HPM remains in operation because of Power Supply Module redundancy and battery backup power. Observe all precautions mentioned in this text when replacing the Power System components.

CAUTION

CAUTION—Batteries may contain toxic materials that are not biodegradable. Batteries should be disposed of safely in accordance with local laws and regulations.

6.6.1 CMOS Battery Replacement

NiCad batteries

The three NiCad batteries that are installed in the Standard Power System to provide standby power for the CMOS memory have a tendency to age over a period of time. Aging occurs even if the batteries have been regularly recharged throughout their lifetime. For this reason, the NiCad batteries should be replaced after every two years of operation.

Alkaline batteries

The alkaline batteries that are installed in the AC Only Power System are not rechargeable and, therefore, must be replaced more often. A six month replacement cycle is suggested, unless an equipment power failure has occurred for a prolonged period. Then, the batteries should be replaced.

Replacement procedure

To replace the batteries, do the following.

Step	Action
1	Remove the old batteries from the battery holder and replace them with fresh ones. It is not necessary to remove power from the batteries while they are being replaced.
2	Observe and match the polarity marked on the case of each battery and the holder. After all the batteries are in place, rotate each one slightly with your finger to assure it makes good contact with the holder.

6.6.2 48 V Backup Battery Replacement

Battery operational and service life

The lead acid batteries provide 20 minutes of standby power for the HPM Power System and have a normal stand-by service life of 4 to 5 years. However, usage and high environmental temperatures will reduce the service life. For this reason, environmental temperature, battery storage time, and battery usage should be monitored and recorded. In the absence of this attention, it is recommended the battery performance be checked on a yearly basis, or be replaced every 3 years to insure proper performance.

Battery performance

All batteries of the same capacity, rating, and specifications, do not provide equivalent performance or reliability. For optimum system backup realization, use only Honeywell recommended and approved batteries.

Continued on next page

48 V Battery Pack service life

The battery end-of-life is defined as the time when the battery capacity, meaning its ability to accept and hold a charge, has decayed to 60% of the original capacity. There are several factors that determine useful service life. The standby service life is directly reduced by events other than a continual 20°C standby condition and are defined as follows.

- Standby (float) service life means that the batteries are connected to a charger and only occasionally discharged. Honeywell 48-volt batteries are designed to operate in standby (float) service for 4 to 5 years at 20°C. The service life of a battery can be shortened by an improper charging voltage. The charging voltage from the Power Supplies should be checked every 6 months for the proper voltage level. See subsection 6.5.2.2 for the recommended procedure.
- As shipped from Honeywell, the batteries are fully charged. However, if a system is stored in a nonpowered state, the batteries will self-discharge and can become unusable. The time required for this to happen is a function of storage temperature.

0° to 20°C	12 months
21° to 30°C	9 months
31° to 40°C	5 months
41° to 50°C	2.5 months

- Batteries should not be left in a discharged condition for extended periods of time, as this strongly affects the ability of the battery to accept a charge thereafter. The batteries should be charged periodically if they are stored or in an nonpowered system.
- The HPM provides proper charging current to the batteries while the subsystem is powered up and running. Whenever ac power is removed from the subsystem, the Power System automatically draws power from the batteries to maintain the subsystem's 24 Vdc power. Anytime the system is intentionally shutdown and left nonpowered, the **BATTERY** switch at the front of the Power System assembly should be placed in the **OFF** position to prevent discharge of the batteries.
- Service life is directly reduced by high ambient temperature. Heat destroys batteries. While the operating temperature range is -15°C to 50°C, maximum service life will be realized when the batteries are operated in an ambient of 20°C. "Brief usage,"that is, a few days, at higher temperatures will have no adverse effect on the service life. However, if such usage is over extended periods of time or occurs repetitively (such as a environment that is not air-conditioned), the service life will be reduced. This reduction may be as much as 20% of service life (1 year) for each 10°C above the reference ambient of 20°C.

Continued on next page

48 V Battery Pack service life, continued

- Service life is directly reduced by the number of discharges and the depth of each discharge. The batteries can provide 200 cycles at 100% depth of discharge, 550 cycles at 50% depth of discharge, 1200 cycles at 30% depth of discharge, or 2000 cycles at 10% depth of discharge. This effect is superimposed on the standby aging effect stated above.

  With an expected 5 year life, 200 cycles would represent one power outage approximately every 9 days, or approximately 2000 ampere-hours of 24 Vdc subsystem backup.

Battery charge voltage check procedure

Use the following procedure to verify that the output voltage to the 48 Volt Battery Pack is proper.

Step	Action
1	Locate the test points marked "**COMMON**" (-) and "**BATTERY**" (+) at the front of the primary Power Supply Module and connect a dc voltmeter with an accuracy of +/- 0.05 volts across the test points.
2	The voltage should read between 54.0 volts minimum to 55.2 volts maximum at 20°C. For each degree the battery enclosure temperature deviates from 20°C, the following adjustments in Power Supply Module's battery charge output voltage are applicable. Above 20°C, the battery charge voltage limits are decreased by 72 mv/deg C. Below 20°C, the battery charge voltage limits are increased by 72 mv/deg C. If the charge voltage is outside of these limits, replace the module.
3	This step and step 5 should be performed during plant shutdowns since it requires disconnecting the battery pack and placing the redundant Power Supply Module's power switch in the **OFF** position. Disconnect the battery pack. With the voltmeter connected to the primary Power Supply Module's battery test points, place the redundant Power Supply Module's power switch in the **OFF** position. The voltage should not fall below the minimum voltage specified in step 3. If it does, replace the redundant Power Supply Module.
4	Place the redundant Power Supply Module's power switch in the **ON** position. Move the test leads to the battery test points on the redundant Power Supply Module and place the primary Power Supply Module's power switch in the **OFF** position. The voltage should not fall below the minimum voltage specified in step 3. If it does, replace the redundant Power Supply Module.
5	Reconnect the battery pack to the Power System.

Continued on next page

6.6.2 48 V Backup Battery Replacement, Continued

End of Battery Pack life check

The battery pack can be checked for the end of its life using the following procedure.

Step	Action
1	Set the **BATTERY** switch on the power system control panel in the **OFF** position**.** Remove the Power System's lower cover. You can use either a screwdriver or a coin to remove the two screws holding it in place.
2	Release the Power System cord connector at the battery.
3	Disconnect the battery pack from the subsystem.
4	Attach two pairs of leads to the battery pack terminals. One pair of leads are for attaching a load resistor and must be a minimum of 1.0 mm^2 (18 AWG) wire. The second pair are for attaching a voltmeter and can be a smaller gauge.
5	Select a voltmeter range of 60 Vdc for monitoring the battery voltage. Attach the voltmeter to the smaller gauge leads.
6	The battery load for the test must be 5 ohms and rated at 500 watts. Five 1-ohm, 100-watt resistors placed in series is recommended.
7	Attach the resistors to the larger test leads. Note the time of attachment.
8	The battery voltage must remain above 40 Vdc for a minimum of 20 minutes. If the battery voltage is not maintained, the battery is considered at the end of its life and must be replaced.
9	All batteries of the same capacity, rating, and specifications, do not provide equivalent performance or reliability. For optimum battery backup performance, use only Honeywell recommended and approved batteries.

Continued on next page

Battery pack removal

Using the following procedure will cause alarms to go off, so be sure to notify Plant Operations in advance that an alarms will occur.

Use the following procedure to remove the battery pack.

Step	Action
1	Set the **BATTERY** switch on the power system control panel to the **OFF** position**.** Remove the Power System's lower cover. You can use either a screwdriver or a coin to remove the two screws holding it in place.
2	Release the Power System cord connector at the battery.
3	Remove two screws holding the front lip of the battery pack to the base of the Power system chassis.
4	Move the Power System cord out of the way so it will not be damaged when the battery pack is removed.
5	Slowly slide the battery pack out into your hands, but be careful, the pack is heavy.

Battery Pack installation

Use the following procedure to install a Battery Pack.

Step	Action
1	Slide the new battery pack into the Power System chassis, being careful not to damage the battery pack connector cord within the compartment.
2	Secure the pack by replacing the two screws through the front lip of the pack into the base of the chassis.
3	Connect the pack to the system by inserting the polarized battery pack plug into the polarized connector cord in the compartment. Carefully dress the cord and connectors to prevent damage.
4	Replace the metal cover.
5	Apply power to the battery by switching the **BATTERY** switch to the on position. Unless it is already in a charged condition, the battery pack may need to be initially charged for 16 hours before it will be capable of sustaining power to the High-Performance Process Manager.

6.6.3 Power Supply Module Replacement

Introduction

The HPM will remain in operation while replacing a Power Supply Module, provided the redundant Power Supply Module option is installed. Be sure to notify Plant Operations that you will cause alarms during the replacement process.

CAUTION

CAUTION—Do not remove both Power Supply Modules at the same time if the system is operational.

The batteries will not power the system unless at least one Power Supply Module is present.

If one of the Power Supply Modules fails, the batteries will not be drained.

ATTENTION

ATTENTION—If the primary (left side) Power Supply Module is removed from the system or turned off, the 6 Vac is not provided to the card files because the redundant Power Supply Module does not provide 6 Vac. This can cause a Soft Failure Alarm Notification for any LLAI card that is present.

Replacement procedure

Use the following procedure to replace a Power Supply Module.

Step	Action
1	If the Power Supply Modules have ac present (**AC In** LED on), the **BATTERY** switch can be placed in the **OFF** position. Place the switch in the **OFF** position before removing the Power Supply Module. Set the recessed toggle switch on one, and only one, Power Supply Module in the down (off) position. Remove two screws at the bottom of the module that hold it to the shelf of the power system chassis.
2	Pull the Power Supply Module straight out of the housing.
3	Before installing the replacement Power Supply Module, be sure the recessed toggle switch is off.
4	Carefully slide the replacement module into the Power System chassis. Don't slam it into its housing. Be careful and be sure that the contacts at the back of the module mate properly with the fixed contacts at the back of the Power System backplane.
5	Secure the replacement module with two screws at the bottom of the module, then set the recessed toggle switch to the on position. Check that the green indicators on the supply are operating satisfactorily and that alarms can be reset.
6	Be sure to place the **BATTERY** switch in the **ON** position.

6.6.4 CMOS Backup Assembly Replacement

Introduction

Replacement of the CMOS Backup Assembly requires the removal of the redundant (right side) Power Supply Module. See subsection 6.6.3 for removal of the Power Supply Module.

Figures 2-28 and 2-29 are an illustrations of the CMOS Battery Backup assembly, and Figures 2-26 and 2-27 illustrate the layout of the Standard Power System backplane with the location of the CMOS Battery Backup assembly connector.

Replacement procedure

Use the following procedure to replace the CMOS Backup assembly.

Step	Action
1	Remove the screw located at the front middle of the CMOS Backup Assembly.
2	Extract the circuit board from the Power System backplane assembly.
3	Insert the replacement circuit board in the connector on the Power System backplane assembly and fasten the screw.

6.7 Cabinet

Cabinet side panels (Markhon)

To remove the cabinet side panels, either for cabinet complexing or for service requirements, remove the two external Phillips screws, lift up on the side panel approximately 1 to 2 inches, and pull the panel outwardly. If the panel does not release, additional lifting of the panel may be required.

Cabinet side panels (Rittal)

To remove the cabinet side panels, either for cabinet complexing or for service requirements, remove the six internal Phillips screws, lift up on the side panel approximately 1 to 2 inches, and pull the panel outwardly. If the panel does not release, additional lifting of the panel may be required.

6.8 I/O Link Extender Optical Coupler Module Replacement

Introduction

Before removing a defective fiber Optical Coupler module, it is necessary to remove its associated I/O Link Extender card to prevent the transmission of erroneous signals on the I/O Link.

Replacement procedure

Use the following procedure to replace the I/O Link Extender coupler

Step	Action
1	Grasp the upper and lower extractors on the I/O Link Extender card and pull them outward in unison. The card should move outward into your hands. Place the card on antistatic material, or in an antistatic container.
2	Remove the fiber optic coupler by grasping the coupler firmly in your hand and pulling it towards you. Place the coupler on antistatic material, or in an antistatic container.
3	Replace the defective coupler, reversing step 2.
4	Reinstall the I/O Link Extender, reversing step 1.
5	If you replaced a Standard I/O Link Extender Optic Coupler module, you must initialize both ends of the link(s) by manually resetting the I/O Link Extender cards using the upper card extractor on the card. When a Long Distance I/O Link Extender Optical Coupler module is replaced, the reinstallation of the I/O Link Extender card produces the initialization at both ends of the link.

Section 7 – IOP Calibration Procedures

7.1 Overview

Section contents

The topics covered in this section are:

	Topic	See Page
7.1	Overview	379
7.2	LLAI, HLAI, and AO IOP Calibration	380
7.2.1	Common Calibration Procedures	380
7.2.2	Precision Test Equipment Required	380
7.2.3	LLAI IOP Calibration Procedure	381
7.2.4	Nonredundant HLAI IOP Calibration Procedure	388
7.2.5	Redundant HLAI IOP Calibration Procedure	391
7.2.6	Nonredundant AO IOP Calibration Procedure	393
7.2.7	Redundant AO IOP Calibration Procedure	395
7.2.8	LLMux IOP Calibration Procedure	397
7.3	Thermocouple Input Accuracy Verification	399

Introduction

This section describes the calibration procedures used to calibrate the High-Performance Process Manager's (HPM's) IOPs.

WARNING

SHOCK HAZARD

Calibration may require access to hazardous live circuits and should only be performed by a qualified service person. More than one switch may be required to deenergize units before calibration.

No manual adjustments

There are no manual adjustments, such as Power Supply Module settings in the HPM. However, there are some semiautomatic calibration procedures for the Low Level Analog Input (LLAI), High Level Analog Input (HLAI), and Analog Output (AO) subsystems that may be required periodically.

CAUTION

CAUTION—Do not attempt recalibration without the proper equipment and a working knowledge of the equipment.

7.2 LLAI, HLAI, and AO IOP Calibration

7.2.1 Common Calibration Procedures

Introduction

Each LLAI, AO, and HLAI subsystem maintains on-board calibration constants for each analog channel that is stored in nonvolatile memory. Field calibration can probably be an annual event or more often, if necessary.

IOP or FTA substitution

Honeywell recommends that if possible, substitution be used when it is suspected that an IOP or FTA is out of calibration, rather than recalibrate the IOP or FTA in an on-line HPM.

7.2.2 Precision Test Equipment Required

Precession equipment is a necessity

You will need precision equipment to accurately recalibrate these subsystems. **Do not attempt recalibration without proper equipment and working knowledge of the equipment.** Table 7-1 lists typical precision test equipment that can be used.

Table 7-1 Typical Precision Test Equipment

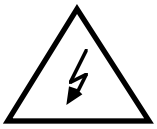
Item	Tolerance	Vendor	Model
Programmable Voltage Source: (with 10 V and 100 mV range)	±(0.002% setting + .0005% range +3 µV)	Electronic Development Co. 11 Hamlin Street Boston, MA 02127	501 J1 (with option D)
Precision Resistors: 100 ohm 500 ohm 2000 ohm	± 0.005% ± 0.005% ± 0.005%	C. T. Gamble 605 Perkins Lane Delanco, NJ 08075	1608AL or 1608PC for each
Digital Multimeter with 10 V range (1 µV/count) and 100 mV range (0.1 µV/count)	± 0.0025 reading + 40 counts	John Fluke Mfg. Co., Inc. PO Box C9090 Everett, WA 98206	8505A

Equipment requirements

The following equipment requirements are recommended.

- A precision voltage source and a Digital Multimeter is required for thermocouple, voltage, and current calibration.
- A precision thermocouple simulator is required to verify the accuracy of the thermocouple inputs.
- A precision resistor of the appropriate value is required for each RTD input to be calibrated.

7.2.3 LLAI IOP Calibration Procedure



CAUTION, RISK OF ELECTRIC SHOCK

Seven ranges

The Low Level Analog Input has seven different ranges that require calibration on a per slot basis, and a special range type for its reference junction calibration. At any one time, only one of the given gain ranges is being used by a given slot. Each range usage is independent from another slot's usage.

Calibration affects eight slots

Although the LLAI performs calibration on an individual slot basis, only calibration affecting all eight slots can be performed.

Range type selection

Calibration of a slot assumes that the range type selected is applied to the slot. The range type is internally derived from the slot's current configuration of sensor type (**SENSRTYP**), PV character (**PVCHAR**), and thermocouple range option (**TCRNGOPT** for a thermocouple input).

ATTENTION

ATTENTION—The user is responsible for reconfiguration of the slots so that the input voltage or resistor applied to each channel is appropriate for the configuration. Any violation, due to a configuration mismatch during calibration, will result in calibration abort errors.

CAUTION

CAUTION—Although mixed ranges of calibration are allowed, never configure slot 1 as an RTD input if there is at least one slot configured for a thermocouple. This is because the reference junction for a thermocouple input is connected to slot 1.

Select RTD or TC calibration

When performing RTD calibration, all eight points must be configured as RTD. The same is true when performing thermocouple calibration. All eight points must be configured as thermocouple.

Continued on next page

Calibration procedure

To calibrate, perform the following steps.

Step	Action
1	Each LLAI IOP card and FTA has been calibrated at the factory for all input types. If recalibration must be performed in the field, power must be applied to the LLAI for at least 30 minutes for temperature stabilization before starting the calibration. The calibration procedure calibrates all channels on one FTA simultaneously, rather than each channel singularly. Have the operator place the IOP card in an Idle state using the HPM Detail Status display.
2	If the FTA has screw terminal strips, temporarily remove the plastic cover. Remove the field wiring from the FTA and substitute "zero input" sources for all channels. These inputs are simply short copper wire jumpers across the input terminals. Refer to Figure 7-1 or Figure 7-2 as appropriate. Notice the difference between Channel 1 and Channels 2 through 8. See Figure 7-1.

Figure 7-1 Zero Calibration Circuit – TC and All Linear Zero Circuits

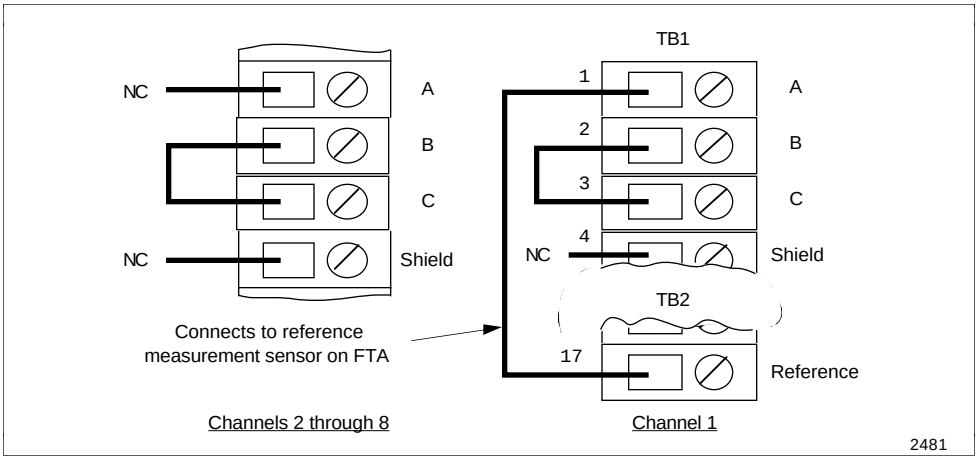
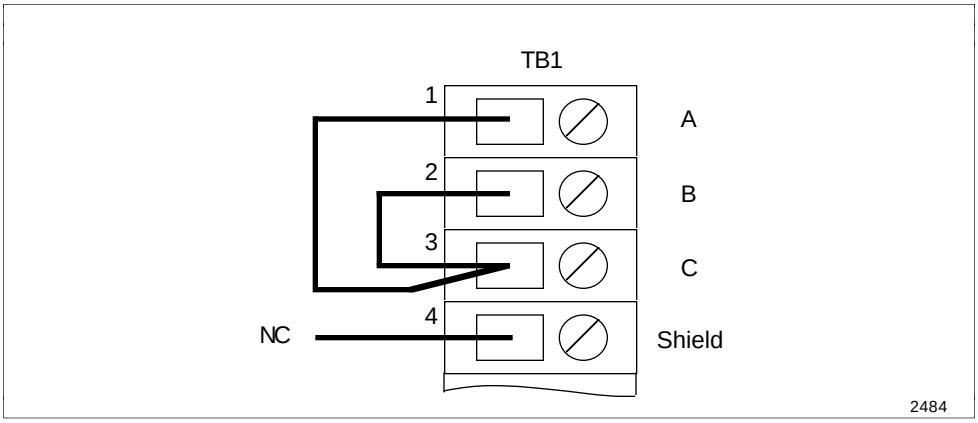


Figure 7-2 Zero Calibration Circuit – RTD Zero
Cu: 10 Ohm, Pt: 100 Ohm, Ni: 120 Ohm

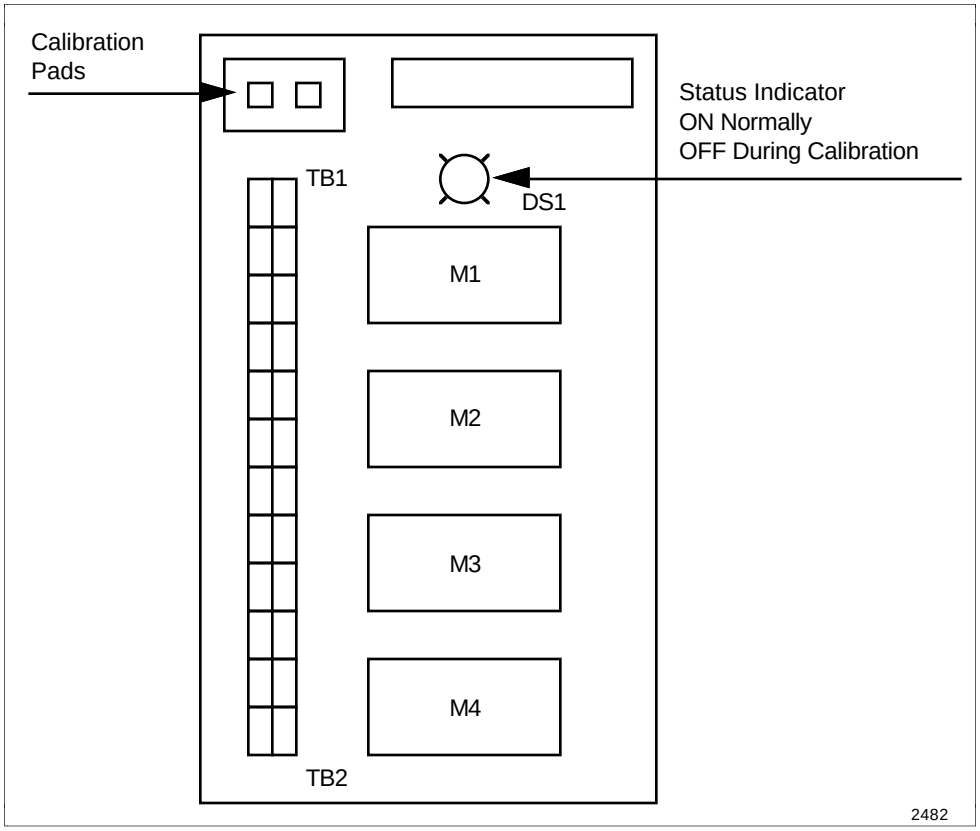


Continued on next page

Calibration procedure, continued

Step	Action
3	Select the **ENABLE CALIBRATION** (or **ENABLE RJ CALIBRATION** if an RJ calibration is being performed) target on the Detail Status display for the LLAI. The **ENABLE CALIBRATION** target changes to the **DISABLE CALIBRATION** target.
4	Momentarily short the two square calibrate pads in the upper-left corner of the FTA under test, as shown in Figure 7-3. Now check the **STATUS** indicator (DS1) on the associated LLAI FTA. You will find it extinguishes immediately, then comes back on in approximately 30 seconds. During this time, the IOP card has performed its "zero input" calibration.

Figure 7-3 LLAI FTA Showing DS1 Status Indicator and Calibration Pads

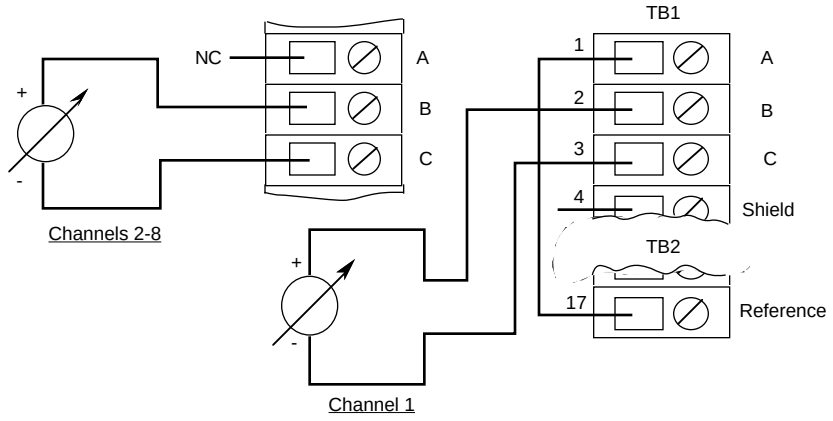


Continued on next page

Calibration procedure, continued

Step	Action
5	Now remove the "zero inputs" and replace them with full-scale signals. Refer to Figure 7-4 or Figure 7-5 for the full scale input value and the connection to the screw or compression terminals.

Figure 7-4 Full Scale Calibration Circuit – TC and All Linear Full Scale Circuits



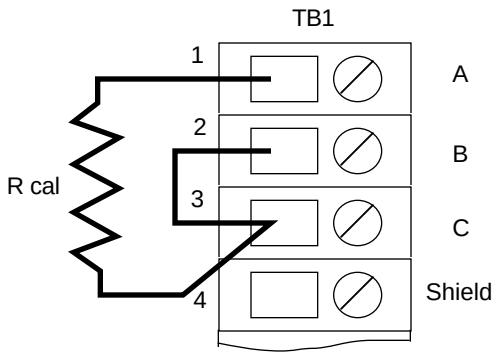
User Input Device	Full-Scale Calibration Values	
	Normal Range	Extended Range
Input Voltage: 0-100 mVdc	100 mV	N/A
0-5 volt	5 V	N/A
Current Input: 4-20 mA	20 mA (5 V)	N/A
10-50 mA	50 mA (5 V)	N/A
Themocouple: ANSI J	40 mV	100 mV
ANSI K	40 mV	40 mV
ANSI E	40 mV	100 mV
ANSI T	40 mV	40 mV
ANSI B	20 mV	20 mV
ANSI S	20 mV	20 mV
ANSI R	20 mV	20 mV
Japanese Type R	20 mV	20 mV

2483

Continued on next page

Calibration procedure, continued

Figure 7-5 Full Scale Calibration Circuit – RTD Full Scale Cu: 10 Ohm, Pt: 100 Ohm, Ni: 120 Ohm



Note:

Be sure there is one wire connected to the "A" terminal, and one wire connected to the "B" terminal. There should be two wires connected to the "C" terminal.

RTD Input Type	Precision Resistor (R cal) Value
Cu: 10 Ohm	100 Ohm
Pt: 100 Ohm	500 Ohm
Ni: 120 Ohm	500 Ohm

2485

Step	Action
6	Again, momentarily short the calibration pads at the upper-left corner of the FTA under test, then check the **STATUS** indicator (DS1) on the LLAI. The **STATUS** indicator remains extinguished for approximately 30 seconds while the IOP card performs its "full-scale" calibration.
7	If a thermocouple input is connected to the LLAI subsystem, it is recommended that you recalibrate the Reference Junction (RJ) input each time the thermocouple is recalibrated. Only channel 1 requires a zero ohm jumper connected to it. Connect a zero-ohm jumper to channel 1 as illustrated in Figure 7-6. Repeat steps 3 and 4. Connect a 2 kohm resistor jumper to channel 1 as illustrated in Figure 7-7. Repeat step 6.

Continued on next page

Calibration procedure, continued

Figure 7-6 RJ Calibration Circuit – RJ Zero

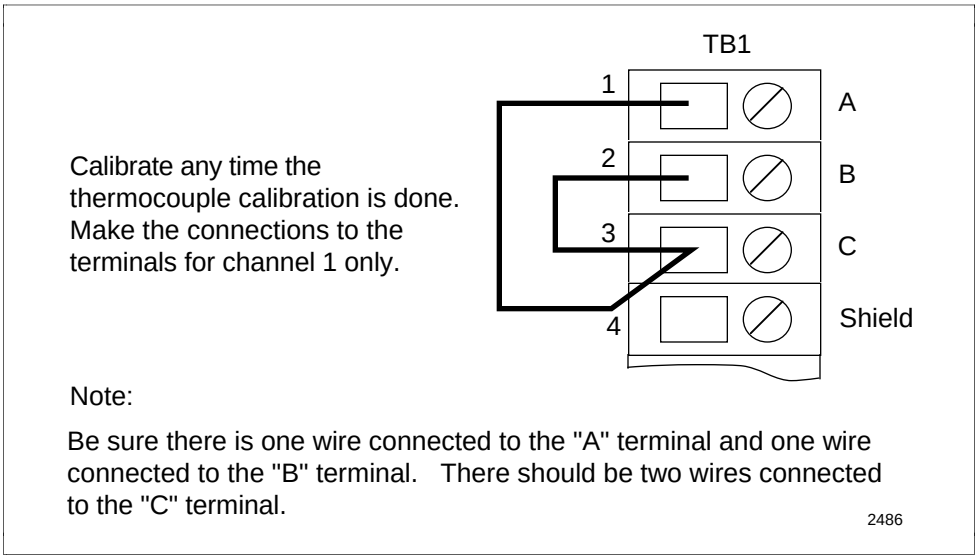
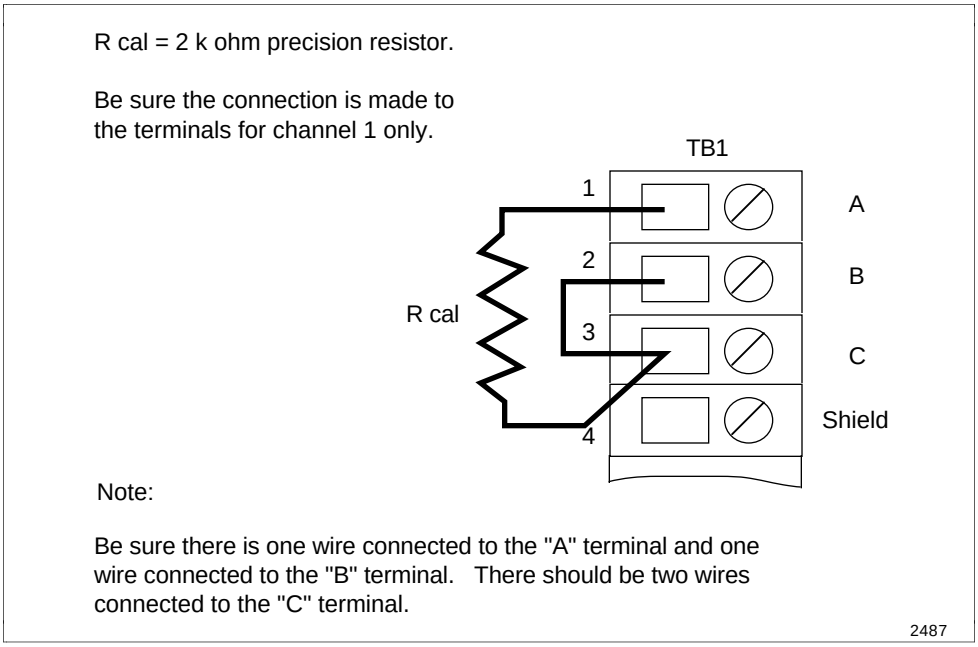


Figure 7-7 RJ Calibration Circuit – RJ Full Scale

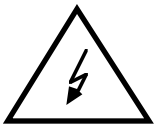


Continued on next page

Calibration procedure, continued

Step	Action
8	Ensure that the calibration target on the LLAI Detail Status display has changed back to **ENABLE CALIBRATION**, indicating that the zero and span calibration process has completed.
9	Check the LLAI IOP card for Soft failures. If a Soft failure occurred, find the source of the failure, correct it, and repeat the calibration procedure. If none occurred, remove the test equipment from the FTA and reconnect the field wiring. If the FTA has screw terminal strips, replace the plastic cover over the strips.
10	Inform the operator that the LLAI subsystem can be returned to on-line operation.

7.2.4 Nonredundant HLAI IOP Calibration Procedure



CAUTION, RISK OF ELECTRIC SHOCK

Introduction

The following calibration procedure is written for the nonredundant model MU-TAIH02 or MU-TAIH03 HLAI FTA, but the procedure can also be used for the redundant model MU-TAIH12, MU-TAIH13, MU-TAIH22, MU-TAIH23, MU-TAIH52, MU-TAIH53, MU-TAIH62, MU-GAIH12/82, MU-GAIH13/83, MU-GAIH14/84, and MU-GAIH22/92 FTAs. See subsection 7.2.5.

Galvanic isolation FTA connection points

The connection points for the calibration voltage source and the shorting location that starts the calibration differs for the model MU-GAIH12/82, MU-GAIH13/83, and MU-GAIH14/84 Galvanically Isolated FTAs. Because of circuit density on the FTA board assembly, IOP calibration terminals, similar to those on a standard FTA, could not be added to the assembly. Instead, unused pins in the FTA's 50-pin auxiliary connector, J19, provide a calibration interface for the Galvanic Isolation HLAI Calibration tool, Honeywell part number 51201450-100. Table 7-2 lists the voltage input pins and calibration start pins.

Table 7-2 Galvanically Isolated HLAI Calibration Connector Pins

Description	Pins
Primary IOP Voltage Source	19 (+) and 44 (-)
Secondary IOP Voltage Source	20 (+) and 45 (-)
Calibration Start (Short together)	21 and 46

Calibration terminals

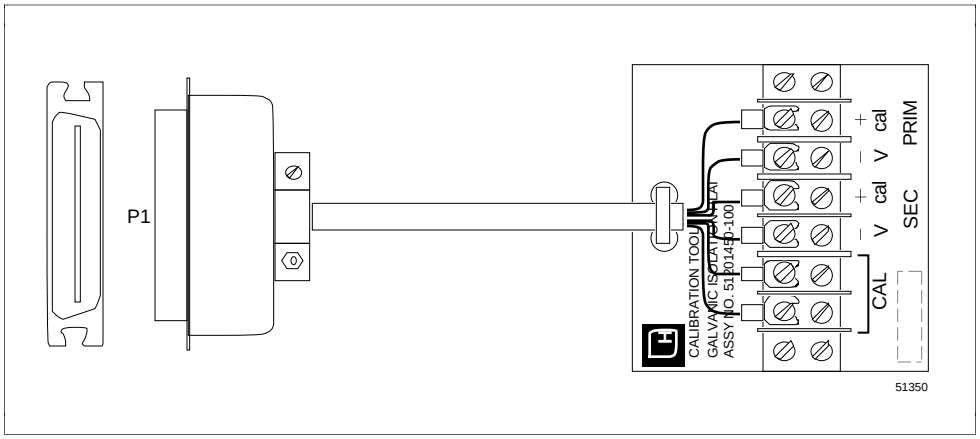
The signals required for calibration of the HLAI IOP are provided at the screw terminals at the end of the tool's cable when the cable is connected to the auxiliary connector on the HLAI FTA. The calibration procedure is the same procedure used for the standard HLAI FTA.

Continued on next page

Galvanic Isolation HLAI Calibration Tool

Figure 7-8 is an illustration of the Galvanic Isolation HLAI Calibration tool.

Figure 7-8 Galvanic Isolation HLAI Calibration Tool (51201450)



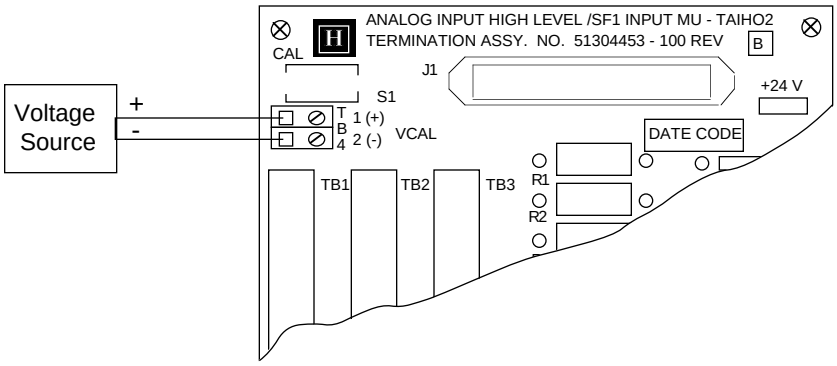
Calibration procedure

Use the following procedure to calibrate a nonredundant HLAI IOP.

Step	Action
1	Have the operator ensure that the IOP card is placed into the Idle state through the HPM Detail Status display. This calibration procedure calibrates all channels simultaneously, rather than each channel singularly.
2	Select the **ENABLE CALIBRATION** target on the Detail Status display for this HLAI. The **ENABLE CALIBRATION** target changes to the **DISABLE CALIBRATION** target.
3	If the voltage source is connected before idling the IOP and enabling calibration, the HLAI will report a Soft failure. Connect the calibration voltage source to the FTA and adjust the voltage to 5 Vdc (4.9995 – 5.0005 Vdc). See Figure 7-9 for the assembly layout of the nonredundant model MU-TAIH02 FTA. The assembly layout of the redundant model MU-TAIH12 FTA is illustrated in Figure 7-10. The assembly layouts of all the HLAI FTAs are illustrated in the *Process Manager I/O Installation* manual.

Continued on next page

Figure 7-9 Nonredundant HLAI Calibration Connections



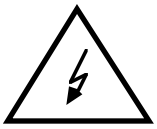
User Input Device		VCAL Voltage Source
Voltage Input:	0-5 volt	5 V
	1-5 volt	5 V
Current Input:	4-20 mA	5 V
	10-50 mA	5 V

6355

Calibration procedure, continued

Step	Action
4	Short the two calibration pads at the upper-left corner of the HLAI FTA as shown in Figure 7-8 to start the calibration. For the Galvanically Isolated FTAs, two pins in the Marshalling Panel connector are shorted together.
5	Ensure that the calibration target on the HLAI Detail Status display has changed back to **ENABLE CALIBRATION**, indicating that the zero and span calibration process has completed. Check for the Soft failure **CALIB ABORT**, which indicates bad calibration.
6	Disconnect the calibration voltage source wiring.
7	Inform the operator that the HLAI can be returned to on-line operation.

7.2.5 Redundant HLAI IOP Calibration Procedure



CAUTION, RISK OF ELECTRIC SHOCK

Simultaneous IOP calibration

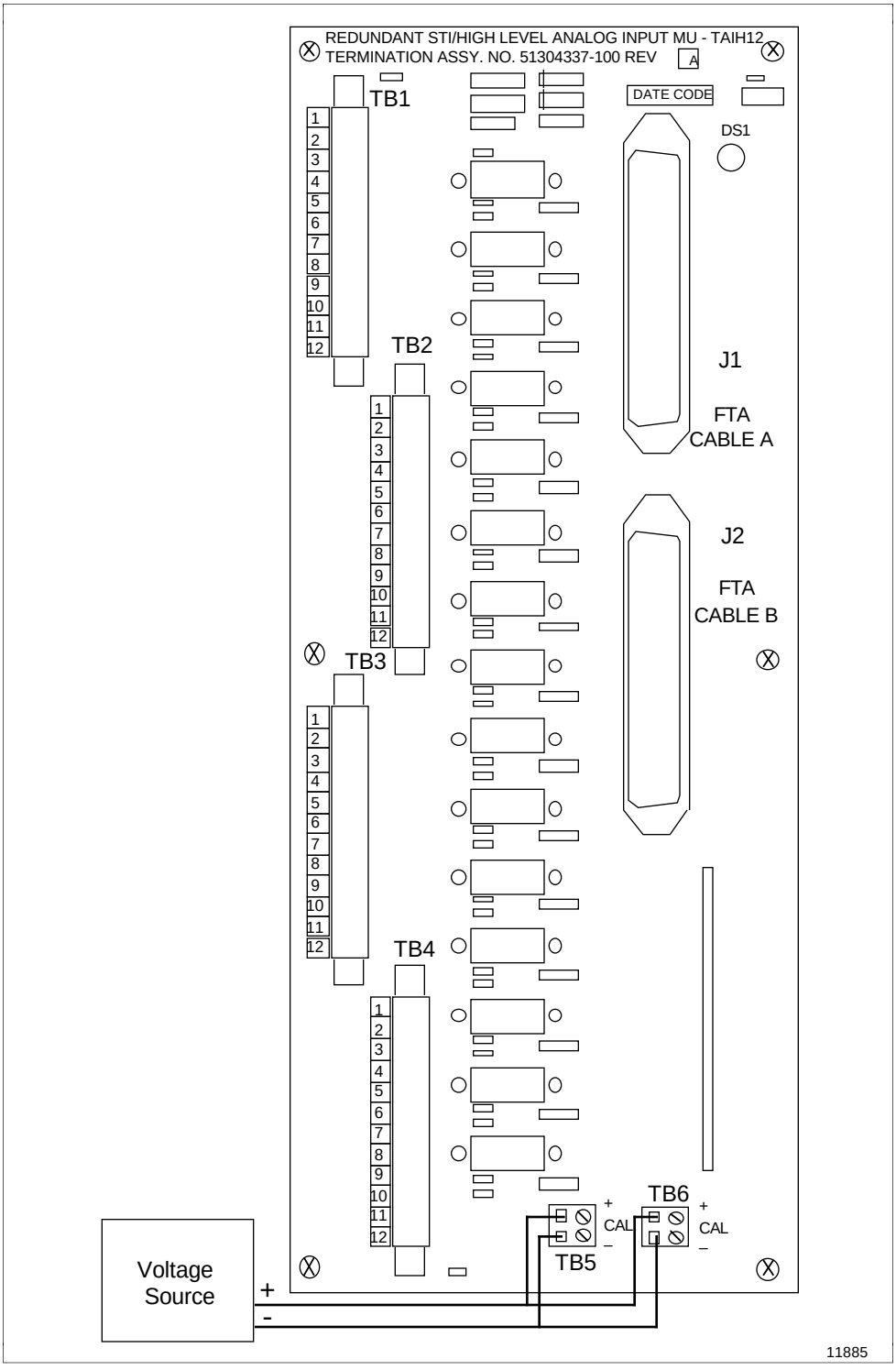
Recalibrate each HLAI IOP separately in an off-line HPM or follow the nonredundant High Level Analog Input FTA calibration procedure in subsection 7.2.4 to simultaneously calibrate both IOPs. The calibration voltage source must be connected to both sets of calibration terminals on the redundant model FTA simultaneously with parallel wiring as shown in Figure 7-10 for the model MU-TAIH12 FTA. Refer to the *Process Manager I/O Installation* manual for the assembly layout and calibration terminal locations for all the HLAI FTA models.

Continued on next page

Calibration connections

Figure 7-10 is an illustration of the redundant HLAI FTA connections necessary to calibrate an HLAI IOP.

Figure 7-10 Redundant HLAI Calibration Connections



7.2.6 Nonredundant AO IOP Calibration Procedure

Calibration procedure

This calibration procedure is written with the nonredundant model MU-TAOX02 as an example, but the procedure can also be used for the nonredundant model MU-GAOX02, and MU-GAOX72 FTAs, and the redundant model MU-TAOX12, MU-TAOX52, MU-GAOX12, and MU-GAOX82 FTAs. Perform the following steps.

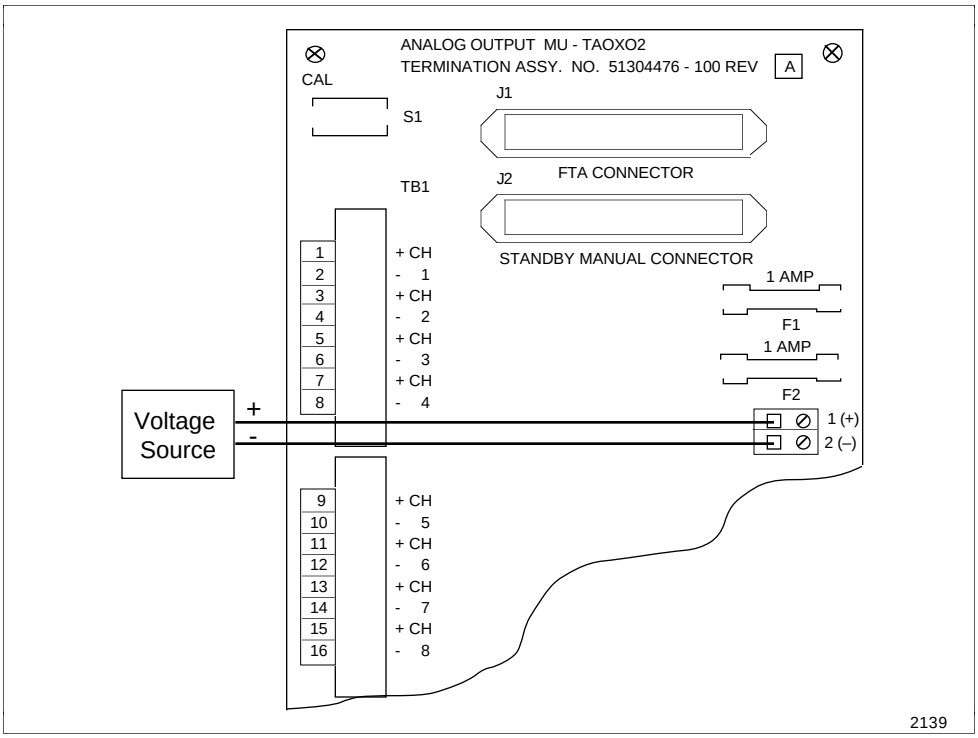
Step	Action
1	Isolate the AO IOP outputs. Use an Analog Standby Manual device discussed in Section 7 in this manual to control the devices connected to the FTA. The Analog Standby Manual device provides isolation from the IOP outputs.
2	Have the operator ensure that the AO IOP card is placed in the Idle state using the HPM Status display.
3	Isolate the AO IOP outputs. Use an Analog Standby Manual device discussed in Section 7 in this manual to control the devices connected to the FTA. The Analog Standby Manual device provides isolation from the IOP outputs.
4	Have the operator select the **ENABLE CALIBRATION** target on the IOP Detail Status display. The target label changes to **DISABLE CALIBRATION**, indicating that the Start Calibration signal from the FTA will be accepted.
5	Connect an adjustable floating voltage source to the FTA output terminals as shown in Figure 7-11 for the nonredundant model MU-TAOX02 FTA, and adjust the source to between 4.9995 and 5.0005 Vdc. The layouts of the redundant model MU-TAOX12 and MU-TAOX52 FTAs are illustrated in the *Process Manager I/O Installation* manual, while the layout of the model MU-GAOX02 and MU-GAOX72 FTAs are also illustrated in the manual. The AO IOP uses this precision voltage reference to do a very accurate short term calibration of the internal loopback ADC. The circuitry is then used to calibrate each output channel.
6	Short together the calibration pads at the upper-left corner of the FTA. The procedure takes approximately 5 seconds. See Figure 7-10. The **DISABLE CALIBRATION** target changes to **ENABLE CALIBRATION** when the procedure is complete.
7	Disconnect the calibration source.
8	Inform the operator that the AO IOP can be placed in control.

Continued on next page

Calibration procedure, continued

Figure 7-11 is an illustration of the redundant Analog Output FTA connections necessary to calibrate an Analog Output IOP.

Figure 7-11 Nonredundant AO Calibration FTA Connections



7.2.7 Redundant AO IOP Calibration Procedure

Simultaneous IOP calibration

Follow the Analog Output FTA calibration procedure in subsection 7.2.6 to simultaneously calibrate both IOPs. The calibration voltage source must be connected to both sets of calibration terminals on the redundant model FTA simultaneously with parallel wiring as shown in Figure 7-12. Refer to *Process Manager I/O Installation* manual for the assembly layout and calibration terminal locations for the model MU-TAOX12, MU-TAOX52, MU-GAOX12, or MU-GAOX82 FTAs.

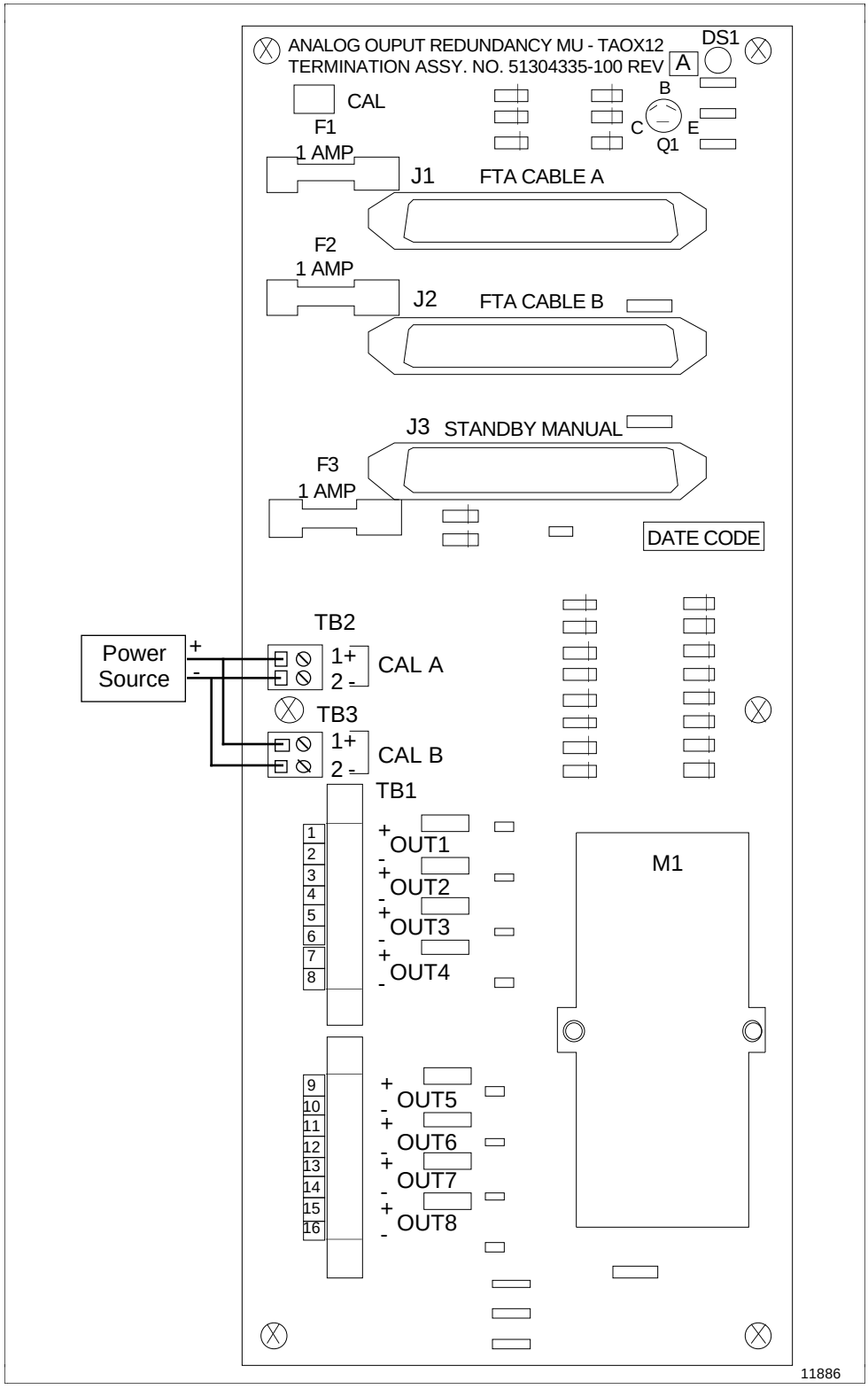
Continued on next page

7.2.7 Redundant AO IOP Calibration Procedure, Continued

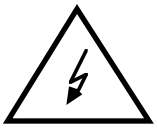
Calibration connections

Figure 7-12 is an illustration of the redundant Analog Output FTA connections necessary to calibrate an Analog Output IOP.

Figure 7-12 Redundant Analog Output Calibration Connections



7.2.8 LLMux IOP Calibration Procedure



CAUTION, RISK OF ELECTRIC SHOCK

Introduction

The LLMux FTA daughter board can only be calibrated when it is mounted on a Thermocouple (TC) FTA. After calibration, the daughter board can be moved to any LLMux FTA and maintain the calibration. However, a TC daughter board is not interchangeable with an RTD daughter board.

Calibration procedure

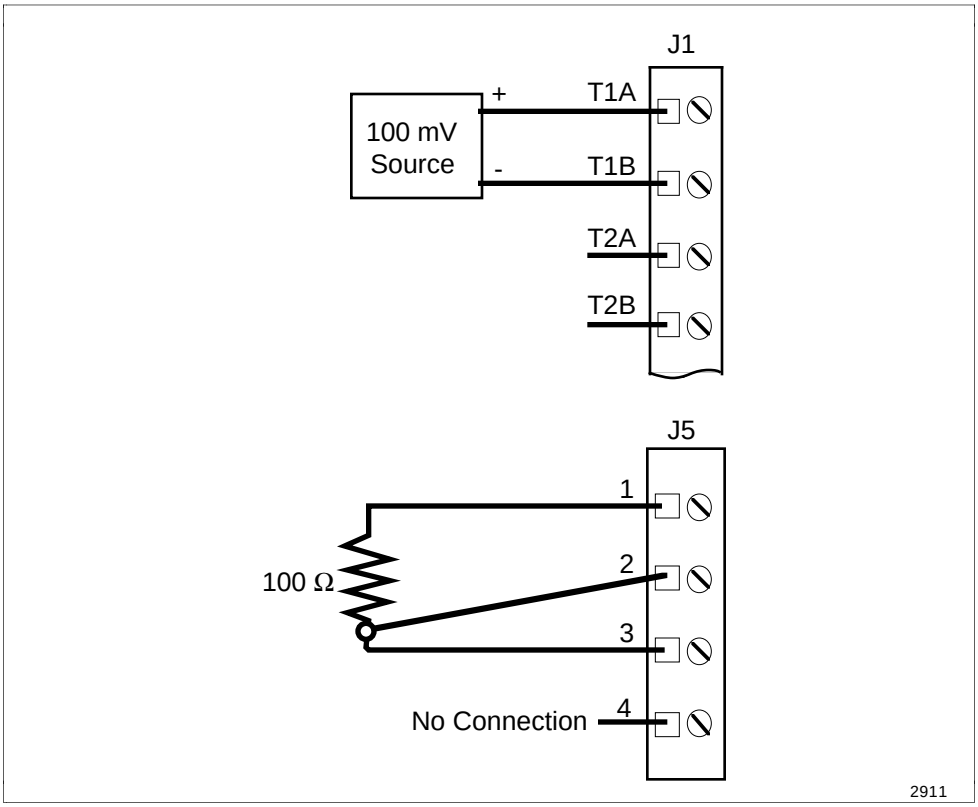
Use the following procedure to calibrate an LLMux FTA.

Step	Action
1	Connect a precision voltage source to point zero, terminals T1A and T1B of terminal strip J1 as shown in Figure 7-13, and set the voltage to 100 millivolts (99.995 - 100.005 millivolts).
2	Remove the two jumpers, JRA and JRB, located between J2 and J3.
3	Connect the precision resistor (three lead 100 ohm ± .005 ohm) to the remote CJR terminals, J5. Apply power for 5 minutes.
4	Calibration is initiated by a single command for each FTA. Have the operator put the IOP in the Idle state and then select the **CALIBRATION** target. The calibration procedure is automatic and completes in less than one second.
5	Remove the voltage source. Disconnect the precision resistor from J5 and reconnect the jumpers removed from JRA and JRB in step 2.

Continued on next page

LLMux FTA calibration connections

Figure 7-13 LLMux FTA Calibration Connections



7.3 Thermocouple Input Accuracy Verification

Introduction

It is necessary to verify the accuracy of a thermocouple input. Verification is accomplished with the use of a precision Thermocouple Simulator, the instrument's operating procedure, and the procedure steps that follow.

Accuracy verification procedure

Perform the following steps to verify the accuracy of the thermocouple.

Step	Action
1	Be sure the equipment is properly installed in the cabinet.
2	Connect a reference grade thermocouple wire between the Thermocouple Simulator and one input of the process control system.
3	Install all equipment covers and close the cabinet doors.
4	Using the HPM Detail Status display at the Universal Station, disable the Open Thermocouple Detection mode for the control point.
5	Allow the equipment to operate normally for 2 hours while temperature gradients stabilize.
6	Verify the accuracy of the thermocouple using the Thermocouple Simulator and following its operating procedure.
7	Move the thermocouple reference wire to another thermocouple input from the process control system and repeat the above procedures, starting at step 3.

Section 8 – Periodic Redundancy Tests

8.1 Overview

Section contents

The topics covered in this section are:

	Topic	See Page
8.1	Overview	401
8.2	HPMM Redundancy	402
8.3	IOP Redundancy	403
8.3.1	Redundant 8-Channel Analog Output IOPs	405
8.4	Power Cable Redundancy	407
8.5	Power Supply Module Redundancy	408

Introduction

This section describes the recommended periodic verification of the equipment's redundancy where applicable.

At an appropriate time, such as during a annual period of scheduled plant maintenance, the High-Performance Process Manager subsystem's availability can be improved by performing specific tests on various hardware parts of the High-Performance Process Manager subsystem. During the tests, personnel should be prepared for either proper operation or improper operation of the hardware. The preparation for improper operation of the hardware during the tests yields the lowest Mean Time to Repair (MTR), which is important when maximizing subsystem availability.

Even though fault coverage is high in the High-Performance Process Manager (HPM) during normal operation, periodic redundancy testing provides additional fault coverage by exercising any hardware that is not in use during normal operation.

8.2 HPMM Redundancy

Introduction

The ability of redundant HPMMs to swap positions, primary to secondary and secondary to primary, can be confirmed by using display commands on the Universal Station.

HPMM swap verification

Perform the following steps to verify that redundant HPMMs will swap their primary and secondary positions.

Step	Action
1	Select the **<SYST STATS>** (SYSTEM STATUS) key on the console and then select the **PROCESS NETWORK STATUS** target on the display for the network that contains the High-Performance Process Manager of interest. The UCN Status display is produced on the console screen.
2	Choose the status box containing the High-Performance Process Manager of interest and then select the **DETAIL STATUS** target on the UCN Status display. The HPM Detail Status display is produced on the screen.
3	Select the **RUN STATES** target on the HPM Detail Status display. The **SWAP PRIMARY** target along with other targets appear at the bottom of the display.
4	Select the **SWAP PRIMARY** target. This produces the **ENTER** and **CANCEL** targets to the right of the **SWAP PRIMARY** target.
5	Note the status of the two HPMMs status boxes on the display and then choose one. One status box should contain an "**OK**" label and the other status box should contain a "**BACKUP**" label. Choose one of these status boxes. Then, select the **ENTER** target. The "**OK**" and "**BACKUP**" labels in the HPMM status boxes should switch positions in 45 seconds or less, depending on the network size, and indicate the HPMM redundancy is functional. In addition, the Alphanumeric display on the High-Performance Comm/Control card will also confirm to swap by switching the primary and secondary indications appropriately. The orientation of the HPMMs can be returned to their original positions by selecting the **ENTER** target a second time.

8.3 IOP Redundancy

Introduction

The ability of a redundant pair of IOPs to swap positions, primary to secondary and secondary to primary, is confirmed by using display commands on the Universal Station.

IOP redundancy terminology

IOP A	IOP A is the physical primary IOP. It is the IOP that is physically connected by cable to the "A" cable connector on a redundant FTA.
IOP B	IOP B is the physical primary IOP. It is the IOP that is physically connected by cable to the "B" cable connector on a redundant FTA.
Primary IOP	IOP B is the physical primary IOP. It is the IOP that is physically connected by cable to the "B" cable connector on a redundant FTA.
Secondary IOP	The secondary IOP is the logical secondary IOP. It can be either IOP A or IOP B that is not controlling the FTA's field terminals or providing the process variable.
IOP Swap	An IOP swap reverses the status of the physical IOPs, A and B. The present primary IOP becomes the secondary IOP, and the present secondary IOP becomes the primary IOP.
IOP Bias	For the 8-channel Analog Output IOP only, operation with the IOP A as the primary IOP and IOP B as the secondary IOP is with the basis, the preferred condition. Operation with the IOP B as the primary IOP and IOP A as the secondary IOP is against the basis, the nonpreferred condition.

Continued on next page

IOP redundancy test procedure

Perform the following steps for each redundant IOP configuration.

Step	Action
1	Select the **<SYST STATS>** (SYSTEM STATUS) key on the console and then select the **PROCESS NETWORK STATUS** target on the display for the network that contains the High-Performance Process Manager (HPM) or Process Manager (PM) of interest. The UCN Status display is produced on the console screen.
2	Choose the status box containing the HPM of interest and then select the **DETAIL STATUS** target on the UCN Status display. The HPM Detail Status display is produced on the screen.
3	Select the **RUN STATES** target on the HPM Detail Status display. The **SWAP PRIMARY** target along with other targets appear at the bottom of the display.
4	Select the **SWAP PRIMARY** target. This produces the **ENTER** and **CANCEL** targets to the right of the **SWAP PRIMARY** target.
5	Note the status in the IOP status box on the display for the redundant pair of IOPs of interest. The status box should contain an "**OK/BKP**" label. Choose the IOP status box of interest. Then, select the **ENTER** target. The "**OK/BKP**" label in the IOP status box should switch to "**BKP/OK**," respectively after approximately 5 seconds, indicating the IOP redundancy is functional. The orientation of the redundant IOPs should be returned to their original positions by selecting the **ENTER** target a second time.
6	Repeat step 5 for any other redundant pairs of IOPs.

8.3.1 Redundant 8-Channel Analog Output IOPs

Introduction

Redundancy for the 8-channel Analog Output IOPs is biased toward the IOP A to maximize reliability. Hardware bias is preferred because IOP B (the physical secondary) is connected to the Analog Output FTA through a switching module on the FTA, while IOP A (the physical primary) is connected directly to the FTA circuitry that interfaces the FTA's field wiring output terminals. Use of the procedure in this subsection tests a redundant pair of Analog Output IOPs for proper operation.

Hardware identification

Locate the following components.

- Analog Output IOP A
- Analog Output IOP B
- The redundant Analog Output FTA
- An Analog Output Standby Manual device
- Devices that are being controlled by the analog output of the FTA
- Control algorithms that are driving the analog outputs

Status check

Using the IOP Detail Status display, check that the IOPs are currently operating normally, as indicated by a status of **OK/BKP**. In addition, be sure the following is true.

- The outputs are being controlled by IOP A
- IOP A and IOP B are synchronized
- IOP A is operating normally without Soft failures
- IOP B is operating normally without Soft failures

Continued on next page

Test procedure

Perform the following steps to test for proper IOP redundancy operation.

Step	Action
1	Begin the test at a convenient time. Disrupt power to IOP B by toggling the IOP's upper extractor. The IOP Detail Status display should indicate a status of **OK/NR [S]** briefly, and then return to a status of **OK/BKP** for the IOPs. Confirm that the field devices are operating properly by observing the operation of the process, or measure the output currents reaching the devices.
2	Disconnect the cable to IOP B. The IOP Detail Status display should indicate a status of **OK/BSF** for the IOPs. Confirm that the field devices are operating properly by observing the operation of the process, or measure the output currents reaching the devices.
3	Reconnect the cable to IOP B. The IOP Detail Status display should return to an **OK/BKP** status for the IOPs.
4	Execute a swap so that IOP B has control of the FTAs outputs. The IOP Detail Status display should indicate a **BKP/OK** status for the IOPs. Check that the IOP Detail Status display continues to indicate **BKP/OK** status for a period of at least two minutes to allow the Redundancy Diagnostics to complete with IOP B now controlling the FTA outputs. Confirm that the output devices are operating properly by observing the operation of the process, or measuring the output currents reaching the field devices before and after executing the swap command.
5	Disrupt power to IOP A by toggling the IOP's upper extractor. The IOP Detail Status display should indicate a **[S] NR/OK** status briefly, then return to **BKP/OK**. Confirm that the output devices are operating properly by observing the operation of the process, or measuring the output currents reaching the field devices.
6	Disconnect IOP A's FTA cable. The IOP Detail Status display should indicate a status of **BSF/OK** for the IOPs. Confirm that the output devices are operating properly by observing the operation of the process, or measuring the output currents to the field devices.
7	Connect IOP A's FTA cable. The IOP Detail Status display should return to a **BKP/OK** status for the IOPs.
8	Allow the subsystem to operate against the bias with IOP B controlling the outputs for a period of time, such as 4 hours. During this period of time, the IOP Detail Status display should continue to indicate a **BKP/OK** status for the IOPs. Ensure that no Soft failures are logged into the System Status Real Time Journal. Continue to monitor that the output devices are operating properly by observing the operation of the process, or measuring the output currents reaching the field devices
9	Execute a swap command so that IOP A has control of the FTAs outputs. The IOP Detail Status display should indicate an **OK/BKP** status for the IOPs. Continue to monitor operation of the output devices with the bias for a period of time, such as 2 hours.

8.4 Power Cable Redundancy

Introduction

Card files, the Digital Input Power Distribution assembly, and the Galvanic Isolation Power Distribution assembly are provided with redundant power cables to enhance power distribution reliability within the High-Performance Process Manager. You should be able to disconnect either end of one of the two power cables providing power to the card file, Digital Input Power Distribution assembly, or Galvanic Isolation Power Distribution assembly without affecting equipment operation.

CAUTION

CAUTION—Power cable redundancy testing should be performed during a plant shutdown.

Test procedure

Perform the following steps for each card file, Digital Input Power Distribution assembly, and Galvanic Isolation Power Distribution assembly.

Step	Action
1	Disconnect one of the pair of power cables for a card file, Digital Input Power Distribution assembly, or Galvanic Isolation Power Distribution assembly at either the Power System connection or the other end of the cable. Determine if the operation of the equipment is impaired by observing the operation of the affected IOPs and/or HPMM cards.
2	Replace the cable connection and then disconnect the other cable in the pair. Determine if the operation of the equipment is impaired.
3	Repeat steps 1 and 2 for all card files, Digital Input Power Distribution assemblies, and Galvanic Isolation Power Distribution assemblies.

8.5 Power Supply Module Redundancy

Introduction

A Power System with redundant Power Supply Modules should continue to provide power to the High-Performance Process Manager without interruption when one of the Power Supply Modules fails or looses ac power.

CAUTION

CAUTION—Power cable redundancy testing should be performed during a plant shutdown.

Test procedure

Perform the following steps to test the Power System's redundancy power capability.

Step	Action
1	With the both Power Supply Modules of a redundant Power System operating, place the **ON/OFF** switch of the right Power Supply Module in the **OFF** position. Observe that the HPMM and IOP cards continue to operate normally (their **Status** and **Power** indicators are illuminated). Return the **ON/OFF** switch to the **ON** position if operation continues normally. Should the HPMM and IOP cards not continue to operate normally, follow the troubleshooting and replacement procedures for the Power Supply Module in Sections 4 and 7, respectively.
2	With both Power Supply Modules of a redundant Power System operating, place the **ON/OFF** switch of the left Power Supply Module in the **OFF** position. Observe that the HPMM and IOP cards continue to operate normally. Return the **ON/OFF** switch to the **ON** position if operation continues normally. Should the HPMM and IOP cards not continue to operate normally, follow the troubleshooting and replacement procedures for the Power Supply Module in Sections 4 and 7, respectively. When the left Power Supply Module's **ON/OFF** switch is placed in the **OFF** position, all Low Level Analog Input IOPs should report a Soft failure at the Universal Station, but they will continue to operate normally.

Section 9 – Spare Parts

9.1 Overview

Section contents

The topics covered in this section are:

	Topic	See Page
9.1	Overview	409
9.2	Periodic Maintenance Parts	410
9.3	Optimum Replaceable Unit (ORU) Parts	413
9.4	UCN Parts	434

Introduction

The parts listed in the following tables are periodic maintenance items and Optimum Replaceable Units (ORU) for the High-Performance Process Manager (HPM). All the listed parts reference the Honeywell part number. For additional or optional equipment part numbers not listed, contact your Honeywell Sales Representative.

9.2 Periodic Maintenance Parts

Periodic maintenance parts list

Table 9-1 lists items that may be required during the life of the High-Performance Process Manager.

Table 9-1 HPM Periodic Maintenance Parts

Name	Description		Part Number
BATTERIES			
NiCad Rechargeable Batteries	Set of 3 AA-size NiCad batteries Set of 3 C-size NiCad batteries		51190422-100 51192060-100
Alkaline Batteries	Set of 3 AA-size Alkaline batteries		51190467-100
FUSES			
Assembly	Quantity	Description	
Left 7-Slot Card File (51401626)	8	2.0 A Subminiature fuse (F1-8)	30754661-021
Right 7-Slot Card File (51401629)	8	2.0 A Subminiature fuse (F1-8)	30754661-021
15-Slot Card File (51401629)	16	2.0 A Subminiature fuse (F1-16)	30754661-021
IOP Card File (51402599)	15 1	2.0 A Subminiature fuse (F1-15) 0.5 A Subminiature fuse (F16)	30754661-021 30754661-014
3-30 Vdc SS DO FTA (51304423)	16	5.0 A Time-delay fuse 5 x 20 mm	51190584-250
3-30 Vdc SS DO FTA (51304650)	16	2.5 A Time-delay fuse 5 x 20 mm	51190584-225
31-200 Vdc SS DO FTA (51304428)	16	1.0 A Time-delay fuse 5 x 20 mm	51190584-210
24-240 Vac SS DO FTA (51304408)	16	3.0 A Time-delay fuse 5 x 20 mm	51190584-230
120-240 Vac SS DO FTA (51304648)	16	2.5 A Time-delay fuse 5 x 20 mm	51190584-225
120 Vac Relay DO FTA (51304443)	16	6.0 A Time-delay fuse 5 x 20 mm	51190584-260
240 Vac Relay DO FTA (51304427)	16	3.0 A Time-delay fuse 5 x 20 mm	51190584-230
24 Vdc Nonisolated DO FTA (51304446)	16 1	0.2 A Fast-action fuse 5 x 20 mm (F1-16) 2.0 A Fast-action fuse 5 x 20 mm (F17)	51190582-120 51190582-220

Continued on next page

Periodic maintenance parts list, continued

Table 9-1 HPM Periodic Maintenance Parts, Continued

Name	Description		Part Number
FUSES, continued			
Assembly	Quantity	Description	
24 Vdc Isolated DO FTA (80364013)	4	1.6 A Fast-action fuse MP16 (F1-4)	83957061-004
24 Vdc Isolated DO FTA (80366183)	16	1.6 A Fast-action fuse MP16 (F1-16)	83957061-004
LLAI FTA (51304437)	4	0.5 A Subminiature fuse (F1-4)	30754661-014
DI FTA (80364010, 80366180)	2	0.5 A Fast-action fuse MP05 (F1, F3)	83957061-002
DI FTA (80364010, 80366180)	1	1.0 A Fast-action fuse MP10 (F2)	83957061-003
DI Power Distribution Assy (51304425)	12	1.0 A Fast-action fuse 5 x 20 mm (F1-12)	51190582-210
SI/SDI FTA (51303932)	2	0.25 A Subminiature fuse (F1-2)	30754661-011
Nonredundant AO FTA (51304476)	2	1.0 A Fast-action fuse 5 x 20 mm (F1-2)	51190582-210
Redundant AO FTA (51304335)	3	1.0 A Fast-action fuse 5 x 20 mm (F1-3)	51190582-210
Redundant AO FTA (80364007, 80366177, 80366481, 80366484)	1	1.0 A Fast-action fuse MP10 (F1)	83957061-003
Pulse Input FTA (51304084)	8	0.25 A Fast-action fuse 5 x 20 mm (F1-8)	51190582-125
Galvanic AO FTA (51304638)	3	1.0 A Subminiature fuse (F1-3)	30754661-019
H-P I/O Link Card	1	3.0 A Fast-action fuse (F1)	30754661-022
Fuseholder Puller	Fuseholder extractor		51190586-100

Continued on next page

Periodic maintenance parts list, continued

Table 9-1 HPM Periodic Maintenance Parts, Continued

Name	Description	Part Number
FILTERS		
Filter Kit (Rittal cabinet)	Louvered cover and filter, 20 /8 x 20 /8 (cm/in.)	51109488-100
Filter (Rittal cabinet)	Replacement filter only, 20 /8 x 20 /8 (cm/in.)	51109488-200
Filter (Markhon cabinet)	Replacement filter only, 39 /15.5 x 61 /24 (cm/in.)	51109541-100

9.3 Optimum Replaceable Unit (ORU) Parts

ORU parts List

This subsection identifies the assemblies that may be required for maintenance during the life of the High-Performance Process Manager. Maintenance procedures are found in this manual. Additional information can be found in the *High-Performance Process Manager Installation* and *Process Manager I/O Installation* manuals.

Table 9-2 Non-Conformally Coated HPM ORU Parts List

Name	Description		Part Number
CABLES			
Power System Cables (Nonshielded)	Power System to card file		
	MU-KDPR01	1 meter	51201397-001
	MU-KDPR02	1.5 meters	51201397-915
		2 meters	51201397-002
		3 meters	51201397-003
	MU-KDPR04	4 meters	51201397-004
	MU-KDPR05	5 meters	51201397-005
		6 meters	51201397-006
		8 meters	51201397-008
	MU-KDPR10	10 meters	51201397-010
	MU-KDPR15	15 meters	51201397-015
	MU-KDPR20	20 meters	51201397-020
	MU-KDPR25	25 meters	51201397-025
	MU-KDPR30	30 meters	51201397-030
	MU-KDPR35	35 meters	51201397-035
	MU-KDPR40	40 meters	51201397-040
	MU-KDPR45	45 meters	51201397-045
	MU-KDPR50	50 meters	51201397-050
Power System Cables (Shielded – for external cabinet use in Europe))	Power System to Power Distribution Assembly		
	MU-KSPR05	5 meters	51204037-005
	MU-KSPR10	10 meters	51204037-010
	MU-KSPR15	15 meters	51204037-015
	MU-KSPR20	20 meters	51204037-020
	MU-KSPR30	30 meters	51204037-030
	MU-KSPR40	40 meters	51204037-040
	MU-KSPR50	50 meters	51204037-050

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description		Part Number
CABLES, continued			
Galvanic Isolation FTA Power Cable	GI Power Distribution assembly to FTA cable		
		0.50 meter	51109620-020
		0.75 meter	51109620-030
		1.00 meter	51109620-040
		1.25 meters	51109620-050
		2.00 meters	51109620-080
		3.00 meters	51109620-120
		4.00 meters	51109620-160
	MU-KGPR05	5.00 meters	51109620-195
	MU-KGPR10	10.00 meters	51109620-390
Power Adapter External Cable	Power Adapter to FTA cable (External to the cabinet)		
	MU-KLX076	76 meters	51190696-076
	MU-KLX152	152 meters	51190696-152
	MU-KLX305	305 meters	51190696-305
Power Adapter Internal Cable	Power Adapter to FTA cable (Internal to the cabinet)		
	MU-KLAM01	30 centimeters	51304465-100
	MU-KLAM02	66 centimeters	51304465-200
	MU-KLAM03	100 centimeters	51304465-300
	MU-KLAM04	200 centimeters	51304465-400
	MU-KLAM05	300 centimeters	51304465-500
I/O Link Interface Cable (Set of two)	HPMM to IOP card file communication cable		
		Two drop in cabinet	51195479-100
		Three drop in cabinet	51195479-200
		Four drop in cabinet	51195479-300
		Five drop in cabinet	51195479-400
		Six drop in cabinet	51195479-500
I/O Link Interface Cable (Set of two, shielded – for use in Europe)	HPMM to IOP card file communication cable		
		Two drop in cabinet	51204042-100
		Three drop in cabinet	51204042-200
		Four drop in cabinet	51204042-300
		Five drop in cabinet	51204042-400
		Six drop in cabinet	51204042-500

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description		Part Number
CABLES, continued			
HPMM Redundancy Cable	HPMM redundancy interconnect cable (2 m)		51201667-100
IOP to FTA Cable	IOP to FTA cable		
		1 meter	51201420-001
		1.5 meters	51201420-915
	MU-KFTA02	2.0 meters	51201420-002
	MU-KFTA03	3.0 meters	51201420-003
	MU-KFTA04	4.0 meters	51201420-004
	MU-KFTA05	5.0 meters	51201420-005
		6.0 meters	51201420-006
	MU-KFTA08	8.0 meters	51201420-008
	MU-KFTA10	10.0 meters	51201420-010
	MU-KFTA15	15.0 meters	51201420-015
	MU-KFTA20	20.0 meters	51201420-020
	MU-KFTA25	25.0 meters	51201420-025
	MU-KFTA30	30.0 meters	51201420-030
	MU-KFTA35	35.0 meters	51201420-035
	MU-KFTA40	40.0 meters	51201420-040
	MU-KFTA45	45.0 meters	51201420-045
	MU-KFTA50	50.0 meters	51201420-050
IOP to FTA Cable (Shielded – for external cabinet use in Europe)	IOP to FTA cable		
		1 meter	51204033-001
		1.5 meters	51204033-915
	MU-KFTS02	2.0 meters	51204033-002
	MU-KFTS03	3.0 meters	51204033-003
	MU-KFTS04	4.0 meters	51204033-004
	MU-KFTS05	5.0 meters	51204033-005
		6.0 meters	51204033-006
	MU-KFTS08	8.0 meters	51204033-008
	MU-KFTS10	10.0 meters	51204033-010
	MU-KFTS15	15.0 meters	51204033-015
	MU-KFTS20	20.0 meters	51204033-020
	MU-KFTS25	25.0 meters	51204033-025
	MU-KFTS30	30.0 meters	51204033-030
	MU-KFTS35	35.0 meters	51204033-035
	MU-KFTS40	40.0 meters	51204033-040
	MU-KFTS45	45.0 meters	51204033-045
	MU-KFTS50	50.0 meters	51204033-050

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
POWER SYSTEM COMPONENTS		
Power Supply Module	Standard 20 A Power Supply Module	51109456-200
Power Supply Module	AC Only 8 A Power Supply Module	51190465-100
Power Supply Module	AC Only 16 A Power Supply Module	51190465-200
48 V Battery Backup	48 V Battery Pack assembly	51303948-100
Power System Backplane Assy	PM/APM Power System backplane	51401166-100
Power System Backplane Assy	HPM Power System backplane	51404172-100
AC/DC Distribution Assembly	AC Only power control and distribution board 115 Vac dual PSMs	51401135-100
AC/DC Distribution Assembly	AC Only power control and distribution board 115 Vac single PSM	51401135-200
AC/DC Distribution Assembly	AC Only power control and distribution board 230 Vac dual PSMs	51401135-300
AC/DC Distribution Assembly	AC Only power control and distribution board 230 Vac single PSM	51401135-400
CMOS Battery Backup Assembly	PM/APM PS Charger/monitor for CMOS memory	51303968-100
CMOS Battery Backup Assembly	HPM PS Charger/monitor for CMOS memory	51309206-100

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name		Description	Part Number
HPMM CARDS/MODULE			
High-Performance Comm/Control		/Control card	51401635-100
High-Performance I/O Link		I/O Link Interface card	51401642-100
HPM UCN Interface		UCN Interface module	51402573-100
IOP CARDS			
HLAI IOP	(MU-PAIH02)	High Level Analog Input card (Replaced by 51304754-100)	51304489-100
HLAI IOP	(MU-PAIH03)	High Level Analog Input card	51304754-100
LLAI IOP	(MU-PAIL02)	Low Level Analog Input card	51304481-100
LLMux IOP	(MU-PLAM02)	Low Level Multiplexer card	51304362-100
DI IOP	(MU-PDIX02)	Digital Input card	51304485-100
DI IOP	(MU-PDIY22)	Digital Input card	80363972-100
AO IOP	(MU-PAOX02)	Analog Output (Replaced by 51304672-100)	51304483-100
AO IOP	(MU-PAOX03)	Analog Output card	51304672-100
AO IOP	(MU-PAOY22)	Analog Output card	80363969-100
DO IOP	(MU-PDOX02)	Digital Output card	51304487-100
DO IOP	(MU-PDOY22)	Digital Output card	80363975-100
STI IOP	(MU-PSTX02)	Smart Transmitter Interface card (Replaced by 51304516-200)	51304516-100
STIM	(MU-PSTX03)	Smart Transmitter Interface Multivariable	51304516-200
PI IOP	(MU-PPIX02)	Pulse Input card	51304386-100
SDI IOP	(MU-PSDX02)	Serial Device Interface card	51304362-200
SI IOP	(MU-PSIM11)	Serial Interface card	51304362-300
DISOE IOP	(MU-PDIS11)	Digital Input Sequence Of Events card	51304690-100
Slot Filler		Empty IOP slot filler card	51304260-200
I/O LINK EXTENDER COMPONENTS			
Standard I/O Link Extender (MU-IOLM02)		Standard I/O Link Extender card Standard fiber optic Tx/Rx coupler (1) Standard fiber optic Tx/Rx coupler (3)	51304419-100 51201557-100 51201557-300
Long Distance I/O Link Extender (MU-ILDX02 – Replaced by MU-ILDX03)		Long Distance I/O Link Extender card Long Distance fiber optic Tx/Rx coupler (1)	51304532-100 51201616-100
Long Distance I/O Link Extender (MU-ILDX03)		Long Distance I/O Link Extender card Long Distance fiber optic Tx/Rx coupler (1)	51304532-100 51309208-100
I/O Link Extender Adapter Kit (MU-ILES01)		I/O Link Extender Adapter kit	51204043-100

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
STANDARD FTA COMPONENTS		
HLAI/STI FTA (MU-TAIH02)	HLAI/STI with compression terminals	51304453-100
HLAI/STI FTA (MU-TAIH12)	HLAI/STI with compression terminals	51304337-100
HLAI/STI FTA (MU-TAIH22)	HLAI/STI with compression terminals	80366195-100
	AI Adapter Module for the above FTA	80367163-001
HLAI/STI FTA (MU-TAIH52)	HLAI/STI with screw terminals	51304337-200
HLAI/STI FTA (MU-TAIH62)	HLAI/STI with screw terminals	80366192-100
	AI Adapter Module for the above FTA	80360713-001
HLAI FTA (MU-TAIH03)	HLAI with compression terminals	51309136-125
HLAI FTA (MU-TAIH13)	HLAI with compression terminals	51309138-125
HLAI FTA (MU-TAIH23)	HLAI with compression terminals	80369165-125
	AI Adapter Module for the above FTA	80367163-001
HLAI FTA (MU-TAIH53)	HLAI with screw terminals	51309138-225
STI FTA (MU-TSTX03)	STI with compression terminals	51309140-125
STI FTA (MU-TSTX13)	STI with compression terminals	51309142-125
STI FTA (MU-TSTX53)	STI with screw terminals	51309142-225
LLAI FTA (MU-TAIL02)	LLAI FTA with compression terminals (Replaced by MU-TAIL03)	51304437-100
	Daughter module for above FTA	51304085-100
LLAI FTA (MU-TAIL03)	LLAI FTA with compression terminals	51309202-125
LLMux FTA (MU-TAMT02)	LLMux local TC with compression terminals (Replaced by MU-TAMT03)	51401491-100
	LLMux Analog board for above FTA	51401564-100
LLMux FTA (MU-TAMT03)	LLMux local TC with compression terminals	51409223-125
LLMux FTA (MU-TAMT12)	LLMux remote TC with compression terminals (Replaced by MU-TAMT13)	51401573-100
	LLMux Analog board for above FTA	51401564-100
	LLMux remote sensor board for above FTA	51304589-100
LLMux FTA (MU-TAMT13)	LLMux remote TC with compression terminals	51409213-125
LLMux FTA (MU-TAMR02)	LLMux RTD with compression terminals (Replaced by MU-TAMR03)	51304477-100
	LLMux daughter board for above FTA	51401364-100
LLMux FTA (MU-TAMR03)	LLMux RTD with compression terminals	51309218-125
AO FTA (MU-TAOX02)	Analog Output with compression terminals	51304476-125
AO FTA (MU-TAOX12)	Analog Output with compression terminals	51304335-125
AO FTA (MU-TAOX52)	Analog Output with screw terminals	51304335-225
	Plug-in module for above FTAs	51304338-100

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
STANDARD FTA COMPONENTS, continued		
AO FTA (MU-TAOY22)	Analog Output with comp term, Stdby Manual	80366481-125
AO FTA (MU-TAOY23)	Analog Output with comp term, no Stdby Manual	80366177-200
AO FTA (MU-TAOY52)	Analog Output with screw term, Stdby Manual	80366484-125
AO FTA (MU-TAOY53)	Analog Output with screw term, no Stdby Manual	80364007-200
DI 120 Vac FTA (MU-TDIA12)	Digital Input 120 Vac with compression terminals	51304439-125
DI 120 Vac FTA (MU-TDIA52)	Digital Input 120 Vac with fixed-screw terminals	51304439-225
	Plug-in module for above FTAs	51190523-225
DI 120 Vac FTA (MU-TDIA72)	Digital Input 120 Vac with removable screw term	51303930-100
DI 240 Vac FTA (MU-TDIA22)	Digital Input 240 Vac with compression terminals	51304431-125
DI 240 Vac FTA (MU-TDIA62)	Digital Input 240 Vac with fixed-screw terminals	51304431-225
	Plug-in module for above FTAs	51190523-325
DI 24 Vdc FTA (MU-TDID12)	Digital Input 24 Vdc with compression terminals	51304441-125
DI 24 Vdc FTA (MU-TDID52)	Digital Input 24 Vdc with fixed-screw terminals	51304441-225
	Plug-in module for above FTAs	51190523-125
DI 24 Vdc FTA (MU-TDID72)	Digital Input 24 Vdc with removable screw term	51303928-100
DI 24 Vdc FTA (MU-TDIY22)	Digital Input 24 Vdc with compression terminals	80366180-100
DI 24 Vdc FTA (MU-TDIY62)	Digital Input 24 Vdc with screw terminals	80364010-100
DO 120/240 Vac FTA (MU-TDOA12)	DO 120/240 Vac SS with fixed-compression term (Replaced by MU-TDOA13)	51304408-100
DO 120/240 Vac FTA (MU-TDOA52)	DO 120/240 Vac SS with fixed-screw terminals (Replaced by MU-TDOA53)	51304408-200
	Solid-state relay plug-in module for above FTAs	51190516-325
DO 120/240 Vac FTA (MU-TDOA13)	DO 24-240 Vac SS with removable comp term.	51304648-125
DO 120/240 Vac FTA (MU-TDOA53)	DO 24-240 Vac SS with removable screw term.	51304648-225
	Solid-state relay plug-in module for above FTAs	51190516-332
DO 3-30 Vdc FTA (MU-TDOD12)	DO 3-30 Vdc SS with fixed-compression terminals (Replaced by MU-TDOD13)	51304423-100
DO 3-30 Vdc FTA (MU-TDOD52)	DO 3-30 Vdc SS with fixed-screw terminals (Replaced by MU-TDOD53)	51304423-200
	Solid-state relay plug-in module for above FTAs	51190516-122
DO 3-30 Vdc FTA (MU-TDOD13)	DO 3-30 Vdc SS with removable comp terminals	51304650-100
DO 3-30 Vdc FTA (MU-TDOD53)	DO 3-30 Vdc SS with removable screw terminals	51304650-200
	Solid-state relay plug-in module for above FTAs	51190516-132

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
STANDARD FTA COMPONENTS, continued		
DO 3-30 Vdc FTA (MU-TDOD14)	DO 3-30 Vdc SS with fixed-compression term	51309153-125
DO 3-30 Vdc FTA (MU-TDOD54)	DO 3-30 Vdc SS with fixed-screw terminals	51309153-225
	Solid-state relay plug-in module for above FTAs	51190516-134
DO 31-200 Vac FTA (MU-TDOD22)	DO 31-200 Vdc SS with compression terminals	51304428-100
DO 31-200 Vac FTA (MU-TDOD62)	DO 31-200 Vdc SS with screw terminals	51304428-200
	Solid-state relay plug-in module for above FTAs	51190516-402
DO 31-200 Vac FTA (MU-TDOD23)	DO 31-200 Vdc SS with compression terminals	51309154-125
DO 31-200 Vac FTA (MU-TDOD63)	DO 31-200 Vdc SS with screw terminals	51309154-225
	Solid-state relay plug-in module for above FTAs	51190516-404
DO 24 Vdc FTA (MU-TDON12)	DO 24 Vdc nonisolated with comp. term	51304446-100
DO 24 Vdc FTA (MU-TDON52)	DO 24 Vdc nonisolated with screw term	51304446-200
DO 24 Vdc FTA (MU-TDOY22)	DO 24 Vdc isolated with compression terminals	80366183-100
DO 24 Vdc FTA (MU-TDOY62)	DO 24 Vdc isolated with screw terminals	80364013-100
DO 120 Vac Relay (MU-TDOR12)	DO 120 Vac/125 Vdc with compression terminals (Replaced by 51309148-125)	51304443-100
DO 120 Vac Relay (MU-TDOR52)	DO 120 Vac/125 Vdc with screw terminals (Replaced by 51309148-225)	51304443-200
	Relay plug-in module for above assemblies	51191945-100
DO 120 Vac Relay (MU-TDOR12)	DO 120 Vac/125 Vdc with compression terminals	51309148-125
DO 120 Vac Relay (MU-TDOR52)	DO 120 Vac/125 Vdc with screw terminals	51309148-225
	Relay plug-in module for above assemblies	51191945-100
DO 240 Vac Relay (MU-TDOR22)	DO 240 Vac/125 Vdc with compression terminals (Replaced by 51309150-125)	51304427-100
DO 240 Vac Relay (MU-TDOR62)	DO 240 Vac/125 Vdc with screw terminals (Replaced by 51309150-225)	51304427-200
	Relay plug-in module for above assemblies	51191945-100
DO 240 Vac Relay (MU-TDOR22)	DO 240 Vac/125 Vdc with compression terminals	51309150-125
DO 240 Vac Relay (MU-TDOR62)	DO 240 Vac/125 Vdc with screw terminals	51309150-225
	Relay plug-in module for above assemblies	51191945-100
DO 240 Vac Relay (MU-TDOY23)	DO 240 Vac/125 Vdc with compression terminals	80366189-100
DO 240 Vac Relay (MU-TDOY63)	DO 240 Vac/125 Vdc with screw terminals	80366185-100
	Relay (NT1) for above assemblies	83970001-110
	Jumper for above assemblies	51190610-101

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
STANDARD FTA COMPONENTS, continued		
Pulse Input FTA (MU-TPIX12)	Pulse Input with compression terminals	51304084-125
Pulse Input FTA (MU-TPIX52)	Pulse Input with screw terminals	51304084-225
	Plug-in module for above FTAs	51201602-100
Serial Device Interface FTA (MU-TSDT02)	Serial Device Interface (Toledo 8142) FTA	51303932-201
	Plug-in module for above FTA	51303934-201
Serial Device Interface FTA (MU-TSDM02)	Serial Device Interface (Manual/Auto Station)	51303932-202
	Plug-in module for above FTA	51303934-202
Serial Device Interface FTA (MU-TSDU02)	Serial Device Interface (UDC 6000)	51303932-203
	Plug-in module for above FTA	51303934-203
Serial Interface (MU-TSIM12)	Serial Interface (Modbus)	51303932-401
	Plug-in module for above FTA	51303934-401
Serial Interface (MU-TSIA12)	Serial Interface (Allen-Bradley)	51303932-403
	Plug-in module for above FTA	51303934-403
Power Adapter (MU-TLPA02)	Power Adapter (Used with LLMux, SDI, and SI)	51309204-125
DI Power Dist Assy (MU-TDPR02)	Digital Input Power Distribution Assembly	51304425-125
DO Standby Manual (MU-SMDC02)	Digital Output Standby Manual Device with case	51304526-100
DO Standby Manual (MU-SMDX02)	Digital Output Standby Manual Device with case and cable	51304527-100
AO Standby Manual (MU-SMAC02)	Analog Output Standby Manual Device Assy with cable	51401277-100
Manual/Auto Station (MU-MASX02)	Honeywell Manual/Auto Station (part number PC6001-U-2MO-40-A0)	

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
GALVANICALLY ISOLATED FTA COMPONENTS		
HLAI FTA (MU-GAIH12)	HLAI FTA with GI Modules (Compress terminals) (Replaced by MU-GAIH13 – 51304718-125)	51304636-100
HLAI FTA (MU-GAIH82)	HLAI FTA with GI Modules (Crimp terminals) (Replaced by MU-GAIH83 – 51304718-325)	51304636-300
	HLAI Galvanic Isolation Module (MTL4041)	51191697-100
HLAI FTA (MU-GAIH13)	HLAI FTA with GI Modules (Compress terminals)	51304718-125
HLAI FTA (MU-GAIH83)	HLAI FTA with GI Modules (Crimp terminals)	51304718-325
	HLAI Galvanic Isolation Module (MTL4041B)	51191697-200
HLAI FTA (MU-GAIH14)	HLAI FTA with GI Modules (Compress terminals)	51304730-125
HLAI FTA (MU-GAIH84)	HLAI FTA with GI Modules (Crimp terminals)	51304730-325
	HLAI Galvanic Isolation Module MTL4041P)	51191928-100
HLAI FTA (MU-GAIH22)	HLAI FTA with GI Modules (Compress terminals)	51304748-125
HLAI FTA (MU-GAIH92)	HLAI FTA with GI Modules (Crimp terminals)	51304748-325
	HLAI Galvanic Isolation Module (MTL4041B)	51191697-200
HLAI Calibration Tool	HLAI calibration tool	51201450-100
24 Vdc DI FTA (MU-GDID12)	24 Vdc DI FTA with GI Modules (Compress Term)	51304640-125
24 Vdc DI FTA (MU-GDID82)	24 Vdc DI FTA with GI Modules (Crimp Terminals)	51304640-325
	24 Vdc DI Galvanic Isolation Module (MTL4016)	51191699-100
24 Vdc DI FTA (MU-GDID13)	24 Vdc DI FTA with GI Modules (Compress Term)	51304728-125
24 Vdc DI FTA (MU-GDID83)	24 Vdc DI FTA with GI Modules (Crimp Terminals)	51304728-325
	24 Vdc DI Galvanic Isolation Module (MTL4013)	51191926-100
AO FTA (MU-GAOX02)	AO nonredun FTA with GI Modules (Comp Term)	51304638-125
AO FTA (MU-GAOX72)	AO nonredun FTA with GI Modules (Crimp Term)	51304638-325
AO FTA (MU-GAOX12)	AO redundant FTA with GI Modules (Comp Term)	51304638-525
AO FTA (MU-GAOX82)	AO redundant FTA with GI Modules (Crimp Term)	51304638-725
	AO Galvanic Isolation Module (MTL4045B)	51192097-100
	Redundancy Module for FTA	51304338-100
DO FTA (MU-GDOD12)	DO FTA with GI Modules (Compression Terminals)	51304642-125
DO FTA (MU-GDOD82)	DO FTA with GI Modules (Crimp Terminals)	51304642-325
	DO Galvanic Isolation Module (MTL4021)	51191698-100
DO FTA (MU-GDOL12)	DO FTA with GI Modules (Compression Terminals)	51304736-125
DO FTA (MU-GDOL82)	DO FTA with GI Modules (Crimp Terminals)	51304736-325
	DO Galvanic Isolation Module (MTL4023)	51191927-100

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
GALVANICALLY ISOLATED FTA COMPONENTS, continued		
LFD Combiner Panel (MU-GLFD02)	Line Fault Detection Combiner Panel	51304732-125
Power Distribution Assembly (MU-GPRD02)	Galvanic Isolation Power Distribution Assembly	51304644-125
Marshalling Panel (MU-GMAR52)	Marshalling Panel	51309156-125
GI Module Connector	Comp-type terminal connector for GI Module Crimp-type terminal connector for GI Module 14-20 AWG wire crimp pins for above connector	51191738-100 51191737-100 51191737-201

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
MISCELLANEOUS COMPONENTS		
Card Case	Plastic case for IOP cards	51304072-100
	Plastic case for HPMM cards	51304072-200
Card Label	Label for HPM UCN Interface module	51109470-100
	Label for High-Performance Comm/Control card	51109604-100
	Label for High-Performance I/O Link card	51109605-100
	Label - Plain blue for IOP filler card	51109474-100
	Label for Low Level Analog Input IOP	51109475-100
	Label for High Level Analog Input IOP	51109476-100
	Label for Analog Output IOP	51109477-100
	Label for Digital Input IOP	51109478-100
	Label for Digital Output IOP	51109479-100
	Label for I/O Link Extender	51109480-100
	Label for Low Level Multiplexer IOP	51109486-100
	Label for Smart Transmitter Interface IOP	51109494-100
	Label for Serial Device Interface IOP	51109568-100
	Label for Serial Interface IOP	51109607-100
FTA Plug-in Terminal Block	8 Point terminal block	51190694-108
	12 Point terminal block	51190694-112
	8 Point terminal block, labeled 1-8, gold contacts, for LLAI	51190787-408
	8 Point terminal block, labeled 9-16, gold contacts, for LLAI	51190787-508
	11 Point terminal block, labeled 9-19, gold contacts, for LLAI	51190787-411
Terminal Block Cover	Cover for terminals on 8-channel LLAI FTA	*51201569-100

* Not an ORU part

Continued on next page

Non-conformally coated ORU parts list, continued

Table 9-2 Non-Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
MISCELLANEOUS COMPONENTS, continued		
Cabinet Fan Assembly	Cabinet Fan assembly, 115 Vac with alarm	51303940-100
	Cabinet Fan assembly, 230 Vac with alarm	51303940-200
Cabinet Fan	Cabinet Fan, 115 Vac	68A8976P1
	Cabinet Fan, 230 Vac	68A8976P2
Cabinet Fan Assembly Board	Cabinet Fan assembly board, 115 Vac	*51201475-100
	Cabinet Fan assembly board, 230 Vac	*51201475-200
Left 7- Slot Card File (MU-HPFH01)	Left 7-Slot HPMM/IOPcard file assy (slots 1-7)	51404125-100
Left 7- Slot Card File (MU-HPFH03)	Left 7-Slot HPMM card file assy (slots 1-7)	51404191-125
Left 7- Slot Card File (MU-HPFI03)	Left 7-Slot IOP card file assy (slots 1-7)	51404191-225
Left 7- Slot Card File Backplane	Left 7-Slot card file backplane assy (slots 1-7)	51401626-100
Right 7- Slot Card File (MU-HPFH11)	Right 7- Slot HPMM/IOP card file assy (9-15)	51404126-100
Right 7- Slot Card File (MU-HPFH13)	Right 7- Slot HPMM card file assy (slots 9-15)	51404192-125
Right 7- Slot Card File (MU-HPFI13)	Right 7- Slot IOP card file assy (slots 9-15)	51404192-225
Right 7- Slot Card File Backplane	Right 7- Slot card file backplane assy (slots 9-15)	51401629-100
15-Slot Card File (MU-HPFX02)	15-Slot HPMM/IOP card file assy (slots 1-15)	51404127-100
15-Slot Card File (MU-HPFX03)	15-Slot HPMM card file assy (slots 1-15)	51404193-125
15-Slot Card File (MU-HPFI23)	15-Slot IOP card file assy (slots 1-15)	51404193-225
15-Slot Card File Backplane	15-Slot card file backplane assy (slots 1-15)	51401632-100
IOP Only Card File (MU-IOFX02)	15 IOP Only card file assembly	51401546-100
IOP Only Card File Backplane	15 IOP Only card file backplane assembly	51402599-100
IOP Only Card File (MU-IOFX03)	15 IOP Only card file assembly	5140xxxx-100
IOP Only Card File Backplane	15 IOP Only card file backplane assembly	5140xxxx-100
Filler Plate	Filler plate between 7-Slot card files	51304720-100
Opto-Isolator	Solid-state opto-isolator for card files	51190516-202
Fuse Holder/Puller	Fuse holder/puller (15 IOP card file)	51190586-100
Fuse Holder/Puller	Fuse holder/puller (HPMM card files)	51309123-100
Jumper	Card file UCN node/I/O Link address plug jumper	51190624-900
Range Resistor	100 ohm range resistor	51190102-100
	250 ohm range resistor	51190102-200
Zero Ohm Resistor	Zero ohm resistor for Power System backplane when adding Battery Pack assembly	51190101-100

* Not an ORU part

Continued on next page

Conformally coated ORU parts list

Table 9-3 is a parts list of confomally coated HPM ORU assemblies.

Table 9-3 Conformally Coated HPM ORU Parts List

Name	Description	Part Number
POWER SYSTEM COMPONENTS		
Power Supply Module	Standard 20 A Power Supply Module	51109456-200
Power Supply Module	AC Only 8 A Power Supply Module	51190465-150
Power Supply Module	AC Only 16 A Power Supply Module	51190465-250
48 V Battery Backup	48 V Battery Pack assembly	51303948-100
Power System Backplane Assy	PM/APM Power System backplane	51401166-150
Power System Backplane Assy	HPM Power System backplane	51404172-150
AC/DC Distribution Assembly	AC Only power control and distribution board 115 Vac dual PSMs	51401135-150
AC/DC Distribution Assembly	AC Only power control and distribution board 115 Vac single PSM	51401135-250
AC/DC Distribution Assembly	AC Only power control and distribution board 230 Vac dual PSMs	51401135-350
AC/DC Distribution Assembly	AC Only power control and distribution board 230 Vac single PSM	51401135-450
CMOS Battery Backup Assembly	PM/APM Charger/monitor for CMOS memory	51303968-150
CMOS Battery Backup Assembly	HPM PS charger/monitor for CMOS memory	51309206-150

Continued on next page

Conformally coated ORU parts list, continued

Table 9-3 Conformally Coated HPM ORU Parts List, Continued

Name		Description	Part Number
HPMM CARDS/MODULE			
High-Performance Comm/Control		/Control card	51401635-150
High-Performance I/O Link		I/O Link Interface card	51401642-150
HPM UCN Interface		UCN Interface module	51402573-150
IOP CARDS			
HLAI IOP	(MC-PAIH02)	High Level Analog Input card	51304489-150
HLAI IOP	(MC-PAIH03)	High Level Analog Input card	51304754-150
LLAI IOP	(MC-PAIL02)	Low Level Analog Input card	51304481-150
LLMux IOP	(MC-PLAM02)	Low Level Multiplexer card	51304362-150
DI IOP	(MC-PDIX02)	Digital Input card	51304485-150
DI IOP	(MC-PDIY22)	Digital Input card	80363972-150
AO IOP	(MC-PAOX02)	Analog Output card	51304483-150
AO IOP	(MC-PAOX03)	Analog Output card ((Replaced by 51309152-175)	51304672-150
AO IOP	(MC-PAOX03)	Analog Output card	51309152-175
AO IOP	(MC-PAOY22)	Analog Output card	80363969-150
DO IOP	(MC-PDOX02)	Digital Output card	51304487-150
DO IOP	(MC-PDOY22)	Digital Output card	80363975-150
STI IOP	(MC-PSTX02)	Smart Transmitter Interface	51304516-150
STIM IOP	(MC-PSTX03)	Smart Transmitter Interface Multivariable	51304516-250
PI IOP	(MC-PPIX02)	Pulse Input card	51304386-150
SDI IOP	(MC-PSDX02)	Serial Device Interface card	51304362-250
SI IOP	(MC-PSIM11)	Serial Interface card	51304362-350
DISOE IOP	(MC-PDIS11)	Digital Input Sequence Of Events card	51304690-150
Slot Filler Card		Slot filler card	51304260-250
I/O LINK EXTENDER COMPONENTS			
I/Standard I/O Link Extender (MC-IOLM02)		Standard I/O Link Extender card Standard fiber optic Tx/Rx coupler (1) Standard fiber optic Tx/Rx coupler (3)	51304419-150 51201557-150 51201557-350
Long Distance I/O Link Extender (MC-ILDX02 – Replaced by MC-ILDX03)		Long Distance I/O Link Extender card Long Distance fiber optic Tx/Rx coupler (1)	51304532-150 51201616-150
Long Distance I/O Link Extender (MC-ILDX03)		Long Distance I/O Link Extender card Long Distance fiber optic Tx/Rx coupler (1)	51304532-150 51309208-150

Continued on next page

Conformally coated ORU parts list, continued

Table 9-3 Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
STANDARD FTA COMPONENTS		
HLAI/STI FTA (MC-TAIH02)	HLAI/STI with compression terminals	51304453-150
HLAI/STI FTA (MC-TAIH12)	HLAI/STI with compression terminals	51304337-150
HLAI/STI FTA (MC-TAIH22)	HLAI/STI with compression terminals	80366195-150
	AI Adapter Module for the above FTA	80367163-001
HLAI/STI FTA (MC-TAIH52)	HLAI/STI with screw terminals	51304337-250
HLAI/STI FTA (MC-TAIH62)	HLAI/STI with screw terminals	80366192-150
	AI Adapter Module for the above FTA	80360713-001
HLAI FTA (MC-TAIH03)	HLAI with compression terminals	51309136-175
HLAI FTA (MC-TAIH13)	HLAI with compression terminals	51309138-175
HLAI FTA (MC-TAIH23)	HLAI with compression terminals	80369165-175
	AI Adapter Module for the above FTA	80367163-001
HLAI FTA (MC-TAIH53)	HLAI with screw terminals	51309138-275
STI FTA (MC-TSTX03)	STI with compression terminals	51309140-175
STI FTA (MC-TSTX13)	STI with compression terminals	51309142-175
STI FTA (MC-TSTX53)	STI with screw terminals	51309142-275
LLAI FTA (MC-TAIL02)	LLAI FTA with compression terminals (Replaced by MC-TAIL03)	51304437-150
	Daughter module for above FTA	51304085-150
LLAI FTA (MC-TAIL03)	LLAI FTA with compression terminals	51309202-175
LLMux FTA (MC-TAMT02)	LLMux local TC with compression terminals (Replaced by MC-TAMT03)	51401491-150
	LLMux Analog board for above FTA	51401564-150
LLMux FTA (MC-TAMT03)	LLMux local TC with compression terminals	51409223-175
LLMux FTA (MC-TAMT12)	LLMux remote TC with compression terminals (Replaced by MC-TAMT13)	51401573-150
	LLMux Analog board for above FTA	51401564-150
	LLMux remote sensor board for above FTA	51304589-150
LLMux FTA (MC-TAMT13)	LLMux remote TC with compression terminals	51409213-175
LLMux FTA (MC-TAMR02)	RTD with compression terminals (Replaced by MC-TAMR03)	51304477-150
	LLMux daughter board for above FTA	51401364-100
LLMux FTA (MC-TAMR03)	LLMux RTD with compression terminals	51309218-125
AO FTA (MC-TAOX02)	Analog Output with compression terminals	51304476-175
AO FTA (MC-TAOX12)	Analog Output with compression terminals	51304335-175
AO FTA (MC-TAOX52)	Analog Output with screw terminals	51304335-275
	Plug-in module for above FTAs	51304338-150

Continued on next page

Conformally coated ORU parts list, continued

Table 9-3 Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
STANDARD FTA COMPONENTS, continued		
AO FTA (MC-TAOY22)	Analog Output with comp term, Stdby Manual	80366481-175
AO FTA (MC-TAOY23)	Analog Output with comp term, no Stdby Manual	80366177-250
AO FTA (MC-TAOY52)	Analog Output with screw term, Stdby Manual	80366484-175
AO FTA (MC-TAOY53)	Analog Output with screw term, no Stdby Manual	80364007-250
DI 120 Vac FTA (MC-TDIA12)	Digital Input 120 Vac with compression terminals	51304439-175
DI 120 Vac FTA (MC-TDIA52)	Digital Input 120 Vac with fixed-screw terminals	51304439-275
	Plug-in module for above FTAs	51190523-225
DI 120 Vac FTA (MC-TDIA72)	Digital Input 120 Vac with removable screw term	51303930-150
DI 240 Vac FTA (MC-TDIA22)	Digital Input 240 Vac with compression terminals	51304431-175
DI 240 Vac FTA (MC-TDIA62)	Digital Input 240 Vac with fixed-screw terminals	51304431-275
	Plug-in module for above FTAs	51190523-325
DI 24 Vdc FTA (MC-TDID12)	Digital Input 24 Vdc with compression terminals	51304441-175
DI 24 Vdc FTA (MC-TDID52)	Digital Input 24 Vdc with fixed-screw terminals	51304441-275
	Plug-in module for above FTAs	51190523-125
DI 24 Vdc FTA (MC-TDID72)	Digital Input 24 Vdc with removable screw term.	51303928-150
DI 24 Vdc FTA (MC-TDIY22)	Digital Input 24 Vdc with compression terminals	80366180-150
DI 24 Vdc FTA (MC-TDIY62)	Digital Input 24 Vdc with screw terminals	80364010-150
DO 120/240 Vac FTA (MC-TDOA12)	DO 120/240 Vac SS with fixed-compression term (Replaced by MC-TDOA13)	51304408-150
DO 120/240 Vac FTA (MC-TDOA52)	DO 120/240 Vac SS with fixed-screw terminals (Replaced by MC-TDOA53)	51304408-250
	Solid-state relay plug-in module for above FTAs	51190516-325
DO 120/240 Vac FTA (MC-TDOA13)	DO 24-240 Vac SS with removable comp term.	51304648-175
DO 120/240 Vac FTA (MC-TDOA53)	DO 24-240 Vac SS with removable screw term.	51304648-275
	Solid-state relay plug-in module for above FTAs	51190516-332
DO 3-30 Vdc FTA (MC-TDOD12)	DO 3-30 Vdc SS with fixed-compression terminals (Replaced by MC-TDOD13)	51304423-150
DO 3-30 Vdc FTA (MC-TDOD52)	DO 3-30 Vdc SS with fixed-screw terminals (Replaced by MC-TDOD53)	51304423-250
	Solid-state relay plug-in module for above FTAs	51190516-122
DO 3-30 Vdc FTA (MC-TDOD13)	DO 3-30 Vdc SS with removable comp terminals	51304650-150
DO 3-30 Vdc FTA (MC-TDOD53)	DO 3-30 Vdc SS with removable screw terminals	51304650-250
	Solid-state relay plug-in module for above FTAs	51190516-132

Continued on next page

Conformally coated ORU parts list, continued

Table 9-3 Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
STANDARD FTA COMPONENTS, continued		
DO 3-30 Vdc FTA (MC-TDOD14)	DO 3-30 Vdc SS with fixed-compression terminals	51309153-175
DO 3-30 Vdc FTA (MC-TDOD54)	DO 3-30 Vdc SS with fixed-screw terminals	51309153-275
	Solid-state relay plug-in module for above FTAs	51190516-134
DO 31-200 Vac FTA (MC-TDOD22)	DO 31-200 Vdc SS with compression terminals	51304428-150
DO 31-200 Vac FTA (MC-TDOD62)	DO 31-200 Vdc SS with screw terminals	51304428-250
	Solid-state relay plug-in module for above FTAs	51190516-402
DO 31-200 Vac FTA (MC-TDOD23)	DO 31-200 Vdc SS with compression terminals	51309154-175
DO 31-200 Vac FTA (MC-TDOD63)	DO 31-200 Vdc SS with screw terminals	51309154-275
	Solid-state relay plug-in module for above FTAs	51190516-404
DO 24 Vdc FTA (MC-TDON12)	DO 24 Vdc 100 ma nonisolated with comp. term.	51304446-150
DO 24 Vdc FTA (MC-TDON52)	DO 24 Vdc 100 ma nonisolated with screw term.	51304446-250
DO 120 Vac Relay (MC-TDOR12)	DO 120 Vac/125 Vdc with compression terminals (Replaced by 51309148-125)	51304443-150
DO 120 Vac Relay (MC-TDOR52)	DO 120 Vac/125 Vdc with screw terminals (Replaced by 51309148-225)	51304443-250
	Relay plug-in module for above assemblies	51191945-100
DO 120 Vac Relay (MC-TDOR12)	DO 120 Vac/125 Vdc with compression terminals	51309148-175
DO 120 Vac Relay (MC-TDOR52)	DO 120 Vac/125 Vdc with screw terminals	51309148-275
	Relay plug-in module for above assemblies	51191945-100
DO 240 Vac Relay (MC-TDOR22)	DO 240 Vac/125 Vdc with compression terminals (Replaced by 51309150-125)	51304427-150
DO 240 Vac Relay (MC-TDOR62)	DO 240 Vac/125 Vdc with screw terminals (Replaced by 51309150-225)	51304427-250
	Relay plug-in module for above assemblies	51191945-100
DO 240 Vac Relay (MC-TDOR22)	DO 240 Vac/125 Vdc with compression terminals	51309150-175
DO 240 Vac Relay (MC-TDOR62)	DO 240 Vac/125 Vdc with screw terminals	51309150-275
	Relay plug-in module for above assemblies	51191945-150
DO 240 Vac Relay (MC-TDOY23)	DO 240 Vac/125 Vdc with compression terminals	80366189-150
DO 240 Vac Relay (MC-TDOY63)	DO 240 Vac/125 Vdc with screw terminals	80366185-150
	Relay (NT1) for above assemblies	83970001-110
	Jumper for above assemblies	51190610-101

Continued on next page

Conformally coated ORU parts list, continued

Table 9-3 Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
STANDARD FTA COMPONENTS, continued		
Pulse Input FTA (MC-TPIX12)	Pulse Input with compression terminals	51304084-175
Pulse Input FTA (MC-TPIX52)	Pulse Input with screw terminals	51304084-275
	Plug-in module for above FTAs	51201602-100
Serial Device Interface FTA (MC-TSDT02)	Serial Device Interface (Toledo 8142) FTA	51303932-251
	Plug-in module for above FTA	51303934-201
Serial Device Interface FTA (MC-TSDM02)	Serial Device Interface (Manual/Auto Station)	51303932-252
	Plug-in module for above FTA	51303934-202
Serial Device Interface FTA (MC-TSDU02)	Serial Device Interface (UDC 6000)	51303932-253
	Plug-in module for above FTA	51303934-203
Serial Interface (MC-TSIM12)	Serial Interface (Modbus)	51303932-476
	Plug-in module for above FTA	51303934-401
Serial Interface (MC-TSIA12)	Serial Interface (Allen-Bradley)	51303932-478
	Plug-in module for above FTA	51303934-403
Power Adapter (MC-TLPA02)	Power Adapter (Used with LLMux, SDI, and SI)	51309204-175
DI Power Dist Assy (MC-TDPR02)	Digital Input Power Distribution Assembly	51304425-175
DO Standby Manual (MC-SMDC02)	Digital Output Standby Manual Device with case	51304526-150
DO Standby Manual (MC-SMDX02)	Digital Output Standby Manual Device with case and cable	51304527-150
AO Standby Manual (MC-SMAC02)	Analog Output Standby Manual Device Assy with cable	51401277-150

Continued on next page

Conformally coated ORU parts list, continued

Table 9-3 Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
GALVANICALLY ISOLATED FTA COMPONENTS		
HLAI FTA (MC-GAIH12)	HLAI FTA with GI Modules (Compress terminals) (Replaced by MC-GAIH13 – 51304718-175)	51304636-150
HLAI FTA (MC-GAIH82)	HLAI FTA with GI Modules (Crimp terminals) (Replaced by MC-GAIH83 – 51304718-375)	51304636-350
	HLAI Galvanic Isolation Module (MTL4041)	51191697-100
HLAI FTA (MC-GAIH13)	HLAI FTA with GI Modules (Compress terminals)	51304718-175
HLAI FTA (MC-GAIH83)	HLAI FTA with GI Modules (Crimp terminals)	51304718-375
	HLAI Galvanic Isolation Module (MTL4041B)	51191697-200
HLAI FTA (MC-GAIH14)	HLAI FTA with GI Modules (Compress terminals)	51304730-175
HLAI FTA (MC-GAIH84)	HLAI FTA with GI Modules (Crimp terminals)	51304730-375
	HLAI Galvanic Isolation Module MTL4041P)	51191928-100
HLAI FTA (MC-GAIH22)	HLAI FTA with GI Modules (Compress terminals)	51304748-175
HLAI FTA (MC-GAIH92)	HLAI FTA with GI Modules (Crimp terminals)	51304748-375
	HLAI Galvanic Isolation Module (MTL4041B)	51191697-200
HLAI Calibration Tool	HLAI calibration tool	51201450-100
24 Vdc DI FTA (MC-GDID12)	24 Vdc DI FTA with GI Modules (Compress Term)	51304640-175
24 Vdc DI FTA (MC-GDID82)	24 Vdc DI FTA with GI Modules (Crimp Terminals)	51304640-375
	24 Vdc DI Galvanic Isolation Module (MTL4016)	51191699-100
24 Vdc DI FTA (MC-GDID13)	24 Vdc DI FTA with GI Modules (Compress Term)	51304728-175
24 Vdc DI FTA (MC-GDID83)	24 Vdc DI FTA with GI Modules (Crimp Terminals)	51304728-375
	24 Vdc DI Galvanic Isolation Module (MTL4013)	51191926-100
AO FTA (MC-GAOX02)	AO FTA with GI Modules (Comp Term)	51304638-175
AO FTA (MC-GAOX72)	AO FTA with GI Modules (Crimp Term)	51304638-375
AO FTA (MC-GAOX12)	AO FTA with GI Modules (Comp Term)	51304638-575
AO FTA (MC-GAOX82)	AO FTA with GI Modules (Crimp Term)	51304638-775
	AO Galvanic Isolation Module (MTL4045)	51192097-100
	Redundancy Module for FTA	51304338-100
DO FTA (MC-GDOD12)	DO FTA with GI Modules (Compression Terminals)	51304642-175
DO FTA (MC-GDOD82)	DO FTA with GI Modules (Crimp Terminals)	51304642-375
	DO Galvanic Isolation Module (MTL4021)	51191698-100
DO FTA (MC-GDOL12)	DO FTA with GI Modules (Compression Terminals)	51304736-175
DO FTA (MC-GDOL82)	DO FTA with GI Modules (Crimp Terminals)	51304736-375
	DO Galvanic Isolation Module (MTL4023)	51191927-100

Continued on next page

Conformally coated ORU parts list, continued

Table 9-3 Conformally Coated HPM ORU Parts List, Continued

Name	Description	Part Number
GALVANICALLY ISOLATED FTA COMPONENTS, continued		
LFD Combiner Panel (MC-GLFD02)	Line Fault Detection Combiner Panel	51304732-175
Power Distribution Assembly (MC-GPRD02)	Galvanic Isolation Power Distribution Assy	51304644-175
Marshalling Panel (MC-GMAR52)	Marshalling Panel	51309156-175
MISCELLANEOUS COMPONENTS, continued		
Cabinet Fan Assembly	Cabinet Fan assembly, 115 Vac with alarm Cabinet Fan assembly, 230 Vac with alarm	51303940-150 51303940-250
Cabinet Fan Assembly	Cabinet Fan assembly, 115 Vac Cabinet Fan assembly, 230 Vac	*51201475-150 *51201475-250
Left 7- Slot Card File (MC-HPFH01)	Left 7-Slot HPMM/IOPcard file assy (slots 1-7)	51404125-150
Left 7- Slot Card File (MC-HPFH03)	Left 7-Slot HPMM card file assy (slots 1-7)	51404191-175
Left 7- Slot Card File (MC-HPFI03)	Left 7-Slot IOP card file assy (slots 1-7)	51404191-275
Left 7- Slot Card File Backplane	Left 7-Slot card file backplane assy (slots 1-7)	51401626-150
Right 7- Slot Card File (MC-HPFH11)	Right 7- Slot HPMM/IOP card file assy (9-15)	51404126-150
Right 7- Slot Card File (MC-HPFH13)	Right 7- Slot HPMM card file assy (slots 9-15)	51404192-175
Right 7- Slot Card File (MC-HPFI13)	Right 7- Slot IOP card file assy (slots 9-15)	51404192-275
Right 7- Slot Card File Backplane	Right 7- Slot card file backplane assy (slots 9-15)	51401629-150
15-Slot Card File (MC-HPFX02)	15-Slot HPMM/IOP card file assy (slots 1-15)	51404127-150
15-Slot Card File (MC-HPFX03)	15-Slot HPMM card file assy (slots 1-15)	51404193-175
15-Slot Card File (MC-HPFI23)	15-Slot IOP card file assy (slots 1-15)	51404193-275
15-Slot Card File Backplane	15-Slot card file backplane assy (slots 1-15)	51401632-150
IOP Only Card File (MC-IOFX02)	15 IOP Only card file assembly	51401546-150
IOP Only Card File Backplane	15 IOP Only card file backplane assembly	51402599-150
IOP Only Card File (MC-IOFX03)	15 IOP Only card file assembly	5140xxxx-150
IOP Only Card File Backplane	15 IOP Only card file backplane assembly	5140xxxx-150
Filler Plate	Filler plate between 7-Slot card files	51304720-150

* Not an ORU part

9.4 UCN Parts

UCN Parts list

The UCN spare parts are listed in Table 9-4 for easy reference. This same list of spare parts can also be found in the *Logic Manager Service* and *Process Manager/Advanced Process Manager Service* manuals. Information about these parts can be found in the *High-Performance Process Manager Installation* and the *Universal Control Network (UCN) Planning* manuals.

Table 9-4 UCN Parts List

Name	Description		Part Number
UCN Drop Cable	RG-6 UCN drop cable (pair)		
		0.5 meter	51195153-900
		1.5 meters	51195153-901
	MU-NKD002	2.0 meters	51195153-002
		2.5 meters	51195153-902
		3.5 meters	51195153-903
		4.5 meters	51195153-904
	MU-NKD005	5.0 meters	51195153-005
	MU-NKD010	10.0 meters	51195153-010
	MU-NKD020	20.0 meters	51195153-020
	MU-NKD030	30.0 meters	51195153-030
	MU-NKD040	40.0 meters	51195153-040
	MU-NKD050	50.0 meters	51195153-050
UCN Trunk Cable	RG-11 UCN trunk cable (pair) – internal application		
	MU-NKT002	2.6 meters	51195199-002
	MU-NKT005	5.2 meters	51195199-005
	MU-NKT010	10.4 meters	51195199-010
	MU-NKT020	20.8 meters	51195199-020
	MU-NKT030	31.2 meters	51195199-030
	MU-NKT040	41.6 meters	51195199-040
	MU-NKT050	52.0 meters	51195199-050
	MU-NKT100	101.4 meters	51195199-100
	MU-NKT200	200.2 meters	51195199-200
	MU-NKT400	400.4 meters	51195199-400
	MU-NKT600	600.6 meters	51195199-600
UCN Trunk Cable	UCN trunk cable RG-11 – external application		
		152.4 meters	51191607-152
		304.9 meters	51191607-305
		762.4 meters	51191607-762
UCN Trunk Cable	UCN trunk cable RG-11 – internal application		51190899-xxx
		152.4 meters	51190899-152
		304.9 meters	51190899-305
		762.4 meters	51190899-762

Continued on next page

UCN Parts list,
continued

Table 9-3 UCN Parts List, Continued

Name	Description	Part Number
UCN Trunk Tap Kit		
	2-Drop tap assembly kit (pair) (MU-NTAP02)	51201394-100
	4-Drop tap assembly kit (pair) (MU-NTAP04)	51201395-100
	8-Drop tap assembly kit (pair) (MU-NTAP08)	51109485-100
UCN Tap Terminator	UCN tap terminator	51190782-100
Trunk Splice Kit	Splice kit for RG-11 (MU-NCSK01)	51195160-100
Trunk Cable Connector Kit	RG-6 drop cable connect kit W/O tool (MU-NKDK01)	51195161-100
	RG-11 trunk cable connect kit W/O tool (MU-NKTK01)	51195162-100
Connector Tool	RG-6 drop cable connector tool (MU-NKDT01)	51190797-200
	RG-11 trunk cable connector tool (MU-NKTT01)	51190795-200
Connector Torque Wrench	25 inch/pound torque wrench kit with three wrench heads for UCN connectors (MU-NKTQ01)	51109612-100

Index

+5 volt power margining 15
15-Slot card file 6
16-channel AO IOP display 217
16-channel DO IOP display 224
24 V battery backup exhaustion 290
24 Vdc distribution 62
24 Vdc fuse protection 64
3.6 Vdc battery output 51
32-channel DO IOP display 225
48 V battery replacement 371
48 Vdc Battery Backup Module 51
48 volt battery backup time 51
48 Volt Battery switch 58
5 Vdc fuse protection 81
6 Vac output 51
8-channel AO IOP display 216

A

AC Only Power System 4, 55, 327
ac power control 4
alkaline battery 55
Alphanumeric display format 295
Analog Output Standby Manual 353
AO FTA redundancy indicator 286
AO IOP calibration 393
AO IOP Detail Status display 216, 218
AO redundancy switching module replacement 368
AUTO CHECKPT target 131, 154

B

Battery Backup Module 58

C

Cabinet Fan assemblies 63
cabinet panel removal 377
card file designations 6
card file power cabling 82
card file replacement 369
card file types 6
CMOS backup assembly replacement 377
CMOS backup time 52
CMOS battery replacement 370
CMOS memory backup 60
CMOS memory NiCad battery backup 51
cold HPMM Startup 299
Comm/Control Hard failure codes 245
Comm/Control Soft failure error codes 269
Communications Error Block display 187
Communications Patches display 190
compression type terminals 47
Connection Test Detail display 344
Connection Test Summary display 340
connector
    compression-type terminal 44
    screw-type terminal 44
Control Error Block display 188
Control Patches display 189
CONTROL STATES target 129, 153
corrective actions 243
Crimp-pin type terminals 46

D

dc power control 4
debug connector 15
Detail Status display selection procedures 116
DETAIL STATUS target 143, 160
Detailed Diagnostic display switch 14
Detailed Display switch 294
device
    Allen-Bradley PLC-2 31
    Allen-Bradley PLC-3 31
    Allen-Bradley PLC-5 31
DI IOP Detail Status display 223
Diagnostic display 13
diagnostic tests 312
Digital Input IOP Detail Status display 223
Digital Output Standby Manual 359
DISOE IOP Detail Status display 230
display definitions 115
display operations 122
DO IOP Detail Status display 224

E

Electrostatic Discharge (ESD) wriststrap 346
ENABLE 145
ESD guidelines 347
ESD protection 346

F

Field Termination Assembly 38
fixed screw-type terminal connector 45
FTA 6
    model MU-TSIA12 31
    model MU-TSIM22 31
    mounting 43
    Serial Interface 31
FTA indicators 322
FTA module and relay replacement 368
FTA Mounting Channel 42, 48
FTA replacement 367
FTA sizes 41
FTA types 38

G

Galvanic isolation module replacement 369
Galvanically Isolated FTA types 40

H

Hard and Soft failure 232
Hard failure 232
hardware removal and replacement 345
High-Performance Comm/Control card 12
High-Performance I/O Link card 12
HLAI FTA redundancy indicator 286
HLAI IOP calibration 388
HLAI IOP Detail Status display 209
horizontal FTA Mounting Channel 48
HPM failure 232
HPM Partial failure 233
HPM Standard Power System 54
HPM Status display 144
HPM UCN Interface module 12
HPM Write Lockout Control display 180
HPMM 10
HPMM Alphanumeric display 294
HPMM alphanumeric display blanking 311
HPMM and IOP removal and replacement 348
HPMM card files 10
HPMM card indicators 290
HPMM card types 12
HPMM Control Configuration display 177
HPMM description 12
HPMM Detail Status displays 115, 166
HPMM functionality 12
HPMM Hard failure 233
HPMM I/O Link Information display 169
HPMM load display sequence 302
HPMM Maintenance Support display 187
HPMM module type 12
HPMM Node Status Information display 191
HPMM RAM Retention startup 306
HPMM Schedule Information display 183
HPMM Soft failure 233
HPMM Soft Failure display 194
HPMM swap verification 402
HPMM UCN Detail Status display 185
HPMM Version/Revision display 175

I, J, K

I/O Link Extender 32
I/O Link Information display 169
I/O Link Interface address pinning 105
I/O Link Interface cabling 88
I/O Link overruns 244
I/O Link overruns corrective actions 244
I/O Link processor Hard failure error codes 273
IOL CABLE COMMANDS target 155
IOP 6
    model MU-PSIM11 31
IOP Box Soft failure error codes 277
IOP calibration 379
IOP card files 18
IOP card indicators 320
IOP Detail Status display 197
IOP Detail Status displays 116
IOP Hard failure 234
IOP Hard failure error codes 275
IOP Only card file 6
IOP redundancy terminology 403
IOP redundancy test procedure 404
IOP Slot Soft failure error codes 283
IOP Slot Soft Failures display 205
IOP Soft failure 234
IOP Soft failure displays 201
IOP to FTA cabling 92
IOPs 20

L

Left 7-Slot card file 6
LLAI IOP calibration 381
LLAI IOP Detail Status display 211
LLAI line frequency clock voltage 63
LLAI line frequency noise cancellation clock circuit 51
LLAI Module replacement 368
LLMux FTAs 24
LLMux IOP 23
LLMux IOP calibration 397
LLMux IOP Detail Status display 220
LOAD/SAVE RESTORE target 127, 151
Long Distance I/O Link Extender 32

M

Manufacturing Information display 193
model
    MU-MASX02 28
model MU-TLPA02 31

N

NIM Detail Status displays 115, 161
NIM Driver Configuration display 161
nonredundant 15-Slot HPMM card file 6
nonredundant 7-Slot HPMM card file 7
nonredundant AO IOP calibration 393
nonredundant HLAI IOP calibration 388
Nonredundant IOP cable replacement 366
Notification displays 298

O

optical coupler module replacement 378
ORUs 412

P, Q

PI IOP Detail Status display 227
Power Adapter 31
Power Adapter cabling 94
power cable redundancy testing 407
power distribution 57
power interrupt switch 5
Power Supply Module 51
Power Supply Module redundancy testing 408
Power Supply Module replacement 376
Power System 6, 51
Power System replacement 370
Power System voltage checks 328
Pulse Input IOP Detail Status display 227

R

redundant 15-Slot HPMM card files 6
redundant 7-Slot HPMM card files 7
redundant AO IOP failure diagnosis 287
Redundant IOP cable replacement 366
removable screw-type terminal connector 45
Request Data Response test 335
Right 7-Slot card file 6
RUN STATES target 157
RUN STATES target display 140

S

SDI FTAs 25
SDI IOP 25
SDI IOP Detail Status display 228
SDI/SI module and fuse replacement 368
SI FTAs 29
SI IOP 29
SI IOP Detail Status display 229
SLOT SUMMARY target 142, 159
Slots with Soft Failures display 208
Soft failure 232
Standard FTAs 39
Standard I/O Link Extender 32
Standard Power System 51, 324
Standby Manual device 350
STI IOP and FTA faults 285
STI/STIM IOP Detail Status display 226

T

thermocouple input accuracy verification 399
total card files 18
total IOPs 18
triangulation test 336
troubleshooting flowchart 236
Troubleshooting flowcharts 235
Troubleshooting table usage 236
types of failures 232

U

UCN CABLE STATUS target 133
UCN cable system 97
UCN cable taps 98
UCN Exerciser Help display 339
UCN Exerciser Overview display 338
UCN Exerciser program 333
UCN Exerciser test procedure 342
UCN node address pinning 100
UCN Status displays 122
UDC 6000 28

V, W, X, Y, Z

vertical FTA Mounting Channel 48
Voltage Margin jumper plug 231

Index

READER COMMENTS

Honeywell's IAC Automation College welcomes your comments and suggestions to improve future editions of this and other publications.

You can communicate your thoughts to us by fax, mail, or toll-free telephone call. We would like to acknowledge your comments; please include your complete name and address.

BY FAX: Use this form; and fax to us at (602) 313-4108

BY TELEPHONE: In the U.S.A. use our toll-free number 1*800-822-7673 (available in the 48 contiguous states except Arizona; in Arizona dial 1-602-313-5558).

BY MAIL: Use this form; detach, fold, tape closed, and mail to us.

Title of Publication: **High-Performance Process Manager Service** Issue Date: **3/96**
Publication Number: **HP13-500**
Writer: **Bob Koegel**

COMMENTS: _____

_____

_____

_____

_____

_____

_____

_____

RECOMMENDATIONS: _____

_____

_____

_____

_____

_____

_____

_____

NAME _____ DATE _____

TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

(If returning by mail, please tape closed; Postal regulations prohibit use of staples.)

Communications concerning technical publications should be directed to:

Automation College
Industrial Automation and Control
Honeywell Inc.
2820 West Kelton Lane
Phoenix, Arizona 85023

FOLD FOLD

From: _____

_____

_____

NO POSTAGE
NECESSARY
IF MAILED
IN THE USA

BUSINESS REPLY MAIL

FIRST CLASS **PERMIT NO. 4332** PHOENIX, ARIZONA

POSTAGE WILL BE PAID BY ....

Honeywell

Industrial Automation and Control
2820 West Kelton Lane
Phoenix, Arizona 85023

Attention: Manager, Quality

FOLD FOLD

Cut Along Line

Additional Comments:

Honeywell

Industrial Automation and Control
Honeywell Inc.
16404 North Black Canyon Highway
Phoenix, Arizona 85023-3033

Helping You Control Your World