

# **High-Performance Process Manager Module Test System**

**HP13-505**



**PM/APM/HPM Service - 2**

***High-Performance  
Process Manager  
Module Test System***

**HP13-505  
Release 510  
10/96**

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## About This Publication

This Reference Manual documents the individual test programs that make up the High-Performance Process Manager Module Test System . It is intended for use by either Honeywell or customer service technicians who are responsible for the isolation of those TPS 3000 hardware failures that are not fully identified by the firmware and on-line software diagnostics. This publication is a reference manual for trained technicians and is intended to supplement TPS 3000 service training, not replace it.

This manual supports the High-Performance Process Manager (HPM).

This publication supports **TotalPlant** Solution (TPS) System network Release 510 and earlier R500 software releases. TPS is the evolution of TDC 3000<sup>X</sup>.

In order to use this manual, you must first be familiar with the content of the *Process Manager Test Executive (PMEX)*.

### NOTE

Hexadecimal numeric values are indicated in this manual by the use of a preceding "\$"; for example, \$0000 or \$FFFF.



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## INTRODUCTION

### Section 1

*This section introduces you to the characteristics and uses of HMMTS. It also provides a list of related publications.*

#### 1.1 WHAT HMMTS IS AND HOW IT WORKS

The High-Performance Process Manager Module Test System (HMMTS) is a collection of test programs that work under the Process Manager Test Executive (PMEX) and are used to verify the correct operation of TPS 3000 High-Performance Process Manager Modules (HPMMs and HPMs). Each test program is concerned with a specific High-Performance Process Manager Module subsystem. Table 1-1 lists the HMMTS test programs by the 4-character names accepted by PMEX.

All references to HPM in this document apply to the High-Performance Process Manager Module (HPMM) as well.

**Table 1-1 — HMMTS Test Program Names**

CCPU	—	Common CPU Tests
GMEM	—	Global Memory Tests
LMEM	—	Local Memory Tests
LNKI	—	I/O Link Tests
PSOE	—	Sequence of Events Tests
RDUN	—	Control Redundancy Tests
TBCS	—	Token Bus Controller Statistics

The test programs are subdivided into individual tests that are designed to verify correct operation of specific functions within the subsystem. You control the operation of HMMTS by keyboard entry of commands that specify the hardware to be tested and the number and sequence of tests to be run.

##### 1.1.1 HMMTS Packaging

HMMTS test programs are packaged with PMEX on either floppy diskette number 51150700 or cartridge disk 51152049. Follow the loading and test system setup instructions in the *Process Manager Test Executive* manual.

## 1.1.2 Test Program Execution

As defined in the individual test writeups, some HMMTS tests run in only one of the two primary HPMM processor board types (COMM and CTRL), while other tests can run in either (or both) processor type(s). The five defined processor testing combinations are

**COMM**—The test program runs in only the Communication processor type.

**CTRL**—The test program runs in only the Control processor type.

**Either**—The test program runs in either processor type and can run simultaneously in both processors within a node.

**COMM+** —The test program runs in only the Communication processor type, but requires interaction with the Control Processor in the same node.

**Either+** —The test program runs in either processor type (or both simultaneously), but requires interaction with the other processor type in the same node.

For those tests that require interaction between COMM and CTRL, only the execution processor is specified; a "server" program in the other processor automatically responds.

Normally, a High-Performance Process Manager Module contains both processor types, but the tests indicated to be "COMM" or "Either" (not "COMM+" or "Either+") can run in a PMM with only a COMM processor.

Simple single-node commands to execute any individual test in an inappropriate processor type are rejected and a error message is output at the TOCS. Similar errors found in a test list (assuming at least one test in the list is acceptable) are ignored.

## 1.2 USES OF HMMTS

HMMTS is useful during system installation and initial hardware validation.

## 1.3 REFERENCES

The following are other TPS 3000 test program publications that will be of use during installation and maintenance of TPS 3000 Process Manager Modules.

Publication Title	Publication Number	Binder Title	Binder Number
<i>Test System Executive</i>	SW13-510	LCN Service - 3	TPS 3060-3
<i>Process Manager Test Executive (PMEX)</i>	PM13-520	PM/APM/HPM Service - 2	TPS 3061-2
<i>Process Manager Test System (PMTS)</i>	PM13-510	PM/APM/HPM Service - 2	TPS 3061-2
<i>High-Performance Process Manager Checkout</i>	HP20-510	Implementation/HPM - 3	TPS 3066-3
<i>High-Performance Process Manager Service</i>	HP13-500	PM/APM/HPM Service - 1	TPS 3061-1

## COMMAND/CONTROL PROCESSOR TESTS (CCPU) Section 2

### 2.1 CCPU TEST ELEMENTS

The CCPU test verifies the integrity of the command and control processors. This includes checking for bus errors, SRAM parity errors, DRAM EDAC errors, Tracked RAM and interrupts, and uninterruptible read-modify-write DRAM operations. These tests provide verification of Flash ROM and Serial EPROM operations, the Watchdog timer, and the Four-Character Alpha-Numeric diagnostic display.

Previous versions of LMEM did not check the Tracked RAM parts of Local Memory. LMEM now checks the Tracked RAM, so the CCPU and RDUN test must share the Tracked RAM. If LMEM halts because the error limit is reached, LMEM holds on to the Tracked RAM and this can cause errors in CCPU and RDUN.

### 2.2 USE INFORMATION

When running CCPU on both processors, the `Operating_Mode` must be set to `BOTH_PROCESSOR`. When running CCPU in only one processor at a time, the `Operating_Node` must be set to `SINGLE_PROCESSOR`.

CCPU and GMEM use the same EDAC memory resources. If the user sets the “HALT ON ERROR” option, an error in CCPU may cause an error in the GMEM reserve EDAC resource process.

Test 9 is a “fatal” test and requires system reset/reload. This is a “Utility” test and therefore must be the only test running in the node.

### 2.3 SETUP PARAMETERS

#### 2.3.1 CCPU-Specific Setup Parameters

<b>Persist_Interval</b>	Numeric Range Inclusive: 0 to 5 This parameter controls the delay in 50 msec intervals between the initial hardware status check and delayed hardware status check. A value of 0 inhibits the delayed hardware status check. This parameter can be changed at any time.
<b>Miscompare_Limit</b>	Numeric Range Inclusive: 1 to 10 This parameter controls the number of miscompares reported per block during error checking. This parameter can be changed only while CCPU is off.
<b>First_Random</b>	Numeric Value: (Any Hex Value) This parameter is used to establish a starting point for the random number sequence used during testing. This parameter can be changed only while CCPU is off.

<b>WD_Processor</b>	String Value: COMM or CTRL This parameter controls which processor will conduct watchdog testing. The remaining processor monitors the test results and reports errors. This parameter can be changed only while CCPU is off.
<b>Operating_Mode</b>	String Value: SINGLE_PROCESSOR or BOTH_PROCESSORS This parameter is used to control the coordination between the two copies of CCPU running in the COMM and CTRL processors. If set to Single_Processor, the program assumes that it is to run without cooperation from the other processor and does not attempt coordination. If set to Both_Processors, the two copies of CCPU synchronize and perform coordinated testing. This parameter can be changed only while CCPU is off.
<b>Alpha_Numeric_Pattern</b>	String Range Inclusive: <space> to <underbar> This parameter is used by the four-character alpha-numeric display test number 10. It can be changed at any time.
<b>Areas_Allowed</b>	String Value: NO_AREAS, MODEL_ONLY, DOMAIN_ONLY, or BOTH_AREAS This parameter is used for developer testing and should be left at its default setting. This parameter can be changed only while CCPU is off.
<b>Limit_Bus_Error</b> (Temporary)	Boolean: FALSE or TRUE This parameter limits the Test 1 Bus Error to the 12-Mbytes expansion block (\$00400000-\$00FFFFFF). This parameter can be changed only while CCPU is off.
<b>Prevent_Global_Bus_Errors</b> (Temporary)	Boolean: FALSE or TRUE This parameter prevents the Test 1 Bus Error testing from accessing the reserved Global Bus Address Space (\$05000000-\$08FFFFFF). If the “Limit_Bus_Error_Testing” is set to TRUE, then this parameter has no effect. This parameter can be changed only while CCPU is off.
<b>Enable</b>	String Value: COMMUNICATIONS_DEBUG, TAS_DEBUG, or TRACKED_RAM_DEBUG This parameter is used for developer testing and should be left at the default setting. This parameters can be changed at any time.
<b>Disable</b>	String Value: COMMUNICATIONS_DEBUG, TAS_DEBUG, or TRACKED_RAM_DEBUG This parameter is used for developer testing and should be left at the default setting. This parameters can be changed at any time.
<b>Tests</b>	Numeric Range Inclusive: 1 to 10

### 2.3.2 General Parameters

<b>Tests</b>	Numeric Range Inclusive: (test dependent)
<b>Error_Limit</b>	Numeric Range Inclusive: 1 through 32767 or –
<b>Pass_Limit</b>	Numeric Range Inclusive: 1 through 32767 or –
<b>Report</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Inhibit</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Scale</b>	Numeric Range Inclusive: 0 to 999
<b>Minutes_Limit</b>	Numeric Range Inclusive: 0 to 32767 or –
<b>Abbreviation</b>	Numeric Range Inclusive: 0 to 4

### 2.4 PRESET PARAMETER VALUES FOR CCPU

Persist\_Interval = 1  
 Miscompare\_Limit = 10  
 First\_Random = 0  
 WD\_Processor = COMM  
 Operating\_Mode = BOTH\_PROCESSORS  
 Alpha\_Numeric\_Pattern = @@@@  
 Areas\_Allowed = BOTH  
 Limit\_Bus\_Error (Temporary) = FALSE  
 Prevent\_Global\_Bus\_Errors (Temp) = FALSE  
 Enable = <no entry>  
 Disable = COMMUNICATIONS\_DEBUG, TAS\_DEBUG, TRACKED\_RAM\_DEBUG  
 Tests = 1-10  
 Error\_Limit = 5  
 Pass\_Limit = –  
 Report = LOG  
 Inhibit = PASSNUMBER, TESTNUMBER, SUSPENDED  
 Scale = 100  
 Minutes = –  
 Abbreviation = 4

### 2.5 MODE CHARACTERISTICS FOR CCPU

<u>System Mode</u>	<u>Programs Running</u>	<u>Tests Running</u>	<u>Delay Between Tests</u>
Subsystem	Only one	One or more	None
Module	One or more	One or more	Random

## 2.6 INDIVIDUAL CCPU TESTS

<b>Test Number/Description</b>	<b>Processor</b>	<b>Run Mode</b>
Test 01—Bus Error Test Verifies proper generation and detection of Bus Error events.	COMM, CTRL	SUB, MOD
Test 02—Parity Error Test Verifies proper generation of Bus Errors caused by SRAM parity errors.	COMM, CTRL	SUB, MOD
Test 03—EDAC Error Test Verifies proper generation of Bus Errors caused by DRAM EDAC errors.	COMM, CTRL	SUB, MOD
Test 04—Tracked RAM Register Test Verifies proper operation of the Tracked RAM start, bounds and current address registers.	COMM, CTRL	SUB, MOD
Test 05—Tracked RAM Test Verifies proper operation of Tracked RAM and Tracking RAM using both COMM and CTRL processors.	COMM, CTRL	SUB, MOD
Test 06—Read-Modify-Write (TAS) Test Verifies proper operation of the DRAM access arbitration logic.	COMM, CTRL	SUB
Test 07—Flash ROM Test (Verifies hardware ability to update a FLASH ROM test cell.	COMM	SUB, MOD
Test 08—Serial EEPROM Test Verifies COMM/CTRL board and UCN modem serial EEPROM operation.	COMM	SUB, MOD
Test 09—Watchdog Test—fatal test Destructive test that requires manual intervention to verify the Watchdog Timer.	COMM, CTRL	SUB
Test 10—Four-Character Alpha-Numeric Display Test Manual intervention test allowing the operator to display characters on the status LEDs.	COMM	SUB

## GLOBAL MEMORY TESTS (GMEM) Section 3

### 3.1 GLOBAL MEMORY TEST ELEMENTS

These tests provide verification of the SRAM Global memory board circuitry. This includes global memory cell uniqueness, memory arbitration circuitry, and EDAC circuitry.

### 3.2 USE INFORMATION

The GMEM and CCPU tests use the same EDAC memory resources. If the user sets the "HALT ON ERROR" option, an error in GMEM may cause an error in the CCPU reserve EDAC resource process.

The COMM card and the CTRL card can both be running tests in the global memory and will arbitrate for use of Global memory areas.

### 3.3 SETUP PARAMETERS

#### 3.3.1 GMEM-Specific Parameters

none

#### 3.3.2 General Parameters

<b>Tests</b>	Numeric Range Inclusive: 1 through 5
<b>Error_Limit</b>	Numeric Range Inclusive: 1 through 32767 or "-"
<b>Pass_Limit</b>	Numeric Range Inclusive: 1 through 32767 or "-"
<b>Report</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Inhibit</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Scale</b>	Numeric Range Inclusive: 0 to 999
<b>Minutes_Limit</b>	Numeric Range Inclusive: 0 to 32767 or "-"
<b>Abbreviation</b>	Numeric Range Inclusive: 0 to 4

### 3.4 PRESET PARAMETER VALUES FOR GMEM

Tests = 1-5  
 Error\_Limit = 5  
 Pass\_Limit = -  
 Report = LOG  
 Inhibit = PASSNUMBER,TESTNUMBER,SUSPENDED  
 Scale = 100  
 Minutes\_Limit = -  
 Abbreviation = 4

### 3.5 MODE CHARACTERISTICS FOR GMEM

<u>System Mode</u>	<u>Programs Running</u>	<u>Tests Running</u>	<u>Delay Between Tests</u>
Subsystem	Only one	One or more	None
Module	One or more	One or more	Random

### 3.6 INDIVIDUAL GLOBAL MEMORY TESTS

<b>Test Number/Description</b>	<b>Processor</b>	<b>Run Mode</b>
Test 01—Global Memory Function Test Performs a DRAM chip select, data access, and memory function test.	COMM, CTRL	SUB, MOD
Test 02—Global Memory Arbitration Test Verifies global memory cell data and cell address access uniqueness.	COMM, CTRL	SUB
Test 03—Global Memory Cell Test Verifies global memory cell data and cell address access uniqueness.	COMM, CTRL	SUB, MOD
Test 04—Global Memory Exerciser Test Verifies COMM/CTRL arbitration circuitry access to global memory.	COMM, CTRL	SUB, MOD
Test 05—Global Memory EDAC Test Verifies proper operation of the GMEM EDAC circuitry.	COMM, CTRL	SUB, MOD

**Section 4**

Reserved for future use.





## 5.4 PRESET PARAMETER VALUES FOR LMEM

Tests = 1-3  
 Error\_Limit = 5  
 Pass\_Limit = –  
 Report = LOG  
 Inhibit = PASSNUMBER, TESTNUMBER, SUSPENDED  
 Scale = 100  
 Minutes\_Limit = –  
 Abbreviation = 4

## 5.5 MODE CHARACTERISTICS FOR LMEM

<u>System Mode</u>	<u>Programs Running</u>	<u>Tests Running</u>	<u>Delay Between Tests</u>
Subsystem	Only one	One or more	None
Module	One or more	One or more	Random

## 5.6 INDIVIDUAL LOCAL MEMORY TESTS

<b>Test Number/Description</b>	<b>Processor</b>	<b>Run Modes</b>
Test 01—Local Memory Function Test Performs a chip select, data access, and TAS memory function test.	COMM, CTRL	SUB, MOD
Test 02—Local Memory Cell Test Verifies local memory cell data and cell address access uniqueness.	COMM, CTRL	SUB, MOD
Test 03—Local Memory Parity Test Verifies the proper operation of the local memory parity test circuitry.	COMM, CTRL	SUB, MOD

## I/O LINK TESTS (LNKI) Section 6

### 6.1 I/O LINK TESTS ELEMENTS

These tests verify the integrity of the HPMM I/O Link hardware. This includes the shared RAM, the 80c31 processor and its associated circuitry, the twisted pair interface, integrity circuits (such as Anti-Jabber and Watchdog Timer), and signals between the 80c31 I/O processor, and the COMM and CTRL processors.

### 6.2 LNK1 USE INFORMATION

Test 9 (see Note below) requires the dual I/O Link cable allowing Link1a to Link1b communication. This test runs only when the dual I/O Links are connected with the cable.

LNKI and RDUN use the same TBC resource. If the user sets the "HALT ON ERROR" option, an error in LNKI may cause an error in the RDUN reserve TBC resource process.

#### NOTE

The dual I/O Link card is a future enhancement to the current single I/O Link card. Using two single I/O Link cards is not the same as the dual I/O Link card.

## 6.3 SETUP PARAMETERS

### 6.3.1 LNKI-Specific Parameters

<b>Number_Of_Links</b>	Numeric Range Inclusive: 1 to 2 This parameter indicates the number of links on the I/O Link board. This parameter can be changed only while LNKI is off.
<b>Tests</b>	Numeric Range Inclusive: 1 to 14

### 6.3.2 General Parameters

<b>Tests</b>	Numeric Range Inclusive: 1 through 14
<b>Error_Limit</b>	Numeric Range Inclusive: 1 through 32767 or –
<b>Pass_Limit</b>	Numeric Range Inclusive: 1 through 32767 or –
<b>Report</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Inhibit</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Scale</b>	Numeric Range Inclusive: 0 to 999
<b>Minutes_Limit</b>	Numeric Range Inclusive: 0 to 32767 or –
<b>Abbreviation</b>	Numeric Range Inclusive: 0 to 4

## 6.4 PRESET PARAMETER VALUES FOR LNKI

Numer\_Of\_Links = 1  
 Tests = 1-14  
 Error\_Limit = 5  
 Pass\_Limit = –  
 Report = LOG  
 Inhibit = PASSNUMBER,TESTNUMBER,SUSPENDED  
 Scale = 100  
 Minutes\_Limit = –  
 Abbreviation = 4

## 6.5 MODE CHARACTERISTICS FOR LNKI

<u>System Mode</u>	<u>Programs Running</u>	<u>Tests Running</u>	<u>Delay Between Tests</u>
Subsystem	Only one	One or more	None
Module	One or more	One or more	Random

## 6.6 INDIVIDUAL I/O LINK TESTS

Test Number/Description	Processor	Run Modes
Test 01—Shared RAM Memory Test Tests the data lines and integrity of the shared RAM.	COMM, CTRL	SUB, MOD
Test 02—80c31 Reset and NOP Test Verifies that the 80c31 accepts commands properly.	COMM	SUB, MOD
Test 03—80c31 Watchdog Timer Test Tests that the Watchdog Timer operates properly.	COMM	SUB, MOD
Test 04—80c31 Suicide Test Verifies that the 80c31 never completes the suicide instruction.	COMM	SUB, MOD
Test 05—80c31 Memory Transfer Test Verifies that the 80c31 transfers data properly.	COMM, CTRL	SUB, MOD
Test 06—Shared RAM Arbitration Test Tests the shared bus arbitration logic.	COMM	SUB, MOD
Test 07—Received Interrupt Test Verifies that the 80c31 interrupt counter operates properly.	COMM, CTRL	SUB, MOD
Test 08—80c31 Jabber Test Verifies that the 80c31 interrupts upon receipt of the jabber signal.	COMM, CTRL	SUB, MOD
Test 09—Dual I/O Link Memory Transfer Test (Dual I/O Link Required) Verifies that the 80c31 can transfer data properly between both sections of a dual I/O Link card.	COMM, CTRL	SUB, MOD
Test 10—COMM/CTRL SRAM Parity Test Verifies that the COMM/CTRL can detect I/O Link shared RAM parity errors.	COMM, CTRL	SUB, MOD
Test 11—80c31 SRAM Parity Test (Processor = COMM only) Verifies the 80c31 can detect and handle bad shared RAM Primary and/or Backup area parity.	COMM, CTRL	SUB, MOD

Test 12—Free Running Counter Test Verifies that the Free Running Counter is operating within tolerance.	COMM, CTRL	SUB, MOD
Test 13—Transceiver Integrity Test Verifies that the I/O Link Transceivers operate properly.	COMM, CTRL	SUB, MOD
Test 14—Serial EEPROM Test Verifies that the I/O Link Serial EEPROM can be accessed properly.	COMM, CTRL	SUB, MOD

## CONTROL REDUNDANCY TESTS (RDUN) Section 7

### 7.1 CONTROL REDUNDANCY TESTS ELEMENTS

These tests verify integrity of the redundancy hardware in the TBC in an HPM pair. A pair consists of two HPMs physically linked as a primary and a secondary, which may or may not be in the same backplane.

### 7.2 USE INFORMATION

The RDUN test requires an installed redundancy cable (part number 51201667-100, revision B across the private path). If a node fails, the redundancy process will fail when it cannot communicate with its partner.

If the HPMM redundant pair is revision F or greater, a test cable (part number 51204100-100) can be installed across the alternate redundant path (the debug ports). With the test cable installed, the parameter `Test_Cable_Installed` should be set to YES. When the program is run, the alternate path is tested automatically through software control. If the parameter is set to NO and no test cable is installed, the path (private or alternate) that has the product cable (part number 51201667-100, revision B) installed across it will be tested. Either path is capable of redundant data transfer; however, only one path can be tested at a time in this configuration.

The RDUN and LNKI use the same TBC resource. If the user sets the “HALT ON ERROR” option, an error in RDUN may cause an error in the LNKI reserve TBC resource process.

### 7.3 SETUP PARAMETERS

#### 7.3.1 RDUN-Specific Parameters

<b>Partner_Installed</b>	<p>Boolean: NO or YES This parameter indicates whether the redundant partner is installed. It can only be changed while RDUN is off.</p>
<b>Test_Cable_Installed</b>	<p>Boolean: NO or YES This parameter is an indication to RDUN to test the HPM alternate redundant path between two redundant partners.</p> <p>NO = Special test cable has not been installed. Test the standard redundant path only.</p> <p>YES = Special test cable has been installed. Test both the standard redunant path and the alternate redundant path.</p>

### 7.3.2 General Parameters

<b>Tests</b>	Numeric Range Inclusive: 1 through 1
<b>Error_Limit</b>	Numeric Range Inclusive: 1 through 32767 or –
<b>Pass_Limit</b>	Numeric Range Inclusive: 1 through 32767 or –
<b>Report</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Inhibit</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Scale</b>	Numeric Range Inclusive: 0 to 999
<b>Minutes_Limit</b>	Numeric Range Inclusive: 0 to 32767 or –
<b>Abbreviation</b>	Numeric Range Inclusive: 0 to 4

### 7.4 PRESET PARAMETER VALUES FOR RDUN

Partner\_Installed = YES  
 Test\_Cable\_Installed = NO  
 Tests = 1  
 Error\_Limit = 5  
 Pass\_Limit = –  
 Inhibit = PASSNUMBER, TESTNUMBER, SUSPENDED  
 Scale = 100  
 Minutes\_Limit = –  
 Abbreviation = 4

### 7.5 MODE CHARACTERISTICS FOR RDUN

<u>System Mode</u>	<u>Programs Running</u>	<u>Tests Running</u>	<u>Delay Between Tests</u>
Subsystem	Only one	One or more	None
Module	One or more	One or more	Random

### 7.6 INDIVIDUAL RDUN TESTS

<b>Test Number/Description</b>	<b>Processor</b>	<b>Run Mode</b>
Test 01—TBC Data Transfer Test Verifies operation of the redundancy TBC during back-to-back transfers.	CTRL	SUB, MOD

## TOKEN BUS CONTROLLER STATISTICS (TBCS) Section 8

### 8.1 TOKEN BUS CONTROLLER TEST ELEMENTS

This test program monitors the UCN event statistics kept by the COMM boards in the HPM modules on a Universal Control Network.

### 8.2 USE INFORMATION

No special operating instructions.

### 8.3 SETUP PARAMETERS

#### 8.3.1 TBCS-Specific Parameters

<b>Clear_All_Statistics</b>	Boolean: NO or YES This parameter indicates whether to clear all statistics or not. It can be changed at any time.
<b>Print_All_Statistics</b>	Boolean: NO or YES This parameter indicates whether to print all statistics or not. It can be changed at any time.
<b>Rate</b>	Numeric range inclusive: 1 to 300 This parameter determines the number of seconds to wait between retrieving statistics. It can be changed at any time.
<b>Loops_Per_Pass</b>	Numeric range inclusive: 1 to 1000 This parameter determines the number of times to retrieve statistics. It can be changed at any time.
<b>Tests</b>	Numeric range inclusive: 1 to 1

#### 8.3.2 General Parameters

<b>Tests</b>	Numeric Range Inclusive: 1 through 1
<b>Error_Limit</b>	Numeric Range Inclusive: 1 through 32767 or –
<b>Pass_Limit</b>	Numeric Range Inclusive: 1 through 32767 or –
<b>Report</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Inhibit</b>	String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED
<b>Scale</b>	Numeric Range Inclusive: 0 to 999
<b>Minutes_Limit</b>	Numeric Range Inclusive: 0 to 32767 or –
<b>Abbreviation</b>	Numeric Range Inclusive: 0 to 4

## 8.4 PRESET PARAMETER VALUES FOR TBCS

Clear\_All\_Statistics = NO  
 Print\_All\_Statistics = NO  
 Rate = 5  
 Loops\_Per\_Pass = 1  
 Tests = 1  
 Error\_Limit = 5  
 Pass\_Limit = -  
 Report = LOG  
 Inhibit = PASSNUMBER,TESTNUMBER,SUSPENDED  
 Scale = 0  
 Minutes\_Limit = -  
 Abbreviation = 4

## 8.5 MODE CHARACTERISTICS FOR TBCS

<u>System Mode</u>	<u>Programs Running</u>	<u>Tests Running</u>	<u>Delay Between Tests</u>
Subsystem	Only one	One or more	None
Module	One or more	One or more	Random

## 8.6 INDIVIDUAL TOKEN BUS CONTROLLER TESTS

<b>Test Number/Description</b>	<b>Processor</b>	<b>Run Mode</b>
Test 01—Monitor Token Bus Statistics Reports all changes to any of the 22 Token Bus statistics counters.	COMM	SUB, MOD

## PROCESS SEQUENCE OF EVENTS (PSOE) Section 9

### 9.1 PROCESS SEQUENCE OF EVENTS TEST ELEMENTS

These tests provide verification of Message Decoder, Master Clock, and Synch Counter Carry functions.

### 9.2 USE INFORMATION

Test 3 runs only from a VIP connected to the COMM/CTRL board serial port.

### 9.3 SETUP PARAMETERS

#### 9.3.1 PSOE-Specific Parameters

**First\_Random**                      Numeric Range Inclusive: (Valid Hex Number)  
This parameter is used to establish a starting point for the random number sequence used during testing. This parameter can be changed only while PSOE is off.

**Tests**                                      Numeric range inclusive: 1 to 3

#### 9.3.2 General Parameters

**Tests**                                      Numeric Range Inclusive: 1 through 3  
**Error\_Limit**                              Numeric Range Inclusive: 1 through 32767 or –  
**Pass\_Limit**                                Numeric Range Inclusive: 1 through 32767 or –  
**Report**                                      String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED  
**Inhibit**                                    String Value: PASSNUMBER, TESTNUMBER, LOG, SUSPENDED  
**Scale**                                        Numeric Range Inclusive: 0 to 999  
**Minutes\_Limit**                          Numeric Range Inclusive: 0 to 32767 or –  
**Abbreviation**                            Numeric Range Inclusive: 0 to 4

### 9.4 PRESET PARAMETER VALUES FOR PSOE

First\_Random = 0  
Tests = 1-3  
Error\_Limit = –  
Pass\_Limit = –  
Report = LOG  
Inhibit = PASSNUMBER, TESTNUMBER, SUSPENDED  
Scale = 100  
Minutes\_Limit = –  
Abbreviation = 4

## 9.5 MODE CHARACTERISTICS FOR PSOE

<u>System Mode</u>	<u>Programs Running</u>	<u>Tests Running</u>	<u>Delay Between Tests</u>
Subsystem	Only one	One or more	None
Module	One or more	One or more	Random
Utility	Only one	Only one	None

## 9.6 INDIVIDUAL PROCESS SEQUENCE OF EVENTS TESTS

<b>Test Number/Description</b>	<b>Processor</b>	<b>Run Mode</b>
Test 01—Message Decoder Test Verifies operation of the UCN Decoder logic.	COMM	SUB
Test 02—Master Clock Test Verifies proper Watchdog Timer and Free Running Counter clocking operation.	COMM	SUB, MOD
Test 03—Synch Counter Carry Test Verifies the Synch Counter carry bits functionality.	COMM	UTIL

## 9.7 ALARM MESSAGES AND DESCRIPTIONS

If the Time Synch gate array Status Register contents do not match the expected values, an alarm is displayed.

```
DD-MMM-YYYY HH:MM:SS NMA nn COMM nn Alarm TEST#nn
WHILE EXECUTING SOME TEST ACTION - TIME SYNCH STATUS REGISTER
    WAS - $XXXX
EXPECTED - $YYYY
    MASK - $ZZZZ
```

If one or both of the Time Synch gate array Synch Latches' contents do not match the expected values, alarms will be displayed.

```
DD-MMM-YYYY HH:MM:SS NMA nn COMM nn Alarm TEST#nn
WHILE LATCHING TYPT SYNCH LATCH - TYPE SYNCH LATCH
    WAS - $XXXX XXXX
EXPECTED - $YYYY YYYY
    MASK - $ZZZZ ZZZZ
```

Where TYPT is the type of Synch Counter/Latch under test and TYPE is the Synch Latch exhibiting an error. The possible values to each Synch Counter/Latch TYPx are AUX or UCN.

If the difference in Master Clock counts in test 4 doesn't match the expected value, an alarm is displayed.

```
DD-MMM-YYYY HH:MM:SS NMA nn COMM nn Alarm 4nn
MASTER CLOCK TEST - MASTER CLOCK COUNT
    UCN WAS - $XXXX XXXX
AUX LATCH WAS - $YYYY YYYY
DIFFERENCE WAS - $ZZZZ ZZZZ
EXPECTED DIFFERENCE WAS 2000 + OR - TOLERANCE
```

If Random numbers were used for a test that caused an alarm message, the following message will be appended to the alarm message.

```
FIRST_RANDOM USED FOR THIS TEST - $XXXX
```



## READER COMMENTS

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**COMMENTS:** \_\_\_\_\_  
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